DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

Dr. Khader Mohammad

Lecture #11

Parasitic Capacitance Estimation

Digital Integrated Circuits

	Course topics and Schedule
	Subject
1	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design The CMOS inverter
5	Combinational logic structures
6	Layout of an Inverter and basic gates
7 8	Static CMOS Logic Dynamic Logic
9	Sequential logic gates; Latches and Flip-Flops
10	Summary : Device modeling parameterization from I-V curves.
11	Interconnect: R, L and C - Wire modeling
12	Parasitic Capacitance Estimation
13	Timing
14	Power dissipation;
15	Clock Distribution
16	SPICE Simulation Techniques (Project)
17	Arithmetic building blocks
18	Memories and array structures
19	Supply and Threshold Voltage Scaling
20	Reliability and IC qualification process
21	Advanced Voltage Scaling Techniques
22	Power Reduction Through Switching Activity Reduction
23	CAD tools and algorithms
24	SPICE Simulation Techniques (Project)

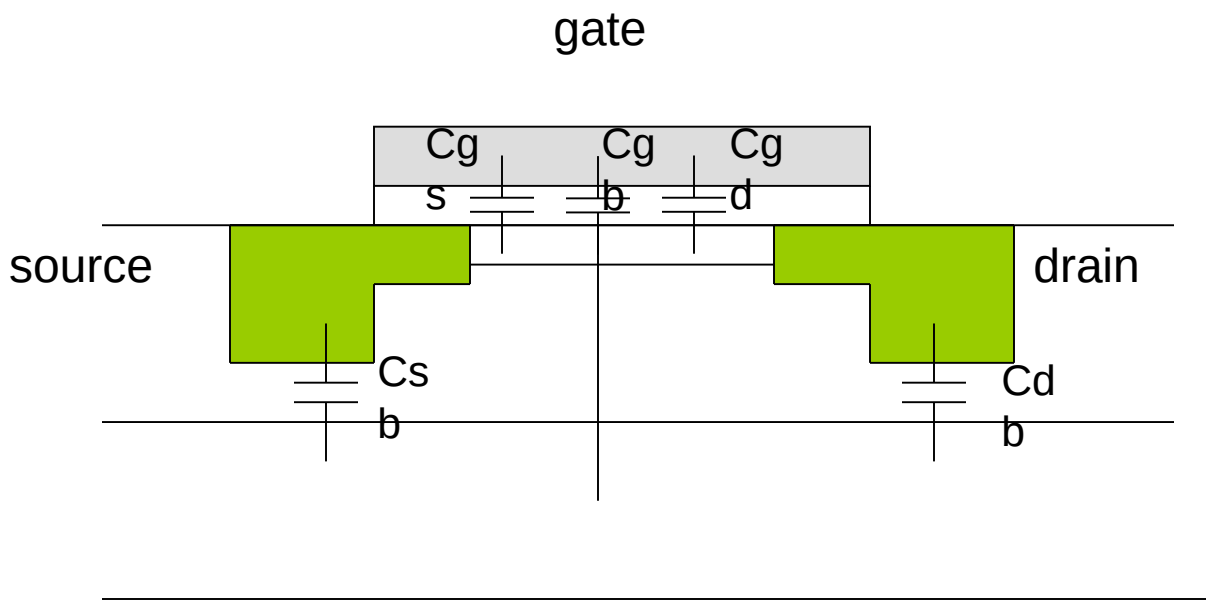
Agenda

- Parasitics in Circuit Design
- Where do parasitics come from?
- Parasitics Estimation
- Scaling of parasitics for simulations

What Parasitics are Contained in a Circuit?

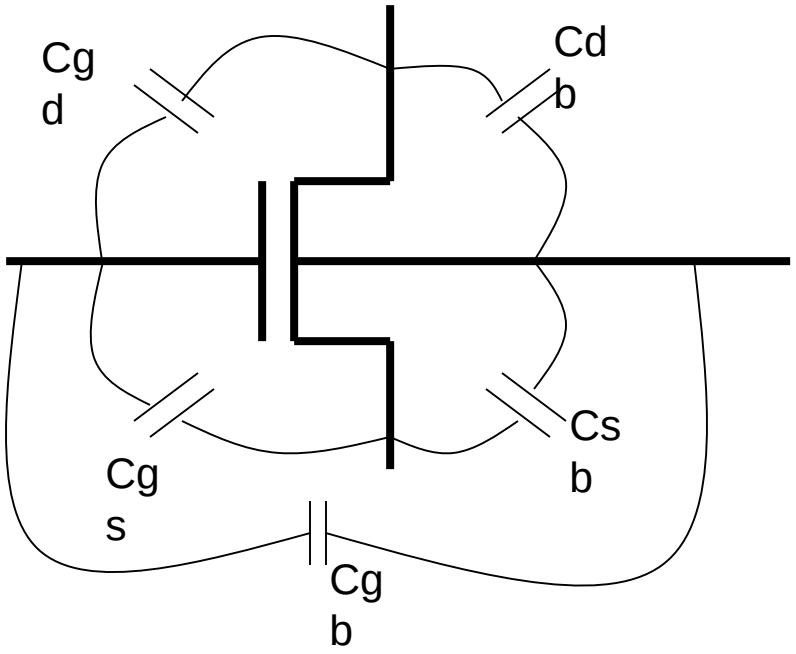
- Transistor related parasitics:
  - Gate Capacitance
  - Diffusion Capacitance
- Interconnect related parasitics:
  - Interconnect Resistance and Capacitance
  - Cross Capacitance (xcap)

Transistor Parasitics



- Cgs, Cgd are gate-to-channel capacitances
- Cgb is gate-to-bulk capacitance
- Csb, Cdb are source/drain diffusion capacitances

Transistor Parasitics



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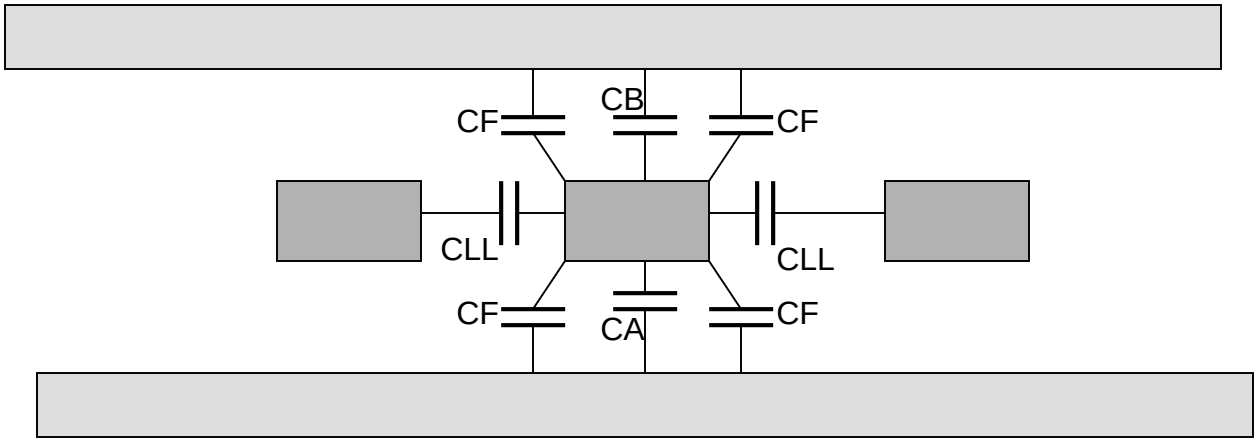
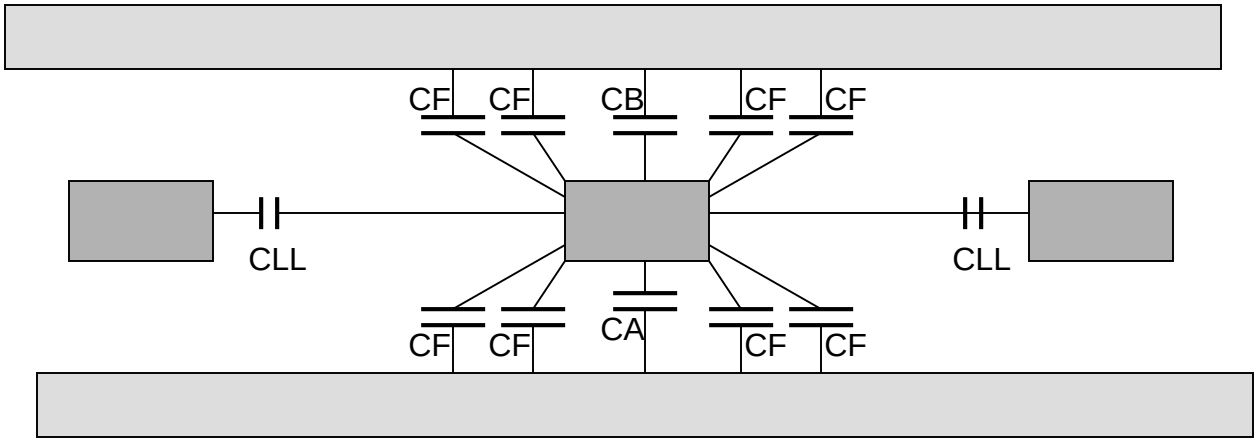
Interconnect Parasitics



- CLL – Line to line Capacitance
- CA,CB – Capacitance to other plane
- CF – Fringing Capacitance

Interconnect Parasitics



- Adding additional spacing will decrease the value of the CLL, but may cause additional fringing capacitance.

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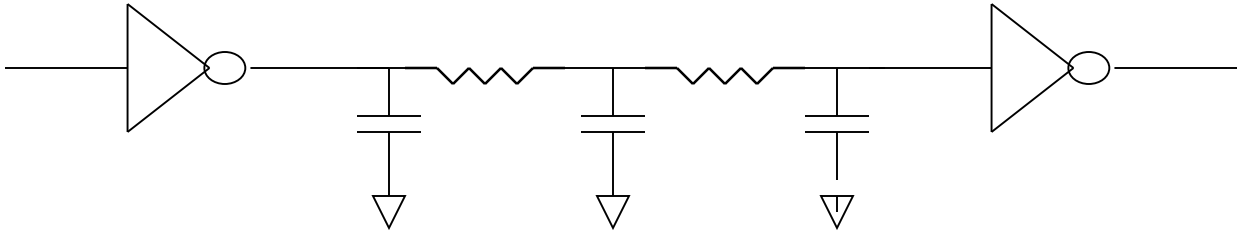
Where do Parasitics Come From

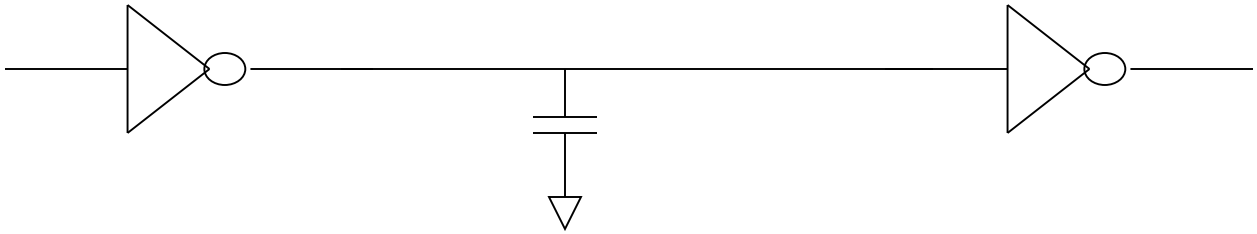
- Extraction
  - Different types of extraction tools will use the layout to produce values for device and interconnect parastics.
- Estimation
  - For designs that do not have layout, there are various ways of estimating parasitics.

Lumped or Distributed?

- Distributed Interconnect Parasitics contain Rs and Cs

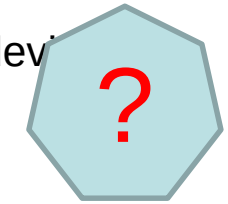


- Lumped Interconnect Parasitics contain only Cs.



Common Parasitics File Types

- Nets
  - Distributed interconnect parasitics, resistance and capacitance
  - Comes from extraction tool, and can be named for that tool (e.g. mntcl, stntcl, antcl …)
- Device parasitics
  - Device parasitics, specified in terms of area and perimeter of the devi
  - Also named for the extraction tool (mdpf, adpf, stdpf, …)
- .xcab
  - Cross capacitance list
  - Lists all “attackers” for each net that is a “victim”
  - Can be generated from the nets file
- .RC
  - Lumped interconnect parasitics, capacitance only
  - Can be generated from the nets file, or estimated.
- Stitched interface
  - Stitched interface and stitched netcell files.
  - Generated from the .ntcl file
- Distributed interconnect
  - Distributed interconnect parasitics, resistance and capacitance, used by timing tool



NET File

```
$NETCELL OF NODE FAEXCMPD/FAEXCMMASTERS1D/FAEXCMMASTER1_0[1]/I36/I121/NET504 OF CELL FAALGCM
.MACRO FAEXCMMASTER1_0[1]/I36/I121/NET504
+ FAEXCMPD/FAEXCMMASTERS1D/FAEXCMMASTER1_0[1]/I36/I121/MP119%S.X10335Y17120_8
+ FAEXCMPD/FAEXCMMASTERS1D/FAEXCMMASTER1_0[1]/I36/I121/MP119%S.X10515Y17678_8
+ FAEXCMPD/FAEXCMMASTERS1D/FAEXCMMASTER1_0[1]/I36/I121/MP119%S.X10775Y17123_8
...
+ X__{FAALGCM}%FAEXCMPD/FAEXCMMASTER00D/FAEXPCMMASTER2_1[0]/I39/N15
+ X__{FAALGCM}%OTH_MIRSLDS2DATA0RGTC32H[69]
+ X__{FAALGCM}%MIRSLDS1DATA1RGTC32H#[56]
R0X5_A1 N28.X10385Y17570_4 N108.X10385Y17570_8 45.44
R0X75_A1 N80.X10825Y16690_4 N112.X10825Y16690_8 45.44
R0X11_A1 N32.X10370Y16645_4 N40.X10385Y16690_4 0.118409
R0X81_A1 N84.X10825Y17570_8 N120.X10825Y16910_8 0.001
R0X1D_A1 N36.X10385Y16910_4 N40.X10385Y16690_4 0.578889
...
C0X20 N32.X10370Y16645_4 VSS 7.43475E-18
C0X30 N48.X10810Y16645_4 VSS 7.00309E-17
C0X1C N28.X10385Y17570_4 VSS 3.21045E-17
C0X34 N52.X11460Y16765_4 VSS 1.54241E-16
C153 N28.X10385Y17570_4 X__{FAALGCM}%FAEXCMPD/FAEXCMMASTER00D/FEXPCMASTER2_1[0]/I39/N15 1.29694E-19
C154 N28.X10385Y17570_4 X__{FAALGCM}%OTH_MIRSLDS2DATA0RGTC32H[69] 1.86296E-19
...
C193 N32.X10370Y16645_4 X__{FAALGCM}%MIRSLDS1DATA1RGTC32H#[56] 2.76394E-19
C194 N48.X10810Y16645_4 X__{FAALGCM}%MIRSLDS1DATA1RGTC32H#[56] 2.32498E-18
$$_AM A1 stntcl
$$_AM CIC 8.022247483e-16
.EOM
```

Node Name

Pins

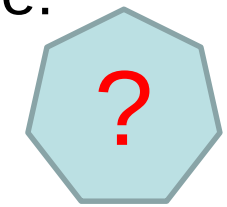
Resistors

Capacitors

End of this Node

DPF File

- Lists all devices in the design
- Lists all four nodes connected to the device: drain,gate,source,bulk
- Gives values for device length and width
- Gives values for area/perimeter of drain and source



- Example:

```
@/i7/mp49 p vcc vcc (model=p_i z=0.85 l=0.04 ps=1.13 as=0.119 ad=0.119 pd=1.13
    cjs=6.57664e-16 cgate=7.244e-16 cjd=6.57664e-16
```

RCD File

- Lists of all node in the design
- Has values for total cap, gate cap, interconnect cap, and cross cap.
- Interconnect cap can come from lumping of .ntcl file capacitances, or from estimation.

XTAB File

- Lists each attacker of each node in the design.
- Comes adding the xcap from the .ntcl file

- Example:

```
BEGIN_ENTRY /NET510
ATTR XCAP
{FMEXPD}%N2  3.88583e-06
{FMEXPD}%N8  7.14513e-06
END_ATTR
END_ENTRY
```

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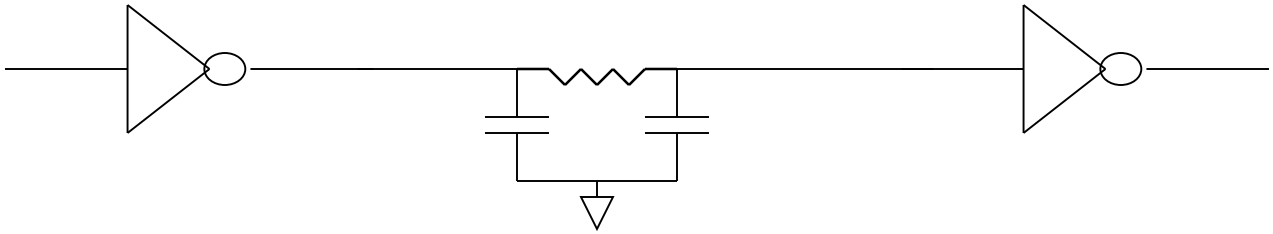
What is Parest?

- When no layout is available for extraction, we must use some tool to estimate the parasitics.
- Estimation can be done for both dynamic and static simulations.
- Estimating devices parasitics is pretty accurate.
  - Size of devices is contained in the schematic.
- Estimating interconnect parasitics is very inaccurate.
  - Length/width/metal_layer of net is not in the schematic

What is an FTRC, and how is it used?

- FTRC (File Tracking Resistor and Capacitors) is a schematic element used to describe the metal interconnect.
- Values are provided by the user for:
  - Length
  - Width
  - MCF
  - Spacing
  - Model (Includes routed metal layer, above metal layer, and below metal layer. For example, rm3m2m4)
- FTC and FTR elements are also available.
- Information stored in the process file is used to determine the value of the Rs and Cs.
- Used for simulation schematics only, not production schematics



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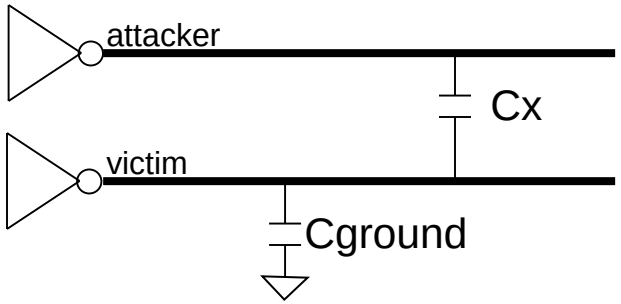
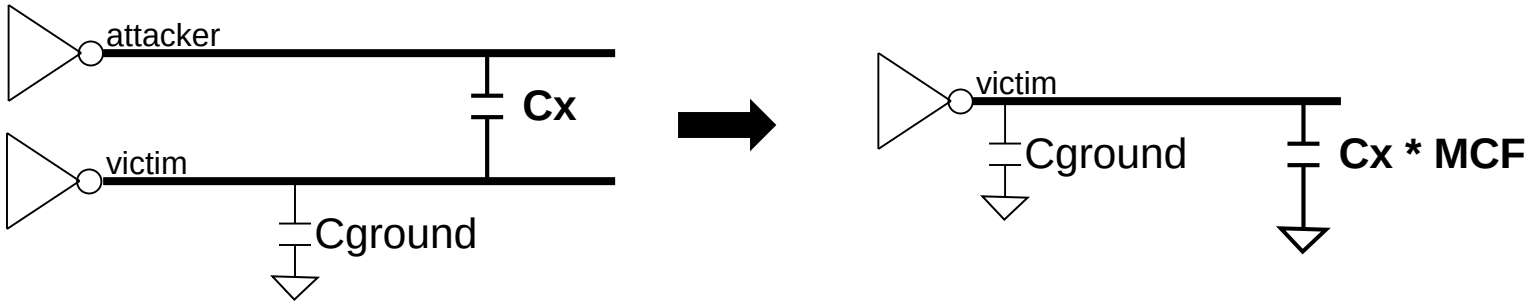
What is MCF



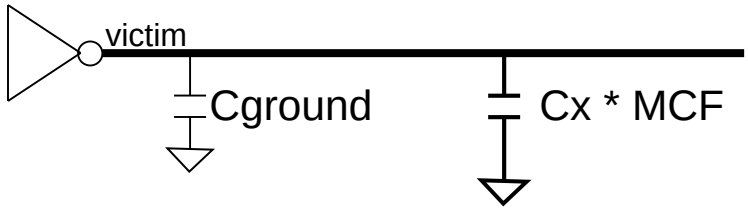
- In the figure above, the time it takes for the “victim” signal to switch can depend on the “attacker” signal.
- The attacker signal can speed up the victim signal if it is switching at the same time and in the same direction as the victim.
- The attacker signal can slow down the victim signal if it is switching at the same time and in the opposite direction as the victim.
- We can model this speed-up or slow-down of the victim timing by increasing or decreasing the value of the Capacitance on that net.
- We will multiply the Cx capacitor by some “MCF” value. (from 0 – 2).

What is MCF



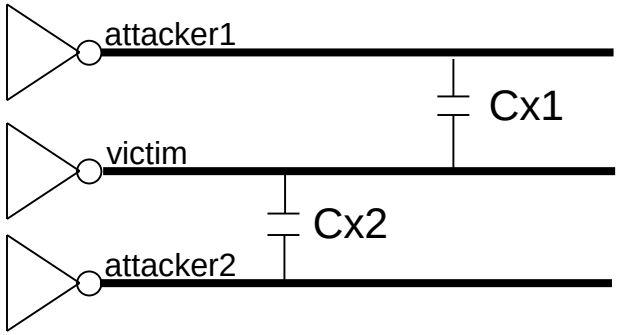
- MCF is a dynamic property, but can be modeled by static timing tools.
- The cross-capacitor is de-coupled from the attacker and the value is multiplied by the “MCF” factor.
- If the attacker is slowing down the victim, an MCF value of 2.0 is applied. If the attacker is speeding up the victim, an MCF value of 0.0 is applied.

What is MCF



- For Tejas MCF values of 2.0/0.0 (max/min) were applied to all cross-capacitances for signals from the same bus, as they had a high chance of switching at the same time as each other.
- For other signals a backoff of the 2.0/0.0 values was given, and MCF values of 1.5/0.5 were applied.
- Note – Capacitances to ground were unaffected ("Cground" in the figure above)
- Yonah/Merom do not use this methodology.
- Each Project must decide what to do about MCF modeling.

What is “Average MCF” ?



- A victim is typically attacked by more than one other net.
- If the MCF between the “victim” and “attacker1” is 2 and the MCF between “victim” and “attacker2” is 1, we could say that the Average MCF of the victim is 1.5.
- We DO NOT use the Average MCF number in any post-layout flow.

How are Parasitics Scaled for Timing Runs?

- Static Timing:
  - Parasitics are extracted at a "typical" corner but values on the actual chips may be slightly different.
  - Because timing runs both a max and min run, we have the option of scaling our "typical" parasitics to make each runs "worst-case".
  - For projectx:
    - In the Max run, all resistances were scaled by 1.15.
    - In the Min run, capacitances were scaled by 0.80
  - For projecty:
    - No resistances were scaled
    - In the Min run, capacitance were scaled by 0.80
- Dynamic Timing:
  - FTRC devices will scale as different process corners are used. Selecting a particular corner will determine if your interconnect is modeled as "fast", "slow", or "typical".