DEPARTMENT OF COMPUTER SYSTEM ENGINEERING

Digital Integrated Circuits - ENCS333

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Lecture #13

Power dissipations

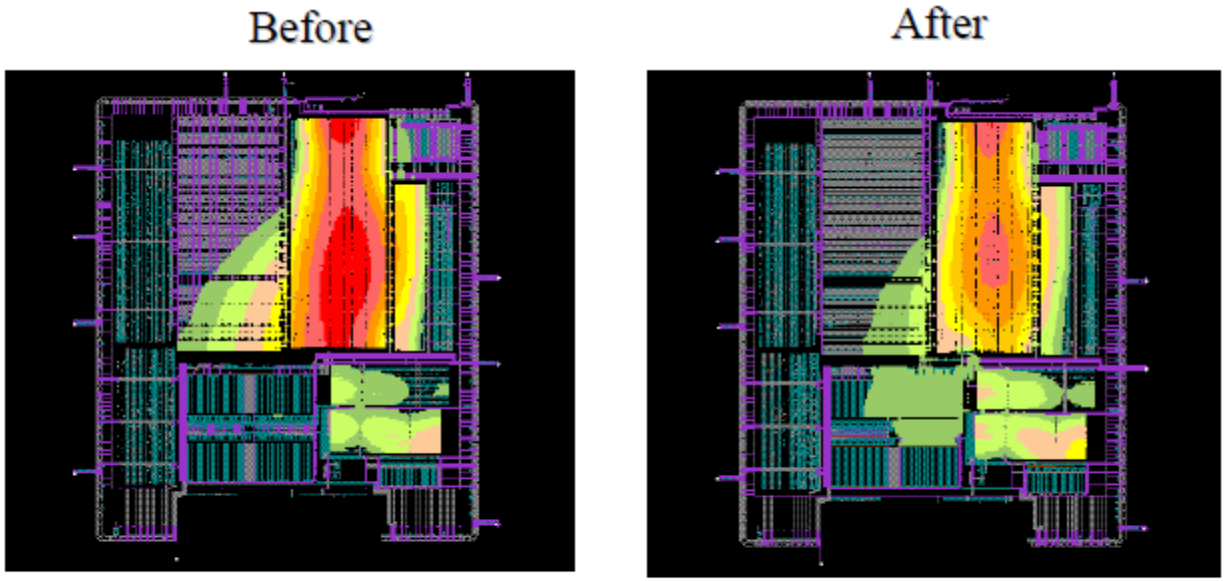
Digital Integrated Circuits

	Course topics and Schedule
	Subject
1	Introduction to Digital Integrated Circuits Design
2	Semiconductor material: pn-junction, NMOS, PMOS
3	IC Manufacturing and Design Metrics CMOS
4	Transistor Devices and Logic Design The CMOS inverter
5	Combinational logic structures
6	Layout of an Inverter and basic gates
7 8	Static CMOS Logic Dynamic Logic
9	Sequential logic gates; Latches and Flip-Flops
10	Summary : Device modeling parameterization from I-V curves.
11	Interconnect: R, L and C - Wire modeling
12	Parasitic Capacitance Estimation
13	Timing
14	Power dissipation;
15	Clock Distribution
16	SPICE Simulation Techniques (Project)
17	Arithmetic building blocks
18	Memories and array structures
19	Voltage, package, protection
20	Reliability and IC qualification process
21	Advanced Voltage Scaling Techniques
22	Power Reduction Through Switching Activity Reduction
23	CAD tools and algorithms
24	SPICE Simulation Techniques (Project)

Impact of Resistance on IC

- We have already learned how to drive RC
- interconnect Impact of resistance is commonly seen in power supply distribution:
  - IR drop
  - Voltage variations
- Power supply is distributed to minimize the IR drop and the change in current due to switching of gates

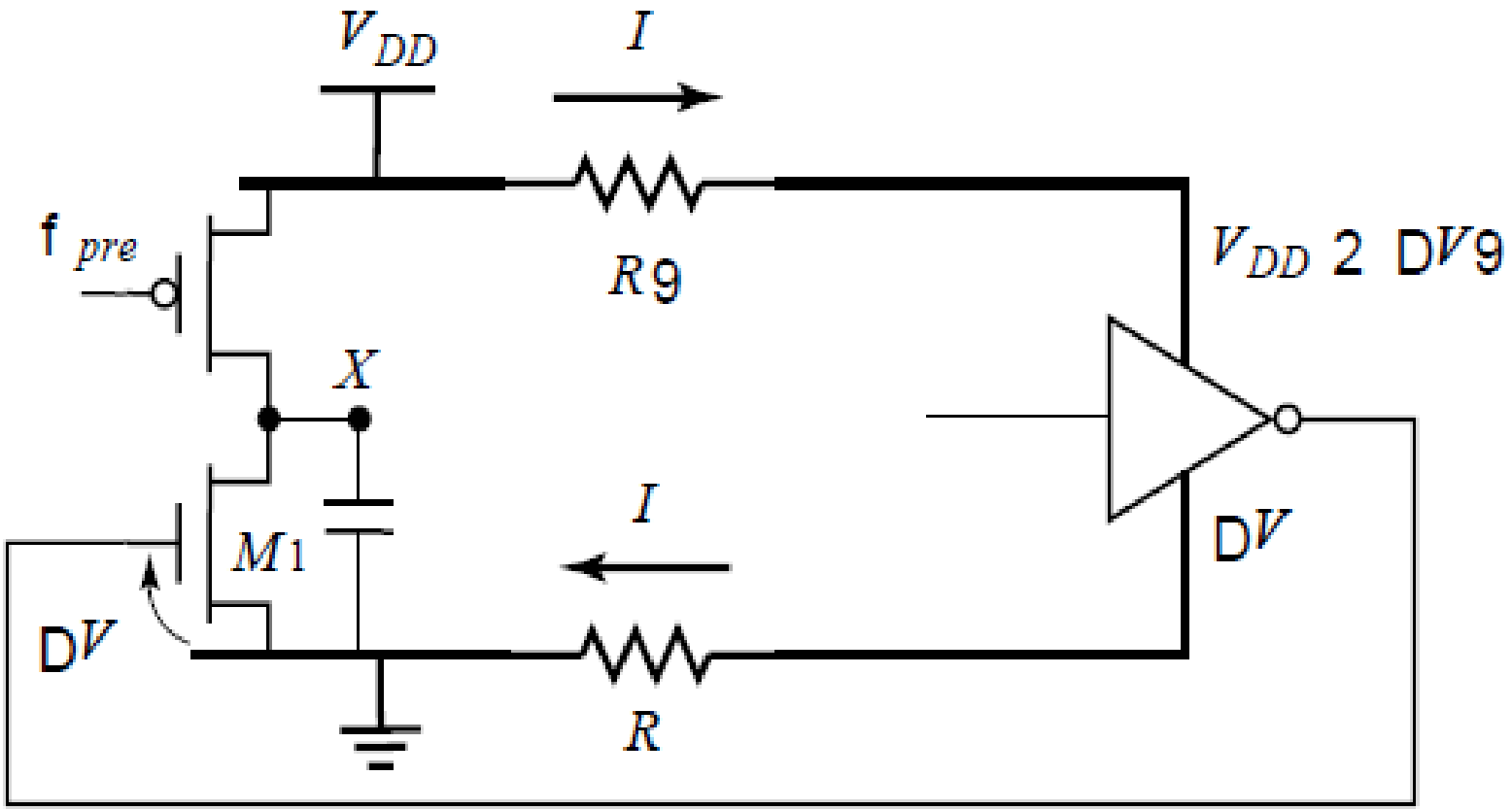
Resistance and the Power Distribution Problem



- Requires fast and accurate peak current prediction
- Heavily influenced by packaging technology

https://www.apache-da.com/products/redhawk

RI Introduced Noise



Power Distribution

- Low-level distribution is in Metal 1
- Power has to be ‘strapped’ in higher layers of metal.
- The spacing is set by IR drop, electromigration, inductive effects
- Always use multiple contacts on straps

Where Does Power Go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

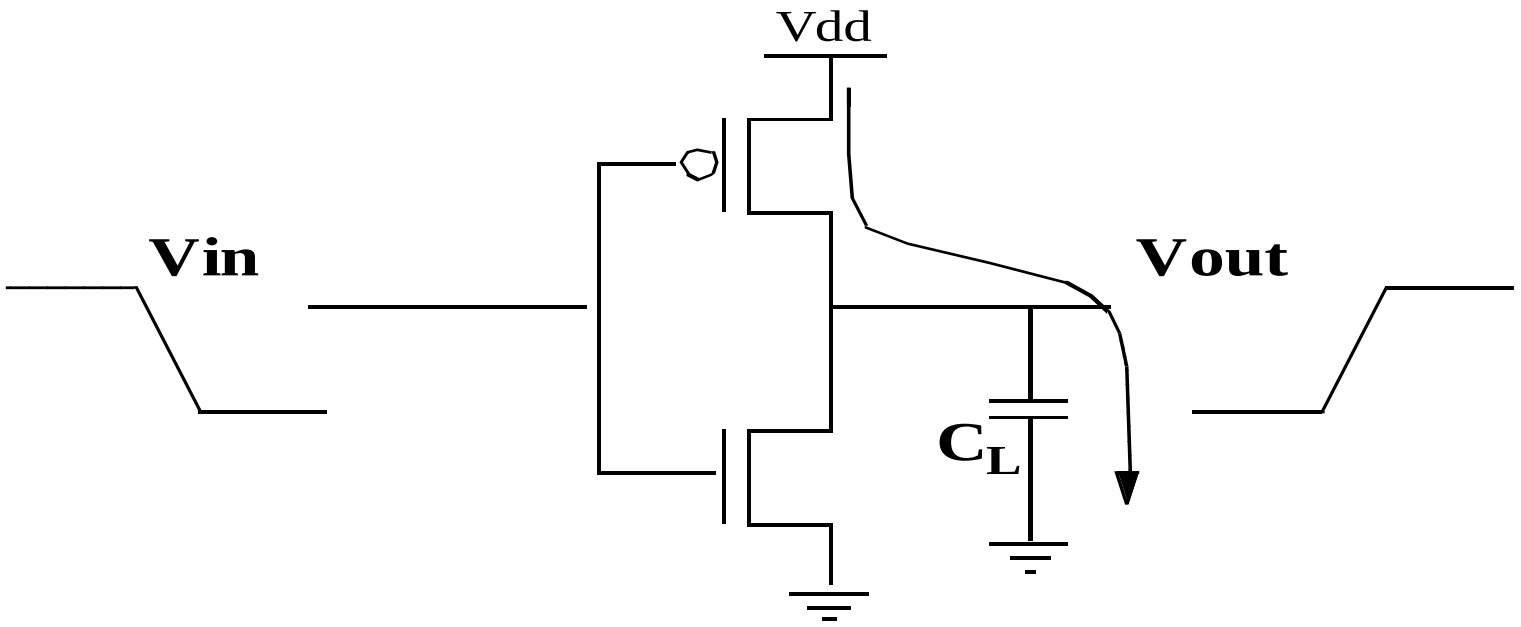
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Dynamic Power Consumption



$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- Not a function of transistor sizes!
- Need to reduce C_L, V_{dd}, and f to reduce power.

Dynamic Power Consumption - Revisited

Power = Energy/transition * transition rate

$$= C_L * V_{dd}^2 * f_{0\rightarrow 1}$$

$$= C_L * V_{dd}^2 * P_{0\rightarrow 1} * f$$

$$= C_{EFF} * V_{dd}^2 * f$$

Power Dissipation is Data Dependent
Function of *Switching Activity*

C_{EFF} = **Effective Capacitance** = $C_L * P_{0\rightarrow 1}$

$P_{0\rightarrow 1} = P_0 \cdot P_1$

Factors Affecting Transition Activity

- "Static" component (does not account for timing)
  - Type of Logic Function (NOR vs. XOR)
  - Type of Logic Style (Static vs. Dynamic)
  - Signal Statistics
  - Inter-signal Correlations
- "Dynamic" or timing dependent component
  - Circuit Topology
  - Signal Statistics and Correlations

Type of Logic Function: NOR vs. XOR

Example: Static 2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities

$p_{A=1} = 1/2$

$p_{B=1} = 1/2$

Then transition probability

$p_{0\to1} = p_{Out=0} \times p_{Out=1}$

$= 3/4 \times 1/4 = 3/16$

If inputs switch every cycle

$\alpha_{0\to1} = 3/16$

Type of Logic Function: NOR vs. XOR

Example: Static 2-input XOR Gate

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

Assume signal probabilities

$p_{A=1} = 1/2$

$p_{B=1} = 1/2$

Then transition probability

$p_{0\to1} = p_{Out=0} \times p_{Out=1}$

$= 1/2 \times 1/2 = 1/4$

If inputs switch in every cycle

$\alpha_{0\to1} = 1/4$

Power Consumption is Data Dependent

Example: Static 2 Input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of 2 input NOR gate

Assume:

P(A=1) = 1/2

P(B=1) = 1/2

Then:

P(Out=1) = 1/4

$P_{0\rightarrow1} = P_0.P_1$

P(0$\rightarrow$1)

= P(Out=0).P(Out=1)

= 3/4 $\times$ 1/4 = 3/16

$$C_{EFF} = 3/16 * C_L$$

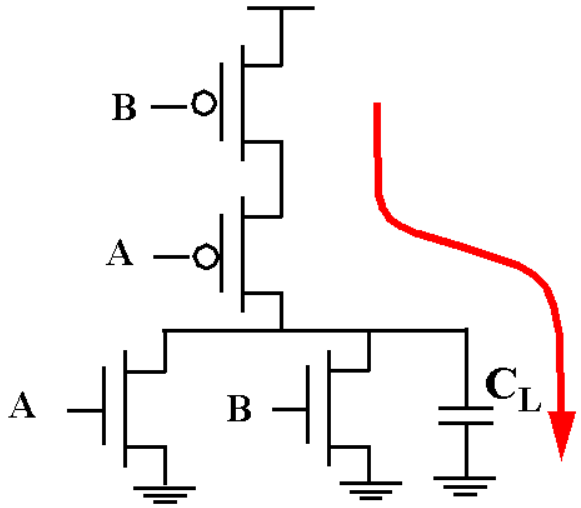
Transition Probabilities for Basic Gates

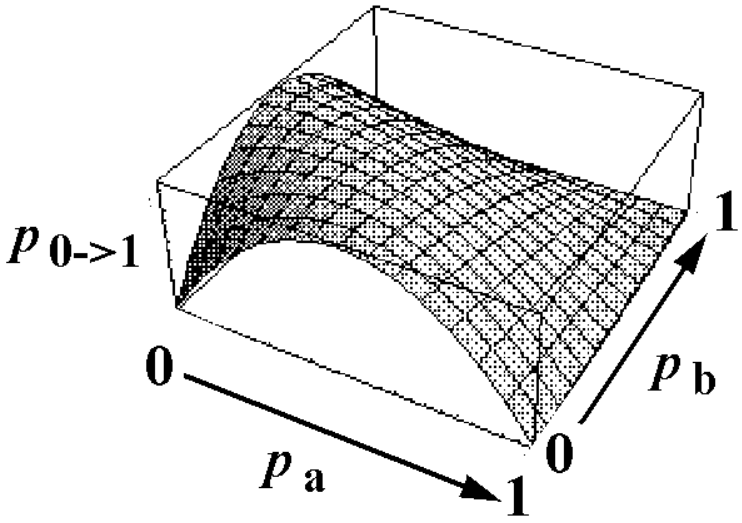
	$P_{0\rightarrow1}$
AND	$(1-P_AP_B)P_AP_B$
OR	$(1-P_A)(1-P_B)(1-(1-P_A)(1-P_B))$
EXOR	$(1 - (P_A + P_B - 2P_AP_B))(P_A + P_B - 2P_AP_B)$

Switching Activity for Static CMOS

$$\mathbf{P_{0\rightarrow1} = P_0 . P_1}$$

Transition Probability of 2-input NOR Gate



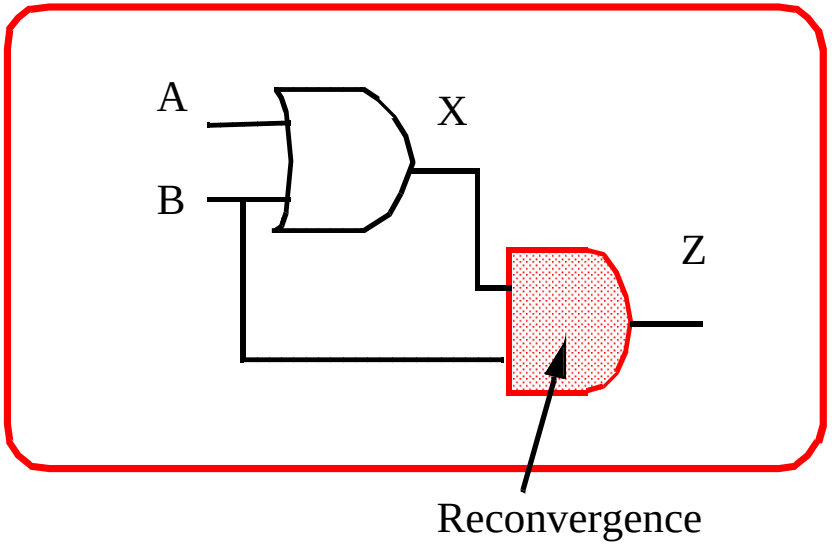


$$p_1 = (1-p_a)\,(1-p_b)$$

$$p_{0->1} = p_0\, p_1 = (1-(1-p_a)\,(1-p_b))\,(1-p_a)\,(1-p_b)$$

- $\alpha_{0->1}$ **is a strong function of signal statistics**

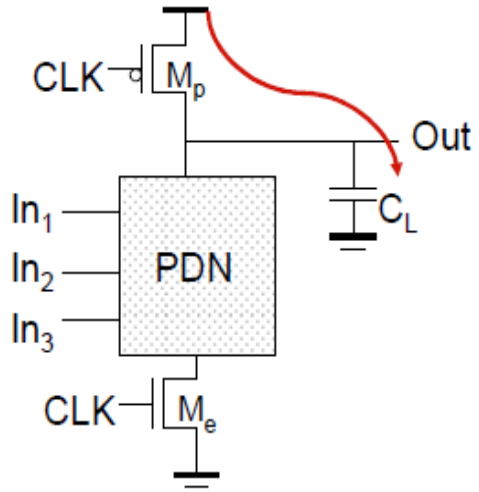
Problem: Reconvergent Fanout



P(Z=1) = P(B=1) . P(X=1 | B=1)

Becomes complex and intractable real fast

How about Dynamic Circuits?



Power only dissipated when previous Out = 0

Dynamic Power Consumption is Data Dependent

Dynamic 2-input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Assume signal probabilities

$P_{A=1} = 1/2$

$P_{B=1} = 1/2$

Then transition probability

$P_{0\rightarrow1} = P_{out=0} \times P_{out=1}$

$= 3/4 \times 1 = 3/4$

Switching activity always higher in dynamic gates!

$P_{0\rightarrow1} = P_{out=0}$

Power is Only Dissipated when Out=0!

$$C_{EFF} = P(Out=0).C_L$$

4-input NAND Gate

Example: Dynamic 2 Input NOR Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of 2 input NOR gate

Assume:

P(A=1) = 1/2

P(B=1) = 1/2

Then:

P(Out=0) = 3/4

$$C_{EFF} = 3/4 * C_L$$

Switching Activity Is Always Higher in Dynamic Circuits

Transition Probabilities for Dynamic Gates

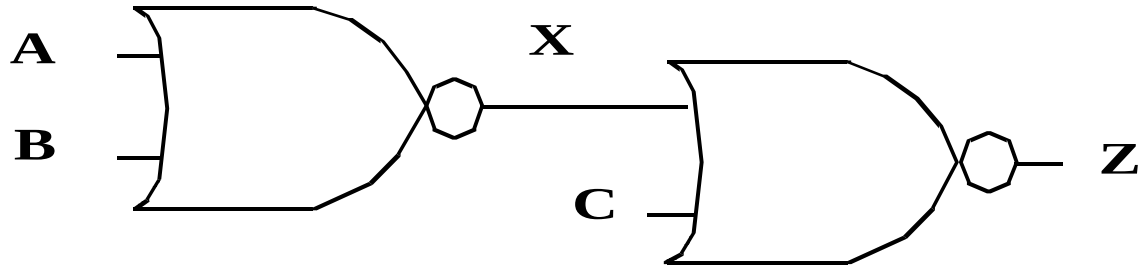
	$P_{0\rightarrow1}$
AND	$(1-P_AP_B)$
OR	$(1-P_A)(1-P_B)$
EXOR	$(1 - (P_A + P_B - 2P_AP_B))$

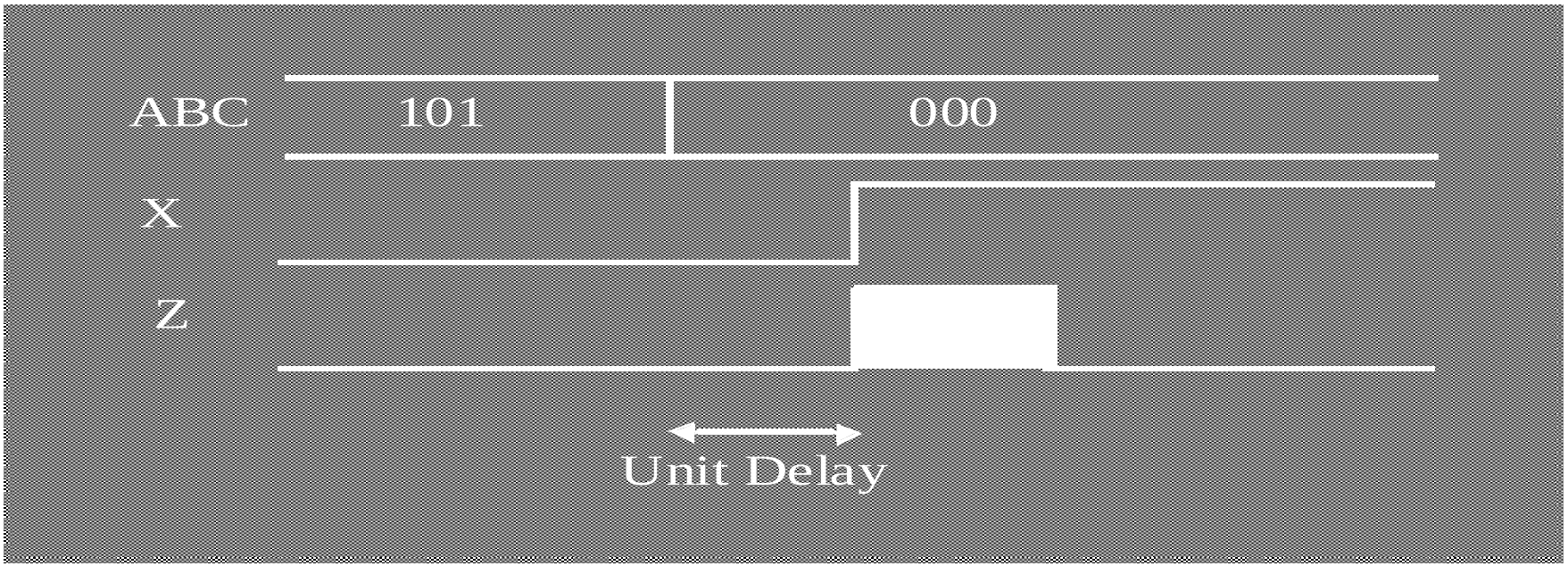
Switching Activity for Precharged Dynamic Gates

$$\mathbf{P_{0\rightarrow1} = P_0}$$

Glitching in Static CMOS

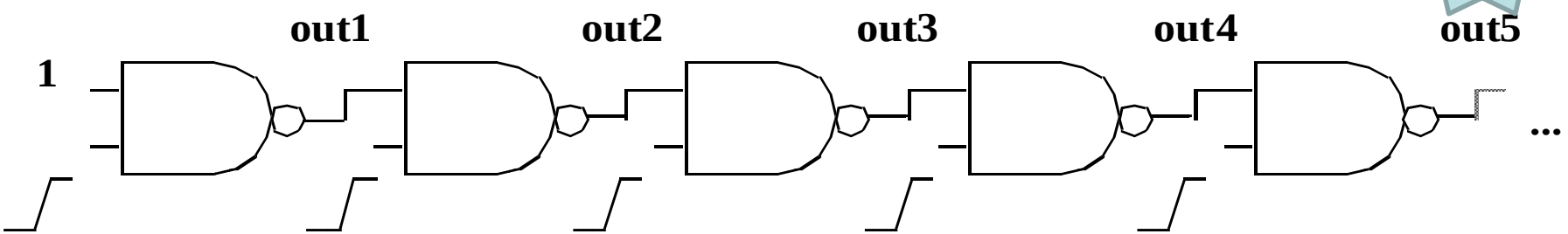
also called: dynamic hazards

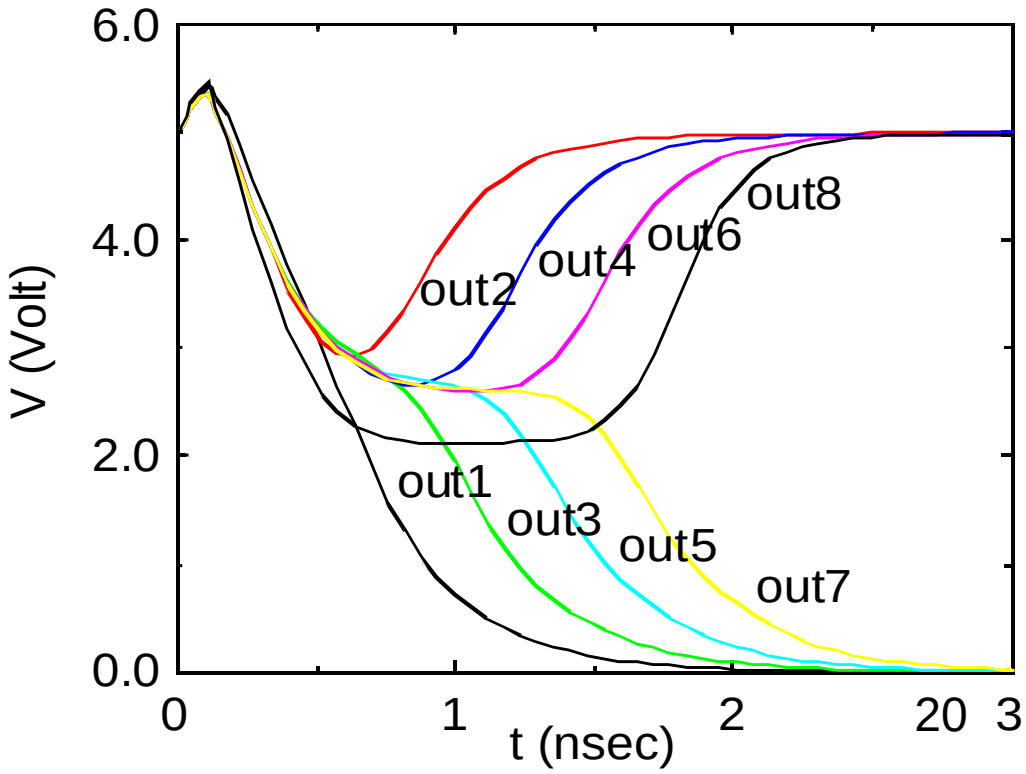




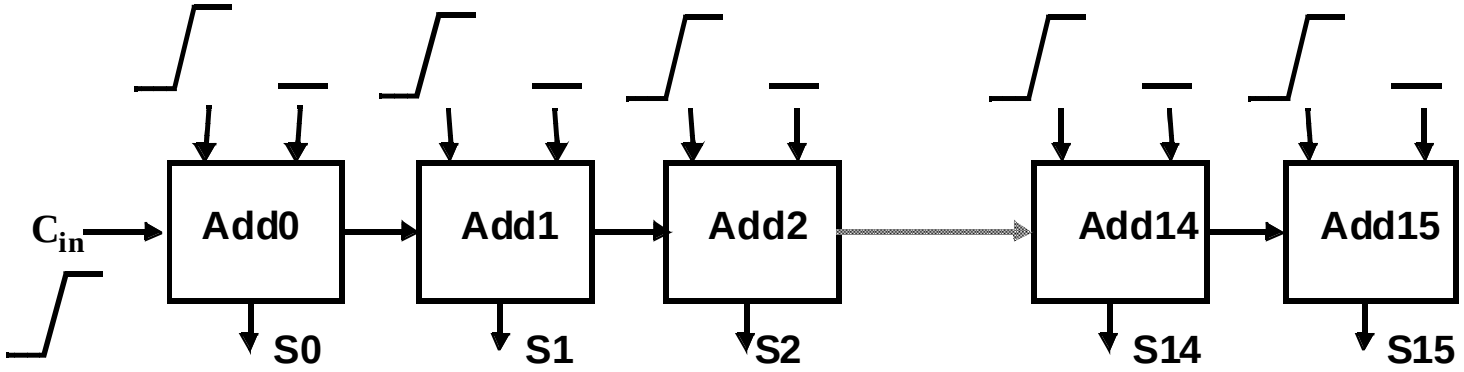
Observe: No glitching in dynamic circuits

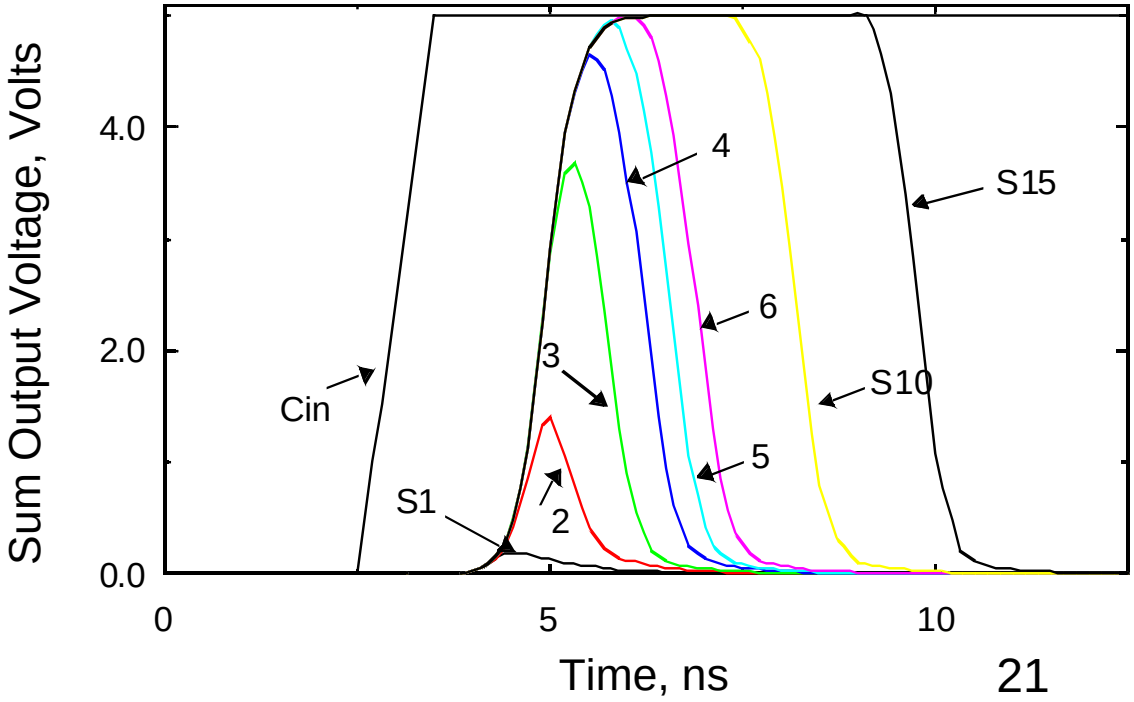
Example 1: Chain of NOR Gates



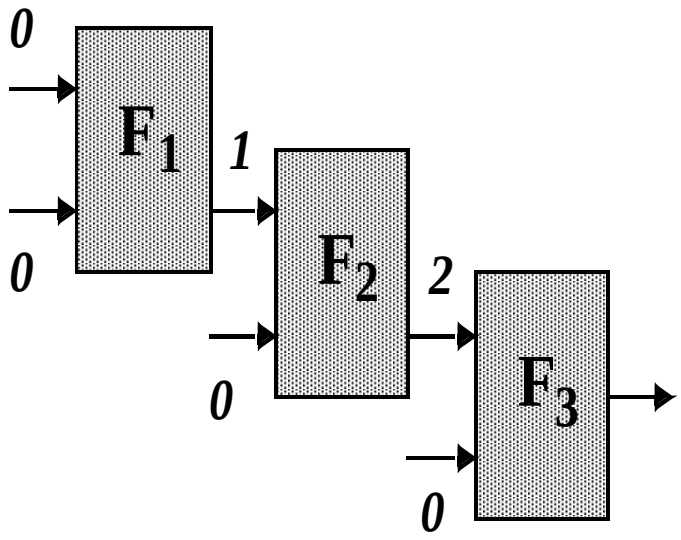


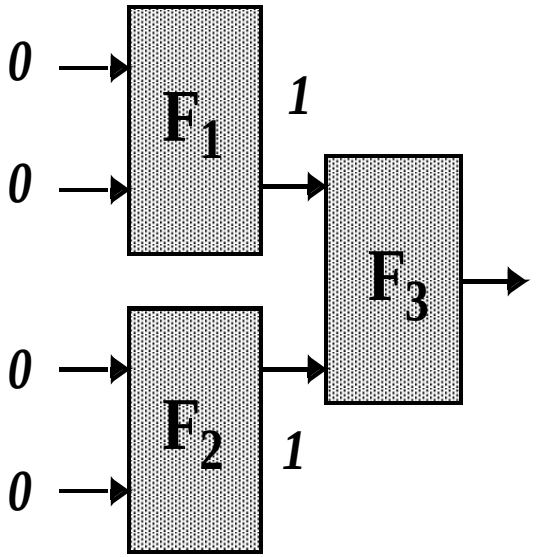
Example 2: Adder Circuit





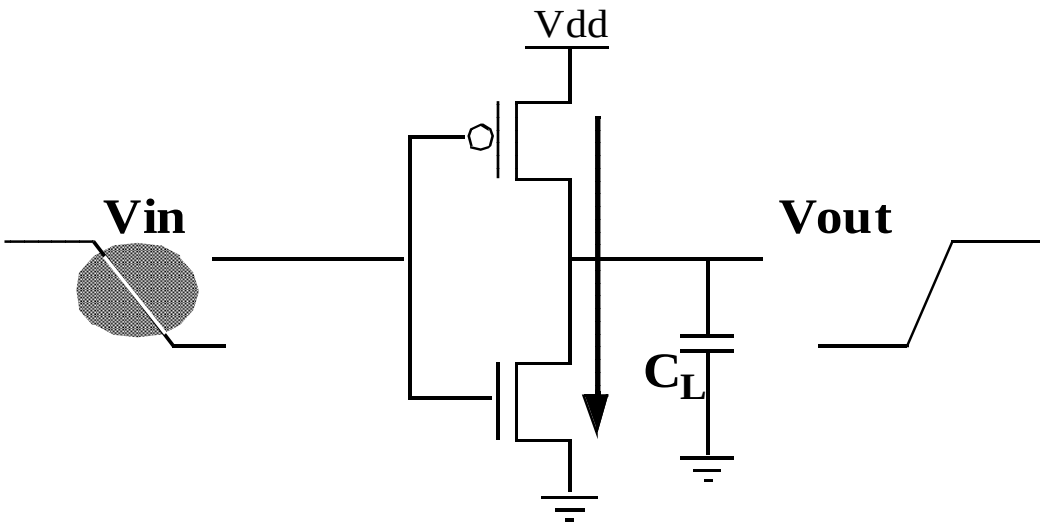
How to Cope with Glitching?

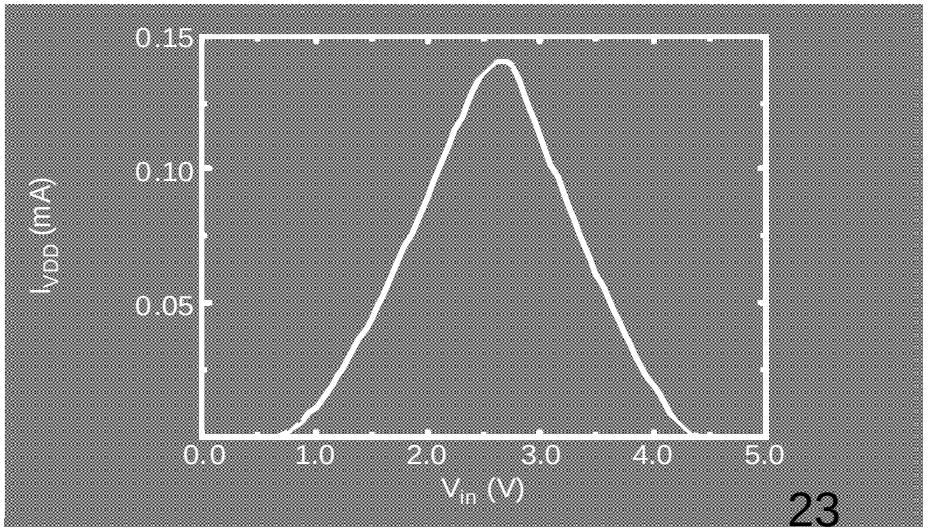




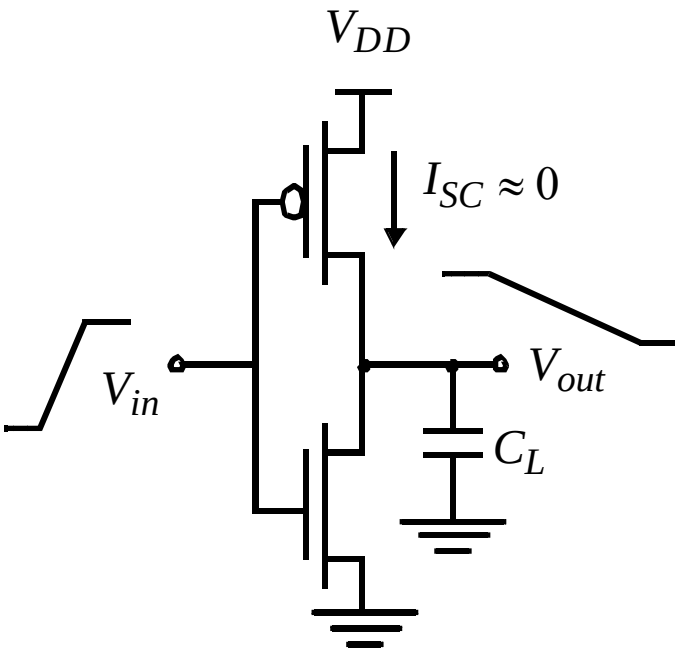
Equalize Lengths of Timing Paths Through Design

Short Circuit Currents

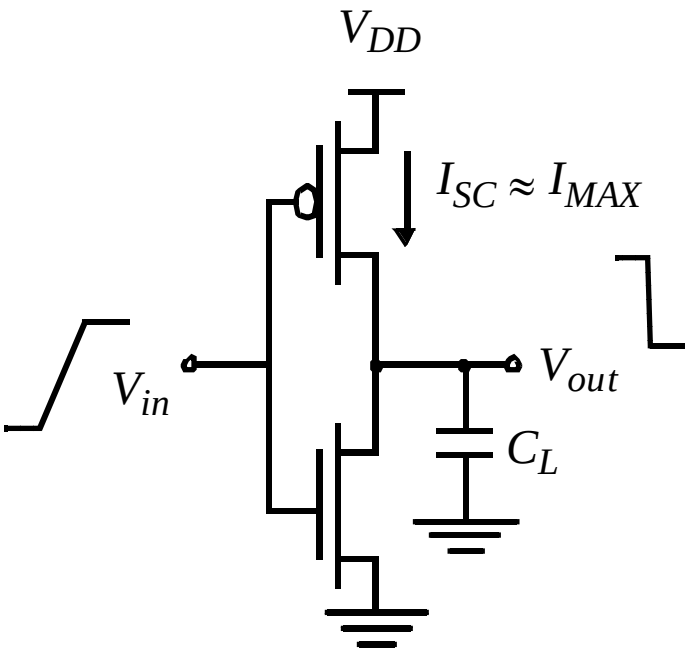




Impact of rise/fall times on short-circuit currents

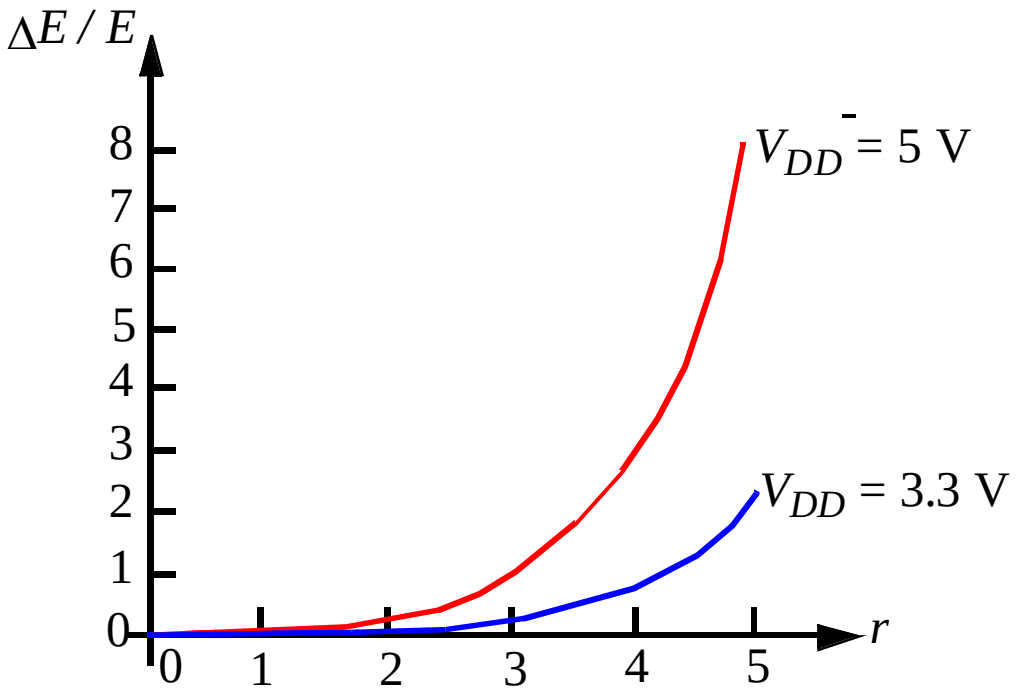


Large capacitive load



Small capacitive load

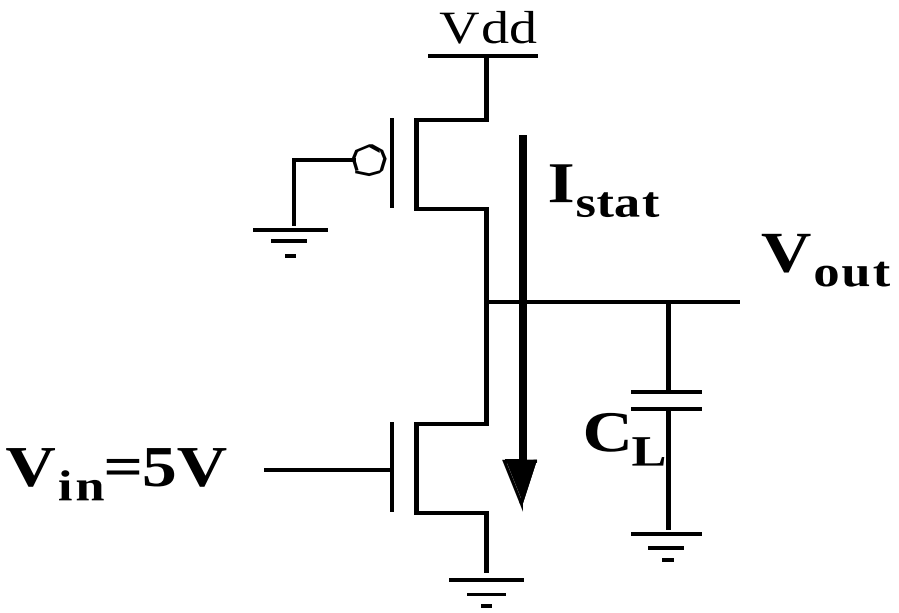
Short-circuit energy as a function of slope ratio



$W/L|_P = 7.2\mu m/1.2\mu m$
$W/L|_N = 2.4\mu m/1.2\mu m$

The power dissipation due to short circuit currents is minimized by matching the rise/fall times of the input and output signals.

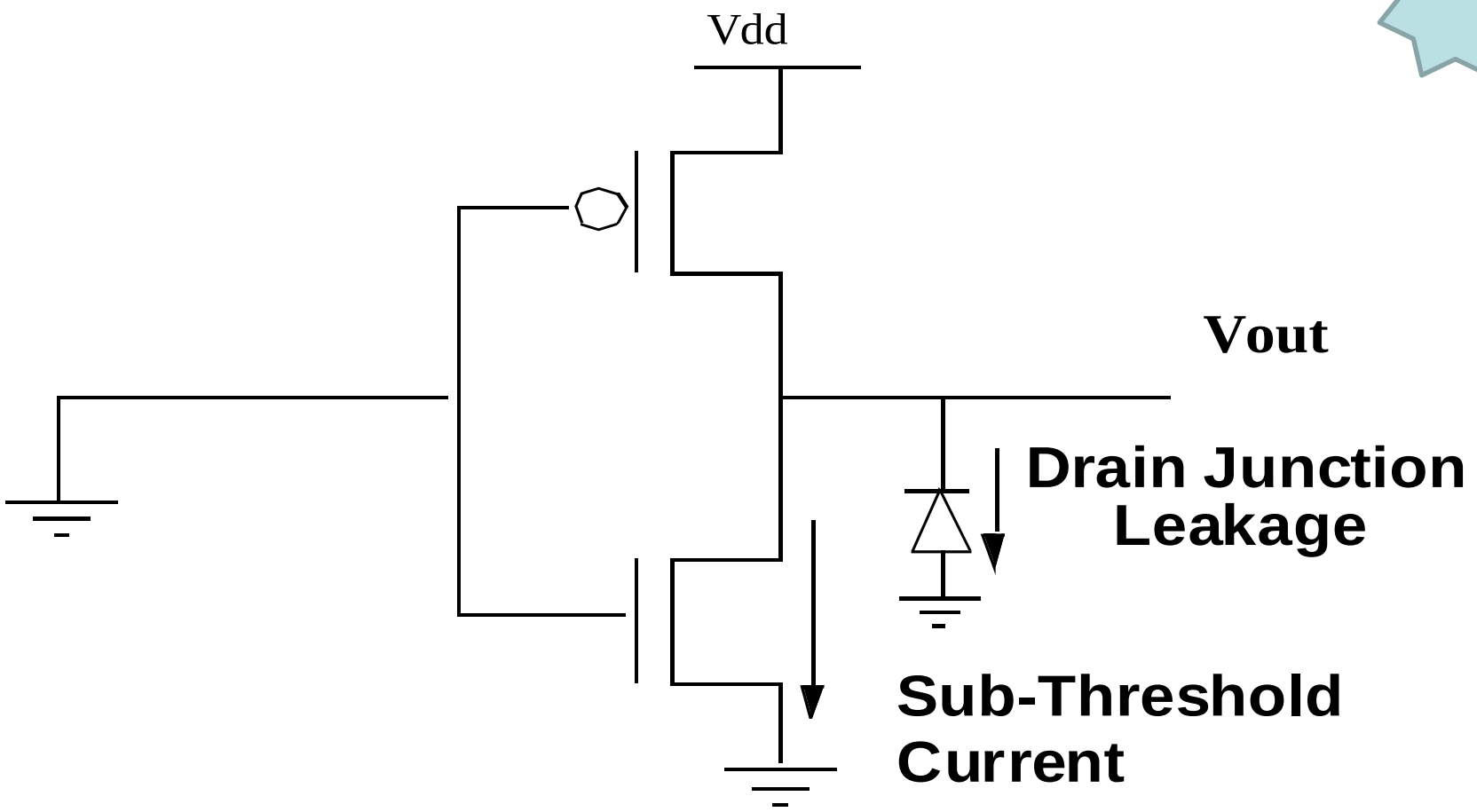
Static Power Consumption



$$P_{stat} = P_{(In=1)} \cdot V_{dd} \cdot I_{stat}$$

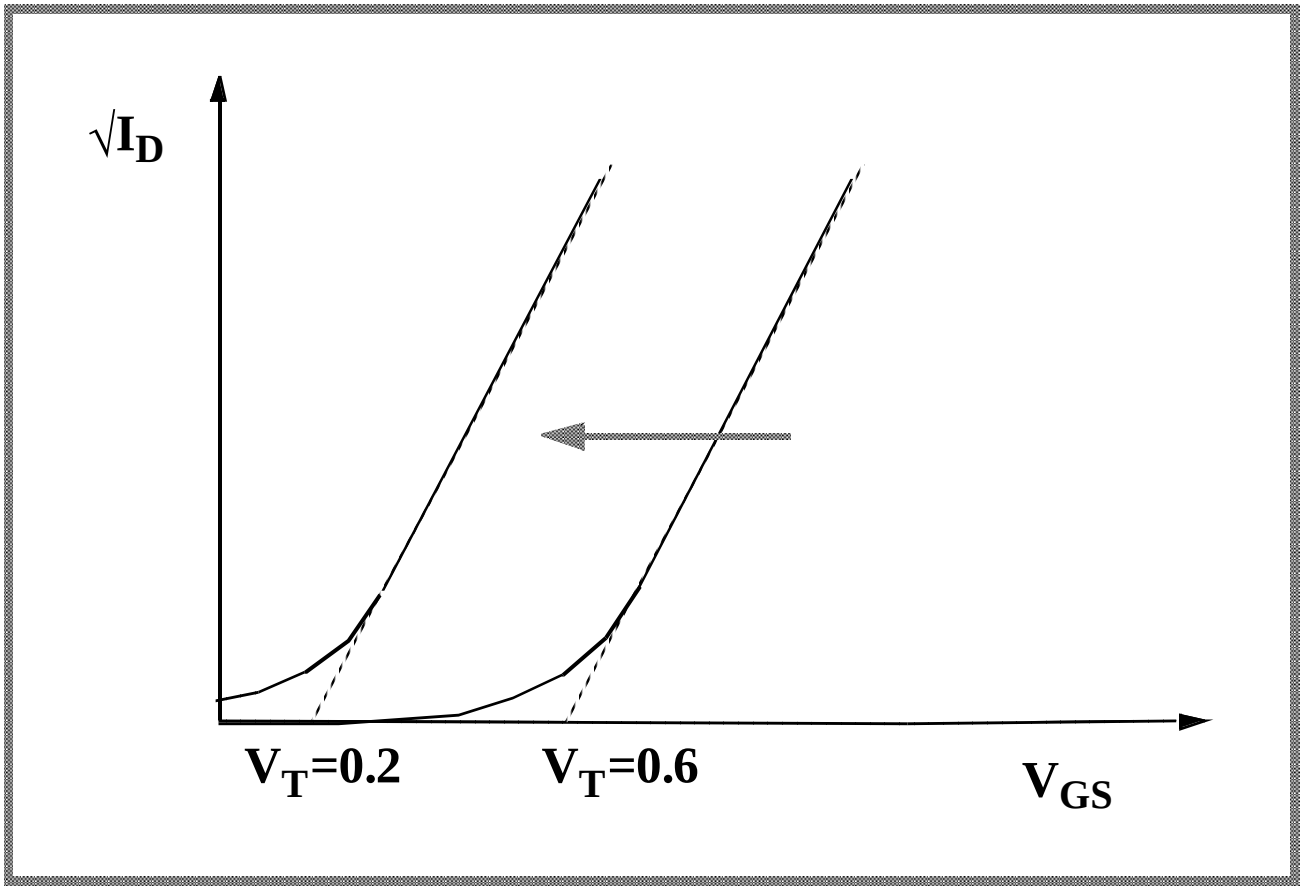
- **Dominates over dynamic consumption**
- **Not a function of switching frequency**

Leakage



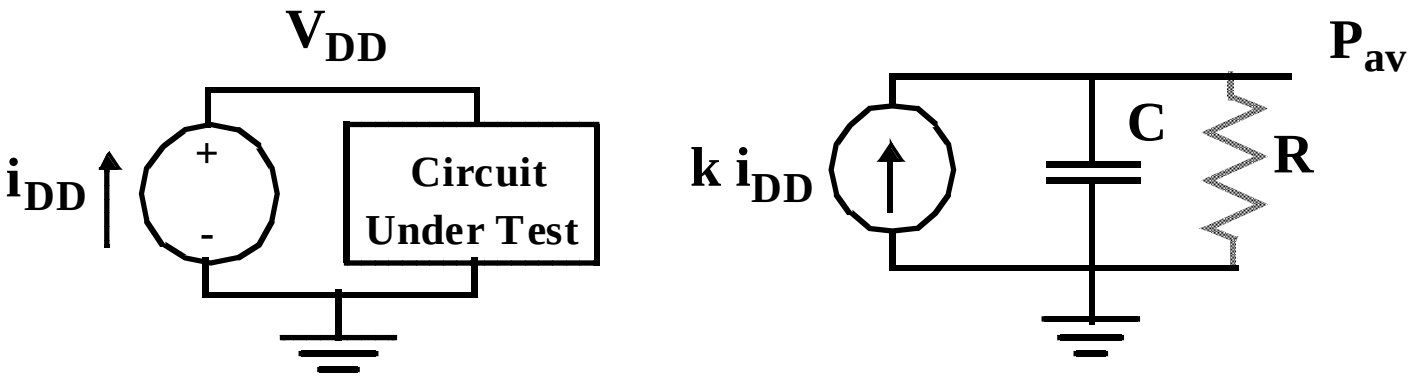
Sub-Threshold Current Dominant Factor

Sub-Threshold in MOS



Lower Bound on Threshold to Prevent Leakage

Power Analysis in SPICE



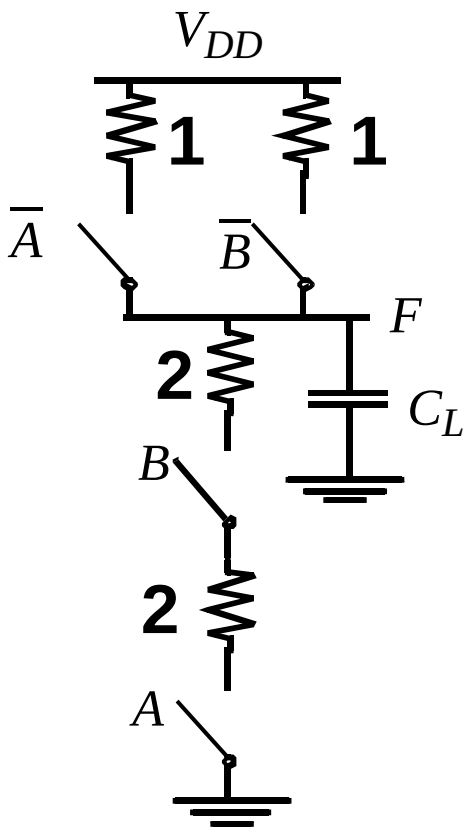
Equivalent Circuit for Measuring Power in SPICE

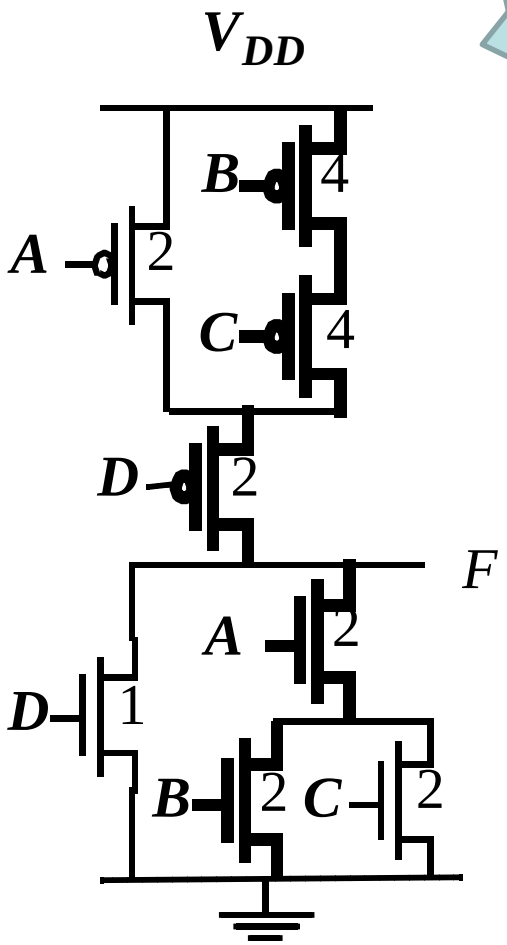
$$C\frac{dP_{av}}{dt} = ki_{DD}$$

$$or$$

$$P_{av} = \frac{k}{C}\int_0^T i_{DD}dt$$

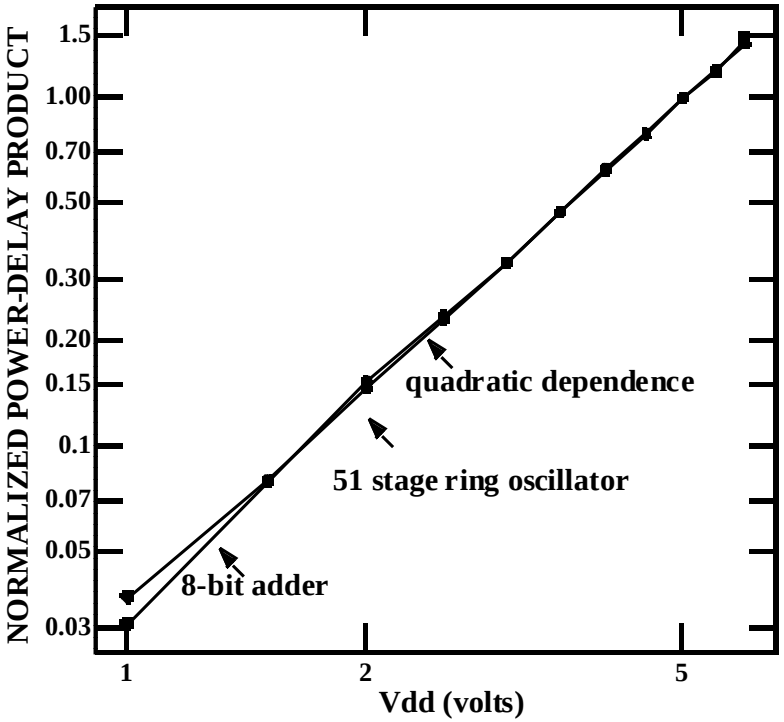
Design for Worst Case





Here it is assumed that $R_p = R_n$

Reducing V_{dd}



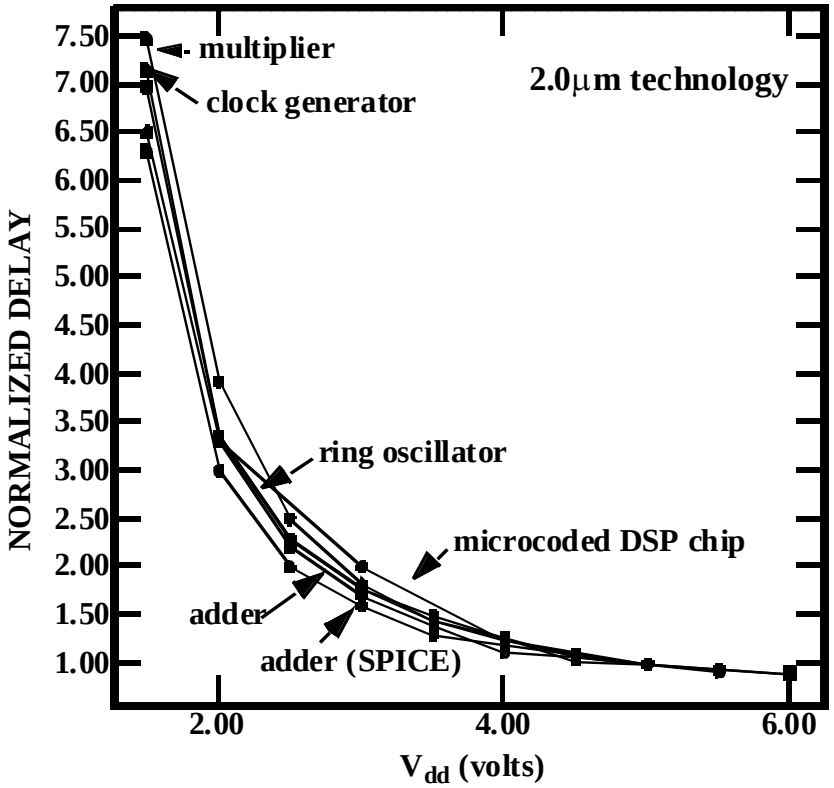
$$P \times t_d = E_t = C_L * V_{dd}^2$$

$$\frac{E_{(Vdd=2)}}{E_{(Vdd=5)}} = \frac{(C_L) * (2)^2}{(C_L) * (5)^2}$$

$$E_{(Vdd=2)} \approx 0.16\ E_{(Vdd=5)}$$

- Strong function of voltage (V^2 dependence).
- Relatively independent of logic function and style.
- Power Delay Product Improves with lowering V_{DD}.

Lower V_{dd} Increases Delay



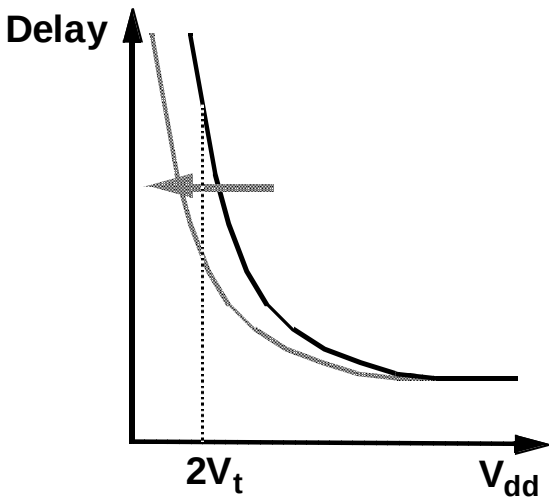
$$T_d = \frac{C_L * V_{dd}}{I}$$

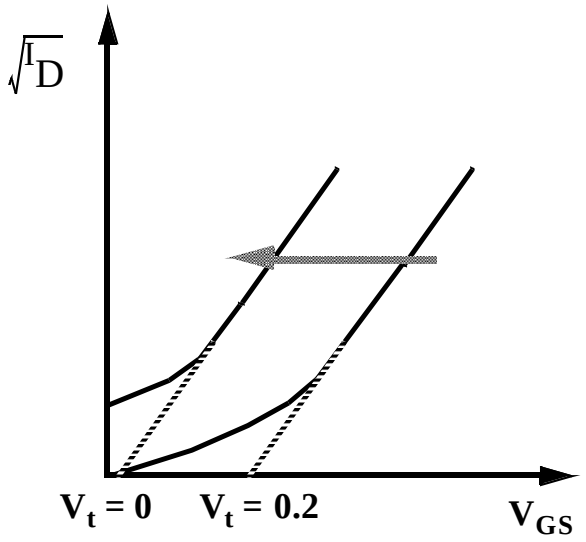
$$I \sim (V_{dd} - V_t)^2$$

$$\frac{T_{d(Vdd=2)}}{T_{d(Vdd=5)}} = \frac{(2) * (5 - 0.7)^2}{(5) * (2 - 0.7)^2} \approx 4$$

- **Relatively independent of logic function and style.**

Lowering the Threshold



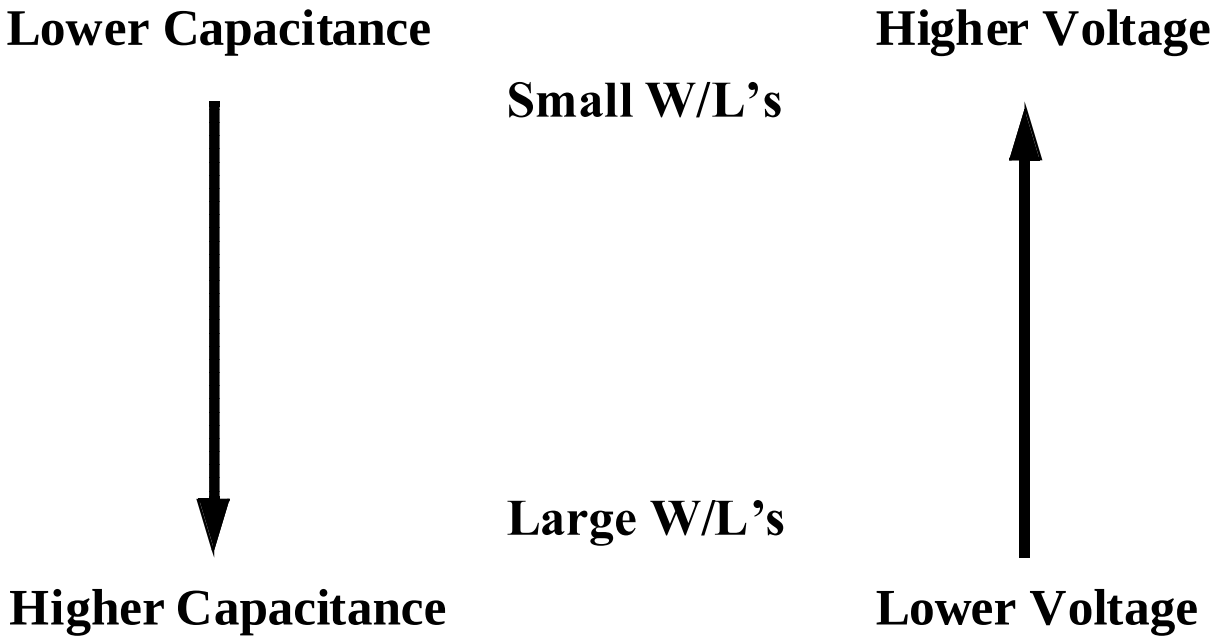


Reduces the Speed Loss, But Increases Leakage

Interesting Design Approach:

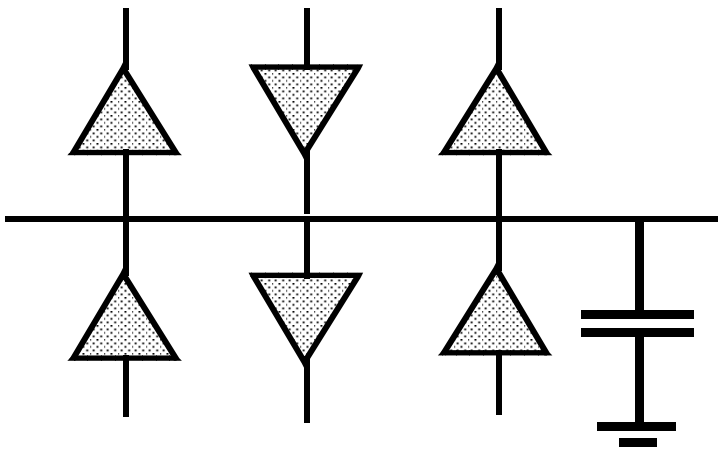
DESIGN FOR $P_{Leakage} == P_{Dynamic}$

Transistor Sizing for Power Minimization

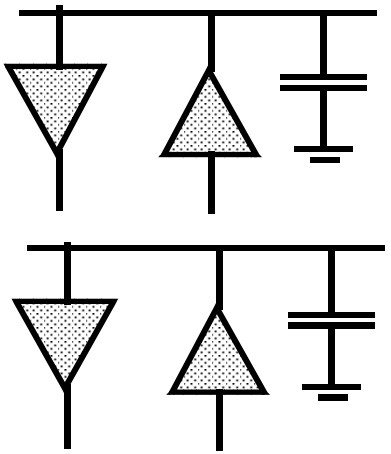


- **Larger sized devices are useful only when interconnect dominated.**
- **Minimum sized devices are usually optimal for low-power.**

Reducing Effective Capacitance



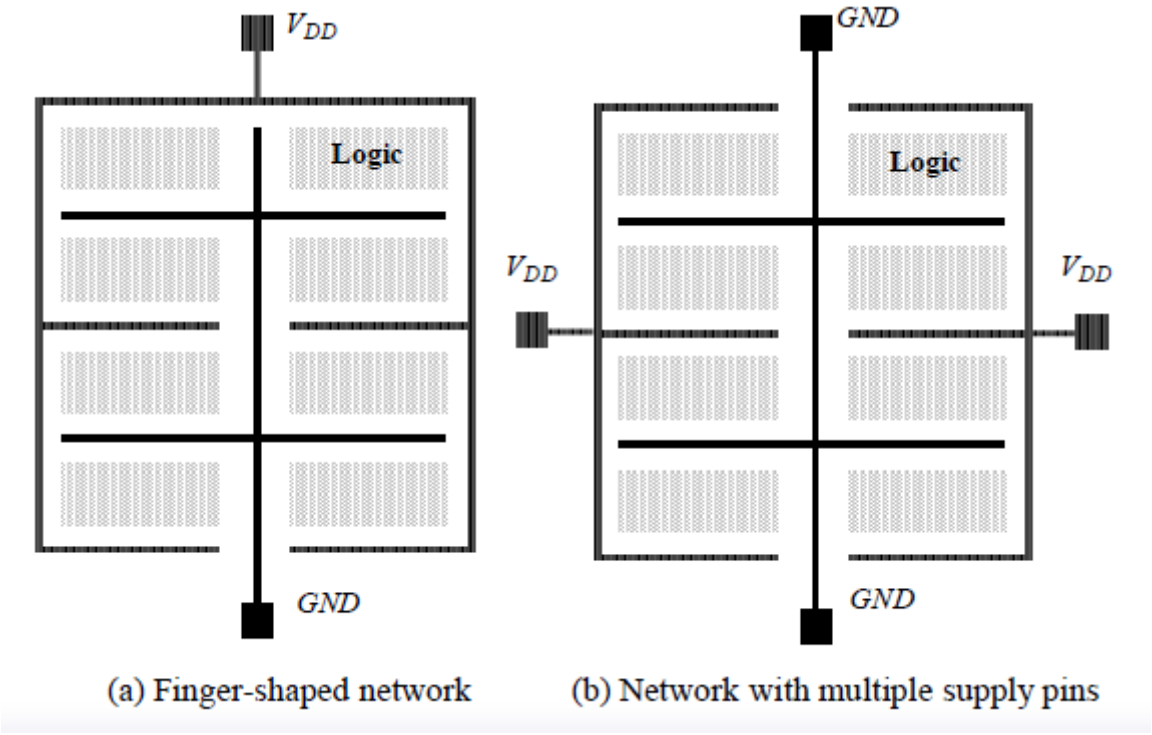
Global bus architecture



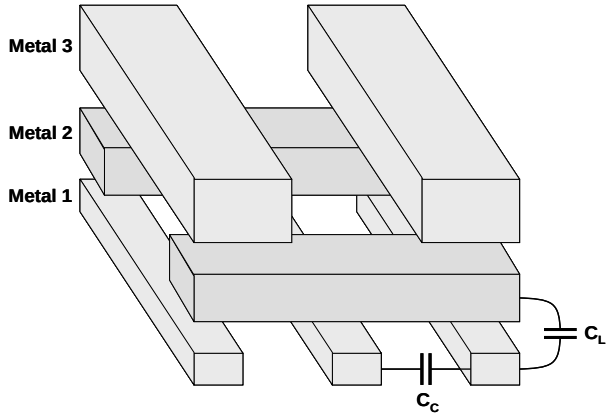
Local bus architecture

Shared Resources incur Switching Overhead

Power and Ground Distribution



Power



$$P = \alpha f C V_{DD}^2$$

Prime choice: Reduce voltage!

- Recent years have seen an acceleration in supplyvoltage reduction
- Design at very low voltages still open question(0.6 … 0.9 V by 2010!)
- Reducing thresholds to improve performance increases leakage
- Reduce switching activity
- Reduce physical capacitance

Where

P is the total dynamic power dissipation,

α the signal transition switching activity,

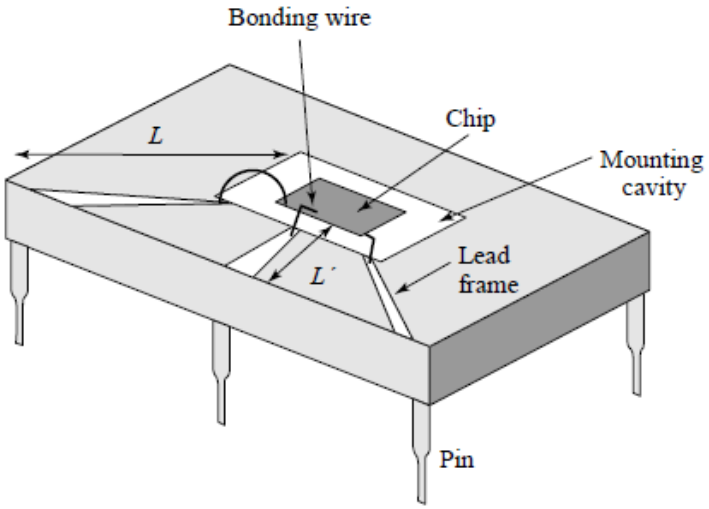
f the operating frequency of the bus,

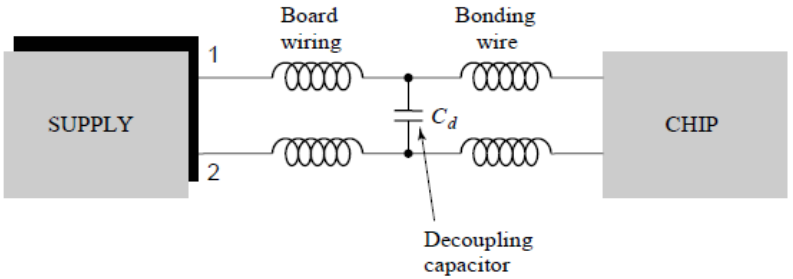
C the load capacitance of the wire line, and

V_{DD} the swing voltage. Reducing the bus power consumption is usually achieved by using a low swing voltage and operating frequency as well as reducing capacitance and switching activity

What will cover

- Aspects of power distribution design
- Power delivery design methodology
- Component behavior
- Modeling techniques

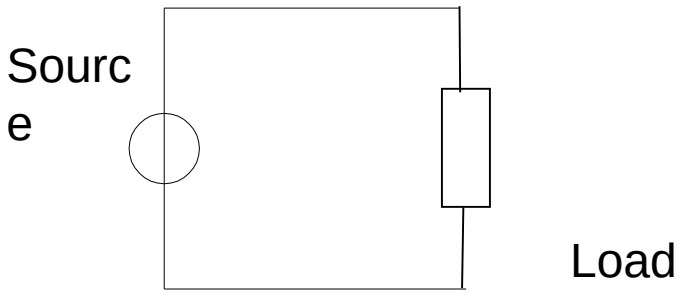




Decoupling capacitors are added:
- on the board (right under the supply pins)
- on the chip (under the supply straps, near large buffers)

Aspects of power distribution design

What is the simplest active network?
- Active element (voltage/current source) & Load (consumer of energy)



- Loads are different elements and devices, for example:
  - Capacitors
  - Resistors
  - Inductors
  - Transistors

Aspects of power distribution design (cont.)

- High level of integration in digital systems is directly affected on the power distribution system.
- There are several aspects of power distribution design:
  - PCB (board) stackup
  - Bypass capacitor (decap) selection and placement
  - Voltage partitioning
  - Package, socket and connector selection
  - Pin assignments, including selection of the signal-to-power and signal-to-ground ratios
  - Pin placement

Aspects of power distribution design (cont.)

- The basic goal in power distribution is to minimize inductance & resistance, while optimizing capacitance over a wide frequency range
- Factors that complicate the design:
  - Cost
  - Size limitations
  - Nonideal component behavior (especially for capacitors)
  - Limits on pin counts
  - Limits on signal-to-power & signal-to-ground ratios
  - Limits on the layer count on the PCB

More ….. Extra

Power delivery design methodology

1. Impedance Concepts

What is an impedance ?

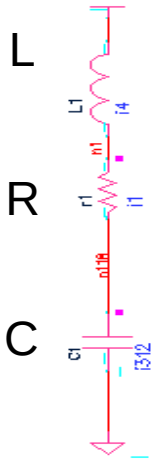
The ratio of voltage to current for exponential waveforms is defined as the impedance **Z.**

For a resistance: $\mathbf{Z_R = R}$ in Ohms

For an inductance: $\mathbf{Z_L = sL}$ in Ohms

For a capacitance: $\mathbf{Z_C = 1/sL}$ in Ohms

For R, L,C in series: **Z(s) = R + sL+ 1/sL**



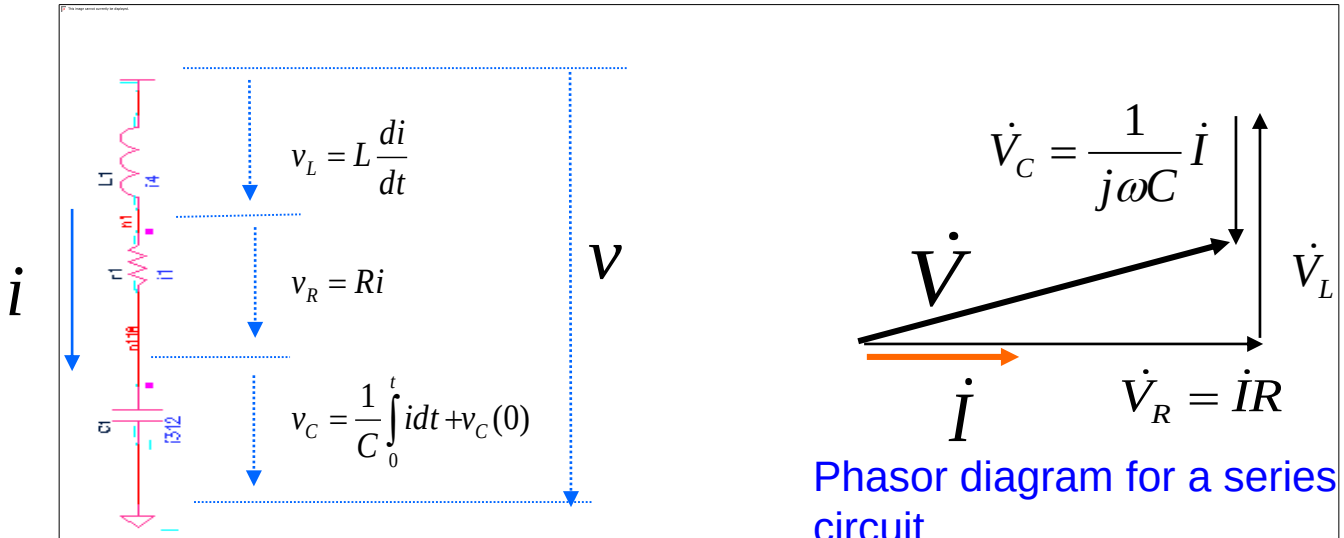
$s = \alpha + j\omega$ => complex frequency

$\alpha = Re(s)$ => damping factor,

$\omega = Im(s)$ => angular frequency.

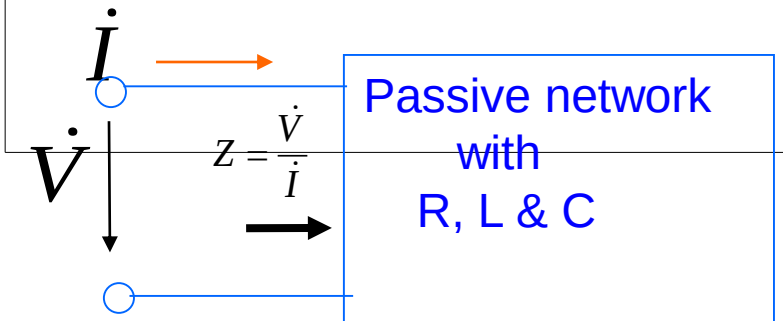
Power delivery design methodology

2. Impedance Concepts



Phasor diagram for a series RLC circuit

Impedance Z is the ratio of the terminal voltage phasor to the terminal current phasor.



$$v = v_L + v_R + v_C$$

$$v = V_m \sin \omega t$$

$$i = I_m \sin(\omega t - \varphi)$$

$$I_m = \frac{V_m}{z} = \frac{V_m}{\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}}$$

$$x_L = \omega L$$

$$x_C = \frac{1}{\omega C}$$

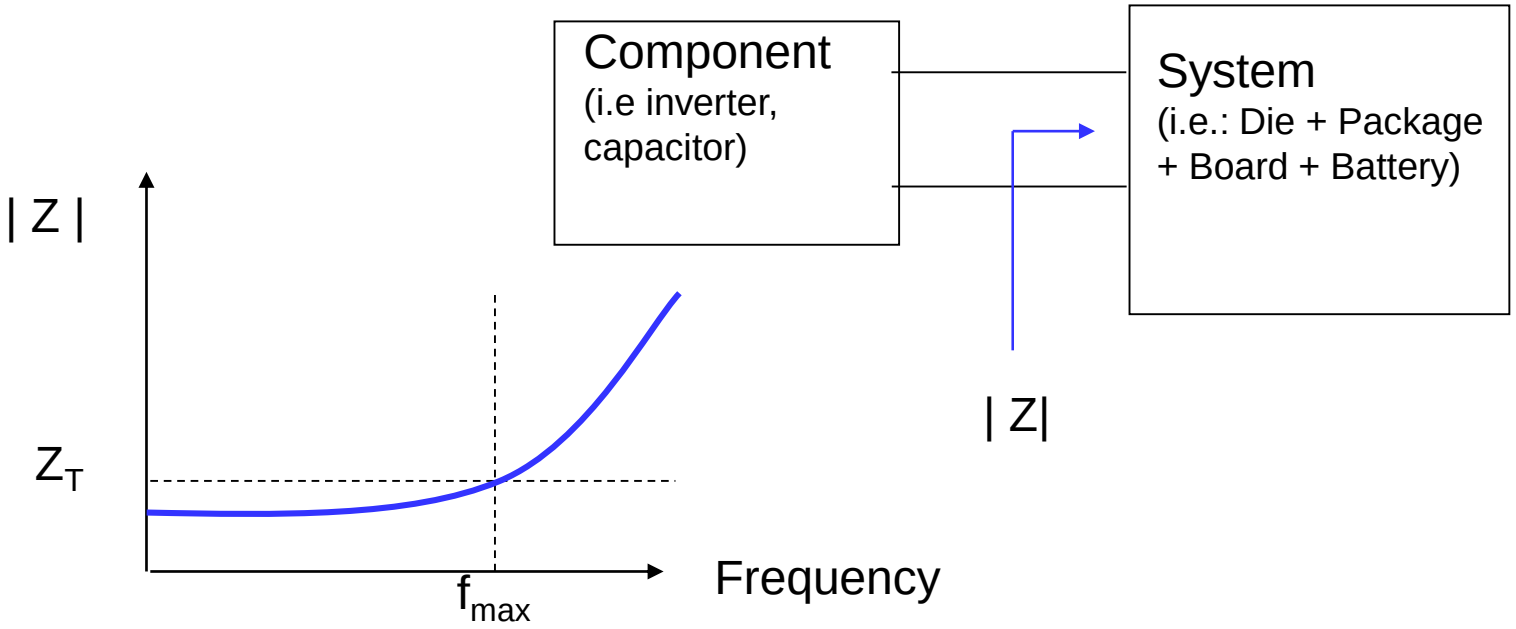
$$Z = R + j(x_L - x_C)$$

Power delivery design methodology (cont.)

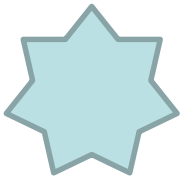
2. Target Impedance

The power distribution system must work as low-impedance voltage source over a bandwidth from DC to several harmonics of the clock frequency (to minimize the generation of noise, radiation of electromagnetic energy and EMI).

Target impedance Z_T is the maximum allowed impedance for the system to meet a specified noise level.



Power delivery design methodology (cont.)



3.Techniques for lowering | Z |:

a) packaging,

b) PCB stackup,

c) bypass capacitor

a) Packaging (include integrated circuit packages, sockets & edge connectors)

|Z| is lowerd:

-by choosing a packaging component that offers a shorter connection for lower partial self inductance

- by assigning more pins to power and ground connections

(lower signal/ground & signal/power).

Package styles:

BGA – ball-grid array (C4 bump)

QFP – quad flat pack

BGAs have more pins than GFPs

Power delivery design methodology (cont.)

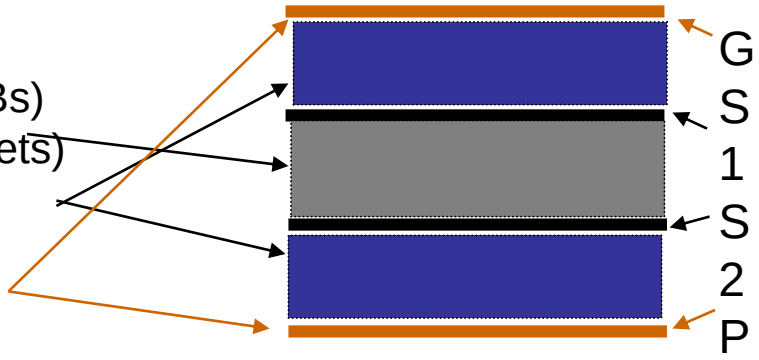
b) PCB stackup

The PCB stackup strongly affects the impedance |Z| of the power distribution system

Multilayer PCB's elements are:

- -cores (two-sided PCBs)
- -pregreg (dielectric sheets)
- -copper sheets

S1, S2 – routing layers
G, P – ground & power planes



Power delivery design methodology (cont.)

c) Bypass capacitance (decap)

High-performance design require bypass capacitance for four reasons:

1) supplying current bursts for fast switching circuits (near the component, large value) ;

2) providing an AC connection between power and ground planes for return currents (near the power pins of high-speed component, small value);

3) controlling EMI (distributed, small value);

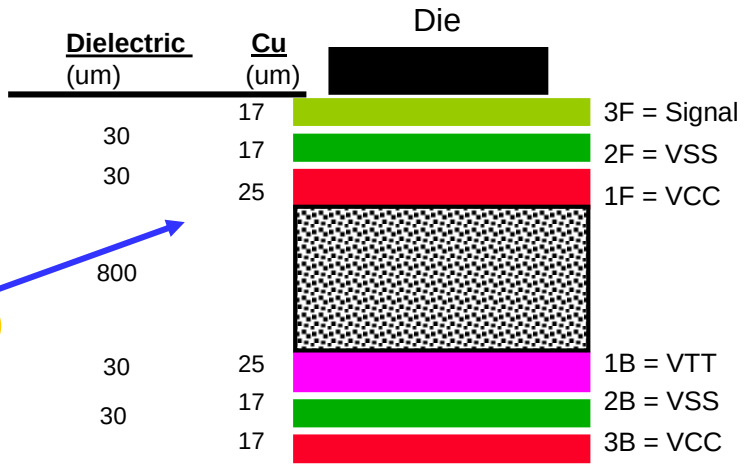
4) lowering the impedance |Z| of the power distribution system (system design).

For all of this uses, capacitors connect the power & the ground planes. The difference is the size and quality of capacitors and their locations.

Power delivery design methodology (cont.)

Example of Package template

- Package
  - ⇨ FCPGA 35 x 35mm
  - ⇨ 2-2-2 Stack up



Package Assumptions (slide of ATD group)

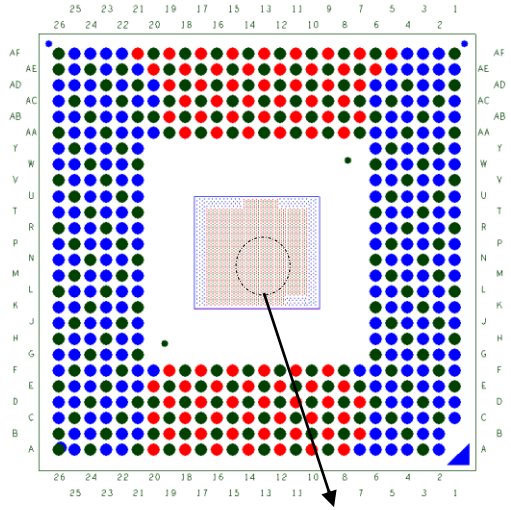
- ⇨ POR X62 FCPGA3 Design Rules
- ⇨ 17um Build up Layer thickness (stretch target)
- ⇨ **Capacitors**
  - ●0805 IDC+ Under the die L = 57pH; R = 6.5mOhm
  - ●Outside the die

    0805 IDC+ L =2.5 * 57pH; R = 6.5mOhm

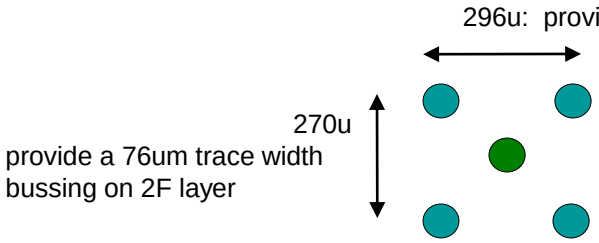
    1206 L = 220pH; R = 5mOhm *(L is too optimistic; Ansoft modeling yields 600pH - 800pH)*

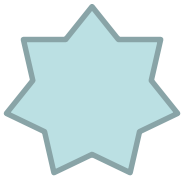
    Did not account for VTT or PLL capacitor requirements.

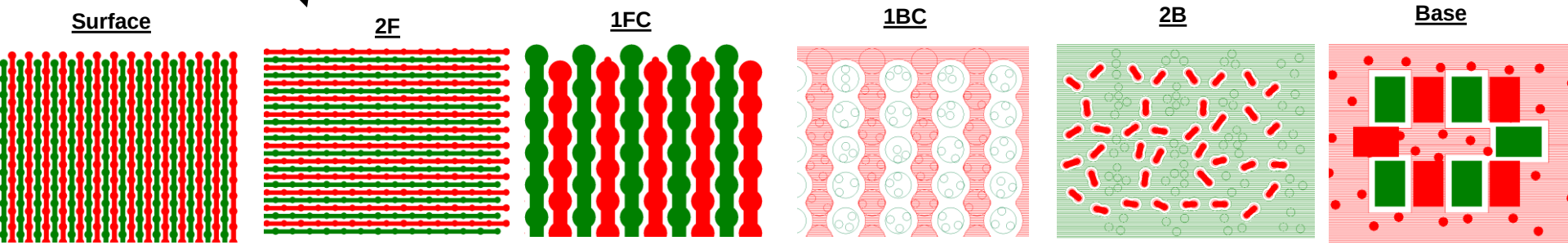
Power delivery design methodology (cont.)

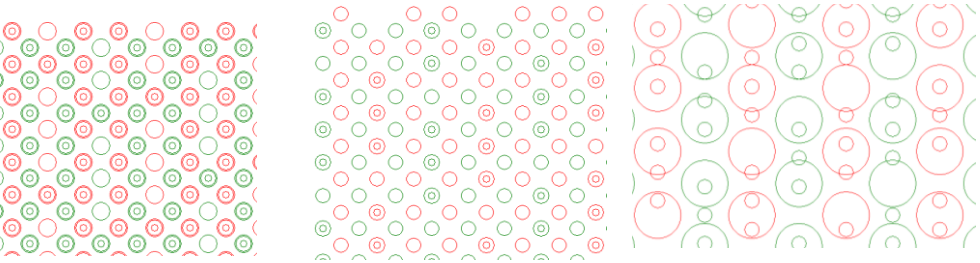


- C4 bump pattern:





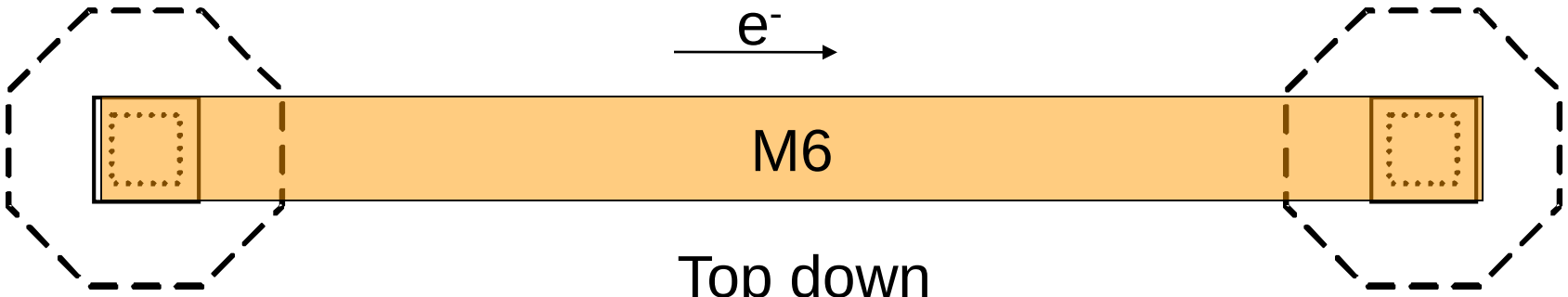




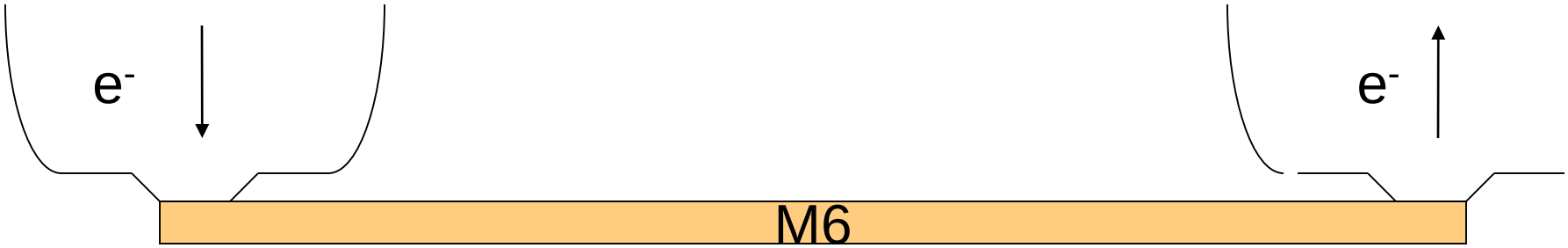
- 75% via connection to die bumps from 2F.
- 25% via connection to die bumps from 1FC or PTH.
- ~ 3 via connection to 2 PTHs

Example: P1262 DT Power Delivery WW17.4
Power Bussing In Netlist, slide of ATD group

C4 Bump & M6 of Die

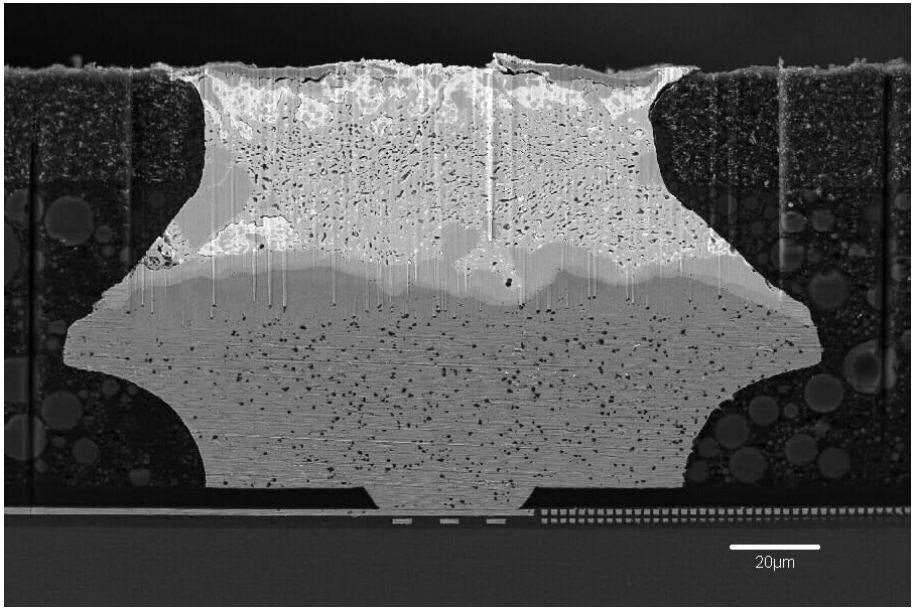


Top down

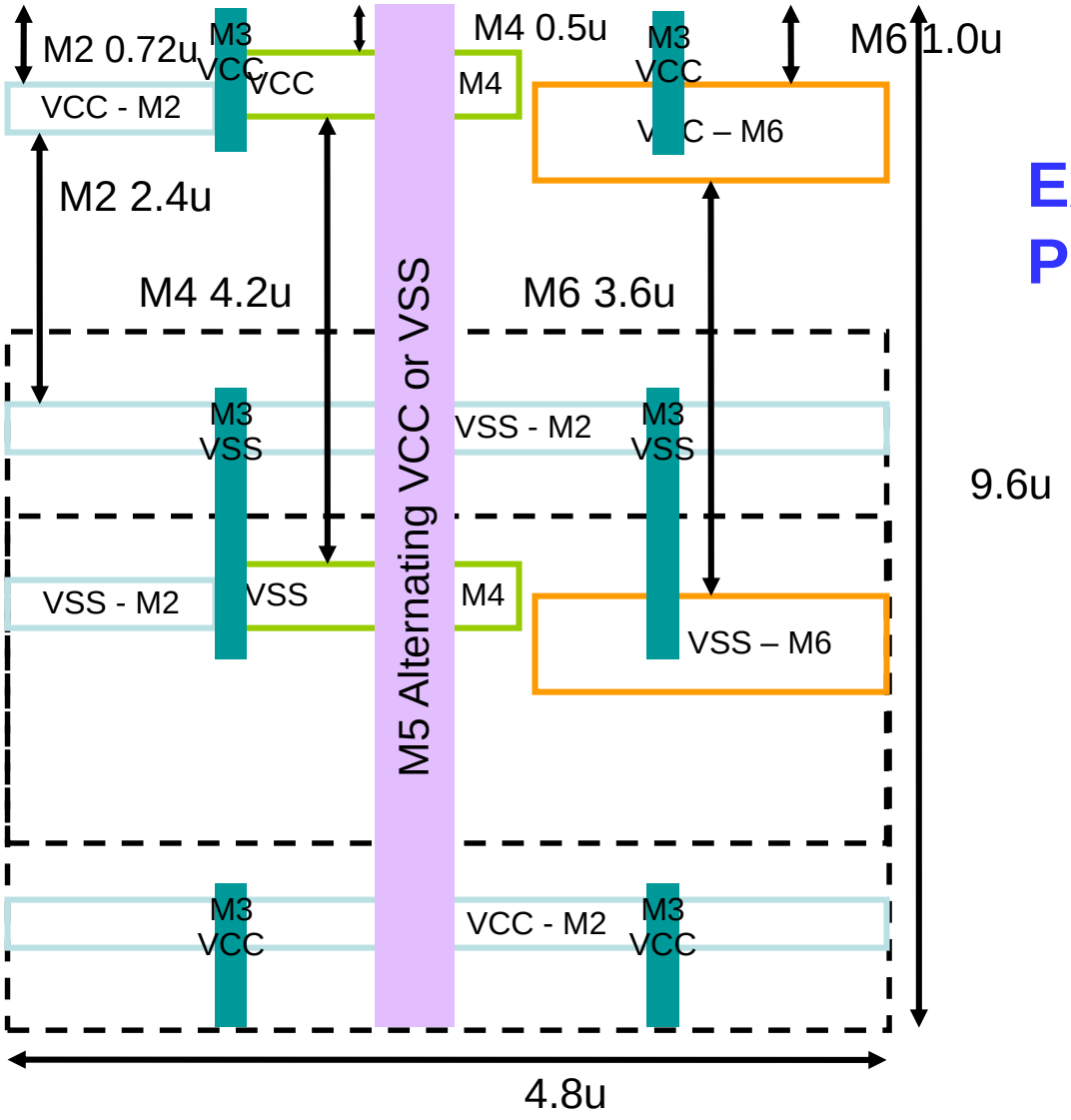


Side View

C4 Bump Cross Section

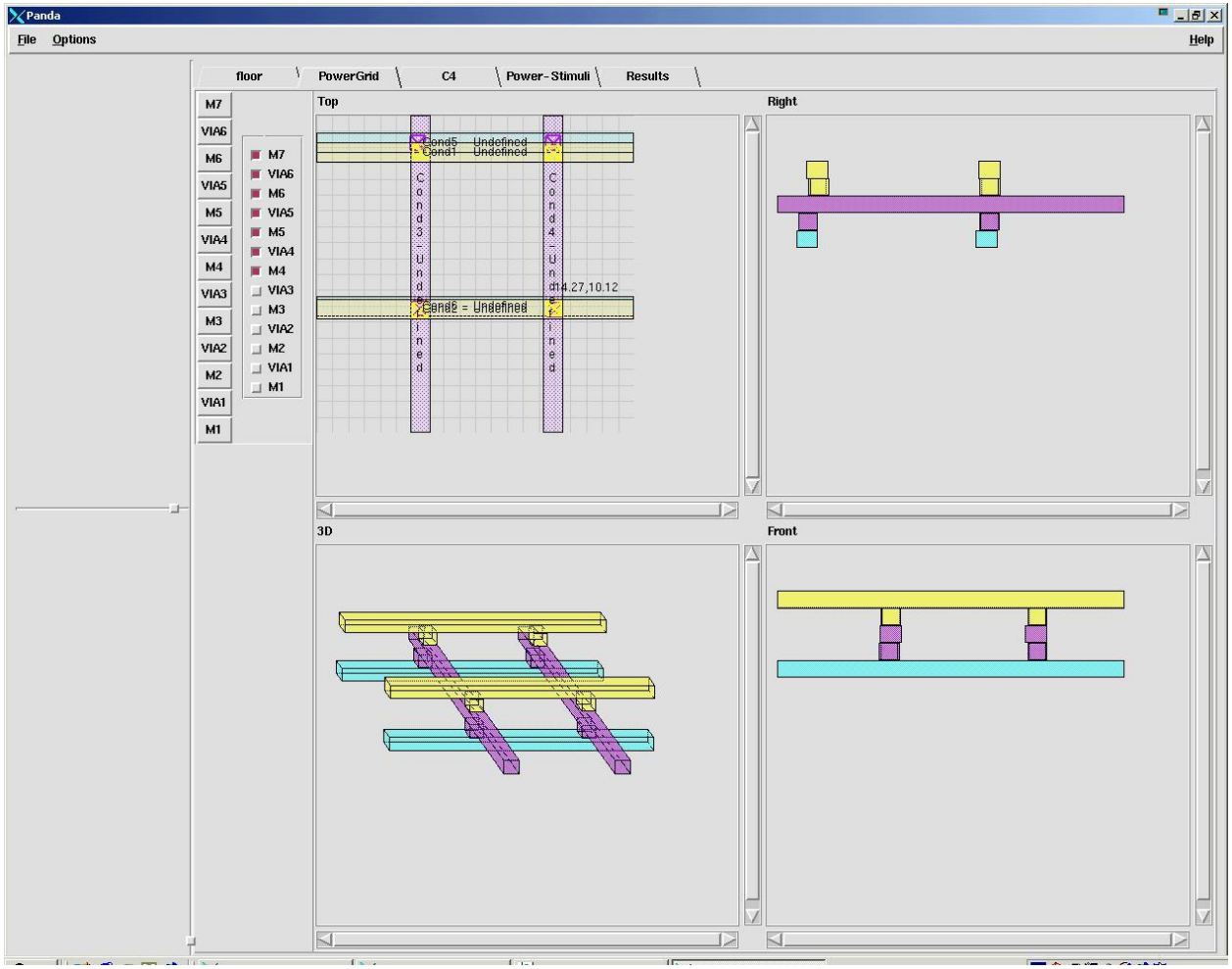


P1262 M2-M6 Power-B. Martell

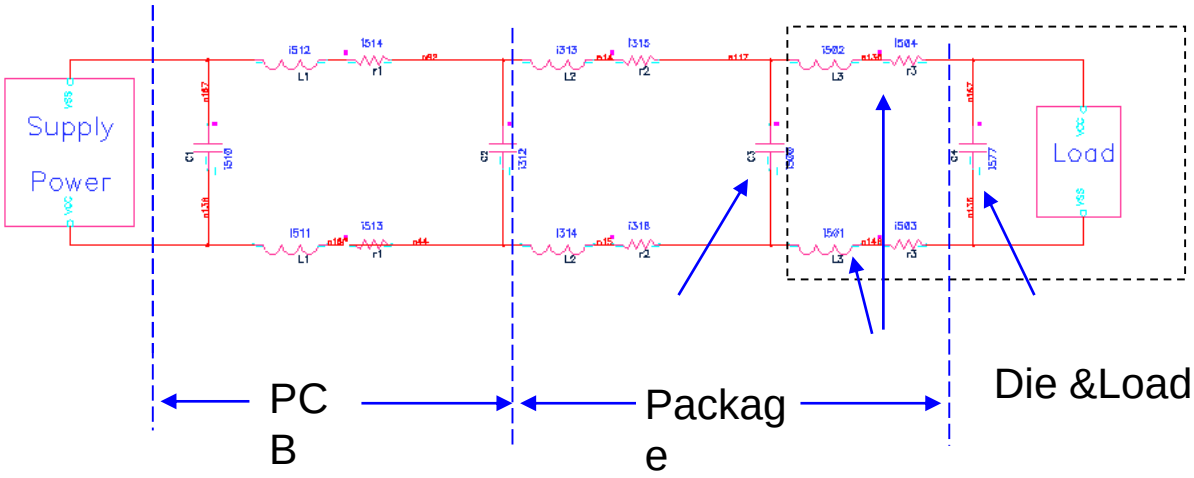


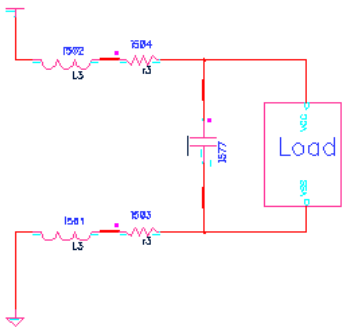
Example of PG template

3D PG: Template for M6, M5 & M4 Panda, GUI



Power Delivery 3-levels Model





Power delivery package to die and die model

Component Behavior

Conductors for power supply & for impulse signals:

$$Z = R + j\omega L$$

=>R, RL, RLM

Pins => R

Capacitors:

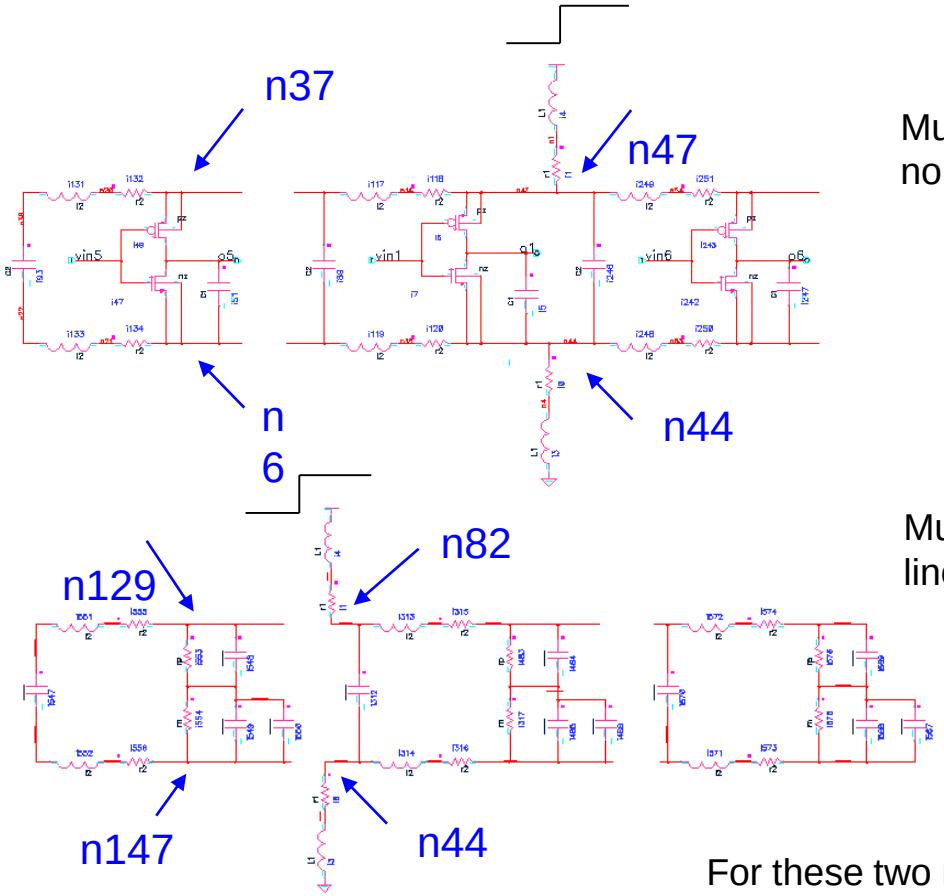
=> open circuit, RC, RL

Transistors: nonlinear & linear models

$$Z = R + j(\omega L - \frac{1}{\omega C})$$

Component behavior

Linear RLC Model and Comparison with Nonlinear Model

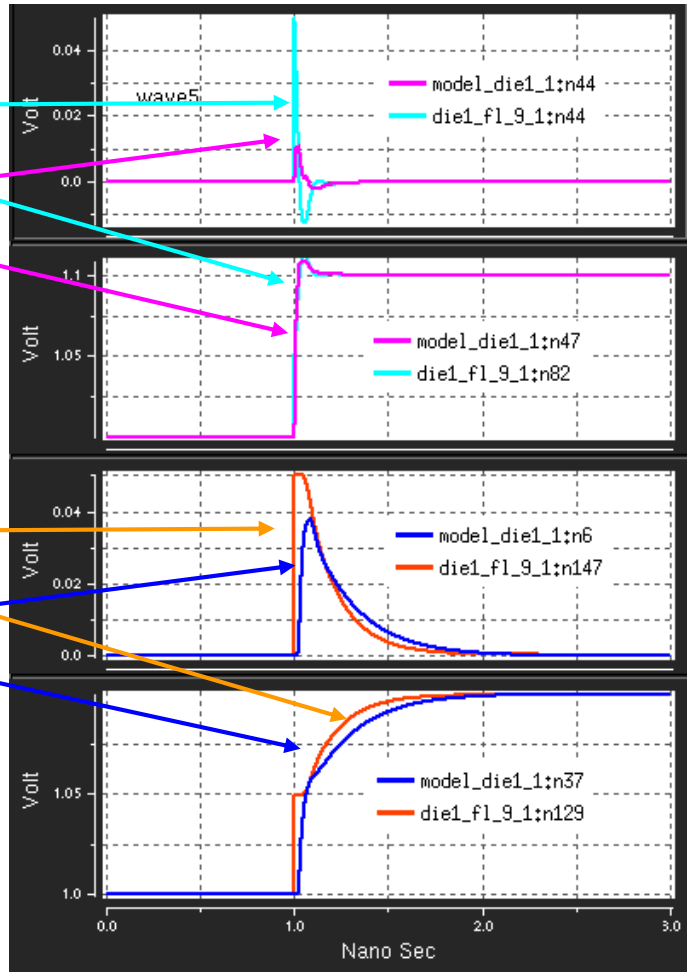


Multi-cascades (9 cascades)
nonlinear model

Multi-cascades (9 cascades)
linear RLC model

For these two models response voltage waves to VCC-input = 1(t)V step-function were found in vcc & vss on die nodes .

Component Behavior (cont.)
Linear and Nonlinear Power Grid Models Results

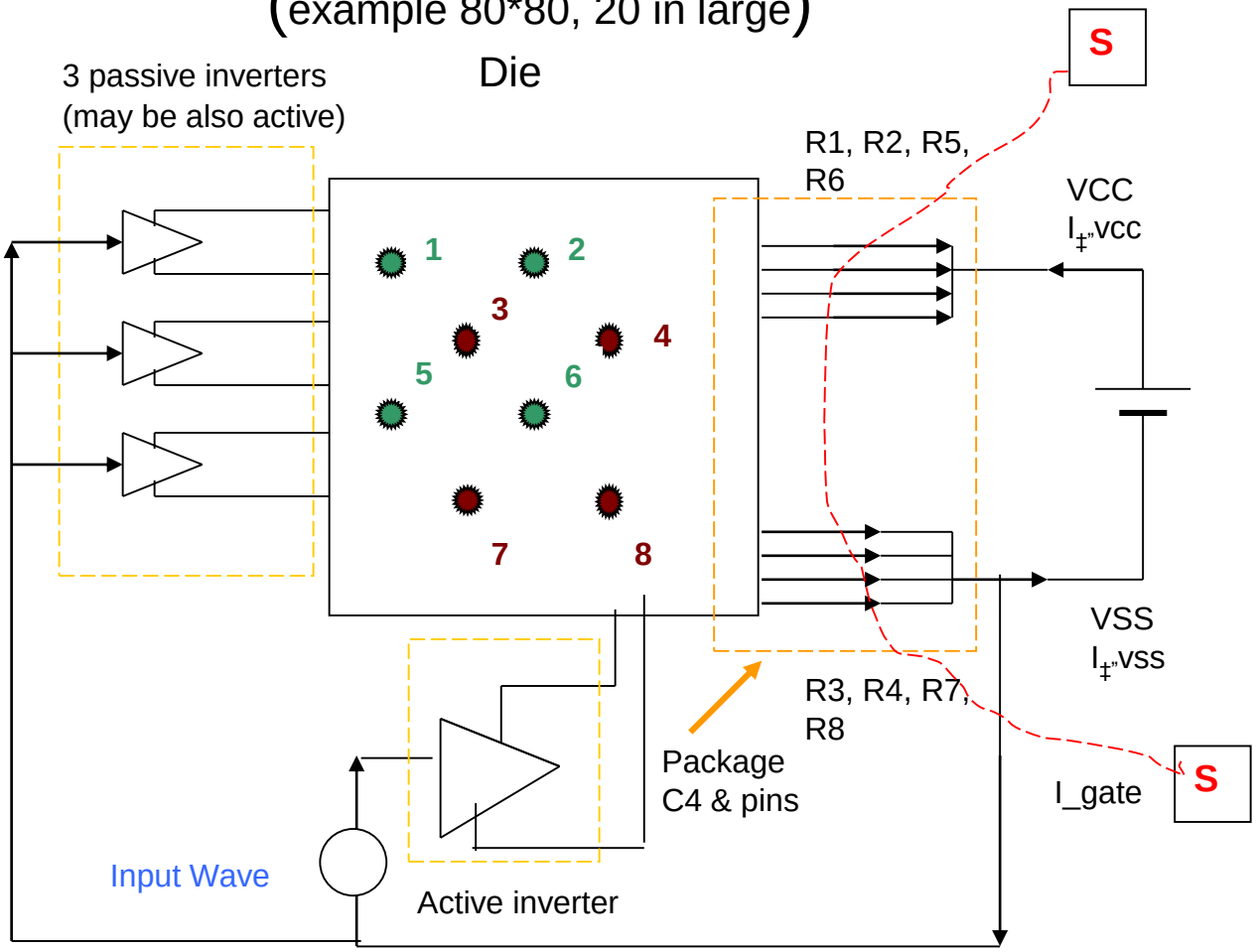


model_die1 is nonlinear model

die1_fl_9 is linear model

Modeling techniques

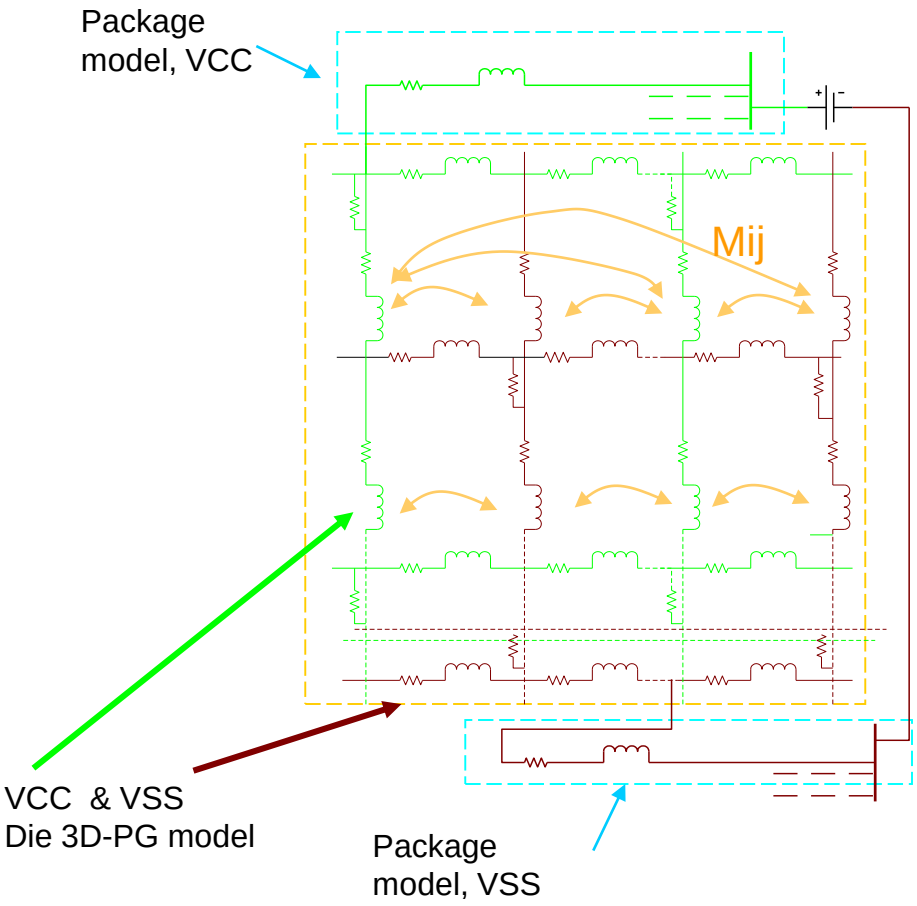
(example 80*80, 20 in large)



$$\sum I_{sectionS} = 0$$

$$\sum I_{sectionS} = \sum I_{c4pins} - \sum I_{gates}$$

3D Die +Package Distributed Model



2D LM-matrix:

	1	2	3	…	n
1	L_1	M_{12}	M_{13}	…	M_{1n}
2	M_{12}	L_2	M_{23}	…	M_{2n}
3	M_{13}	M_{23}	L_3	…	M_{3n}
……					
n	M_{1n}	M_{2n}	M_{3n}	…	L_n

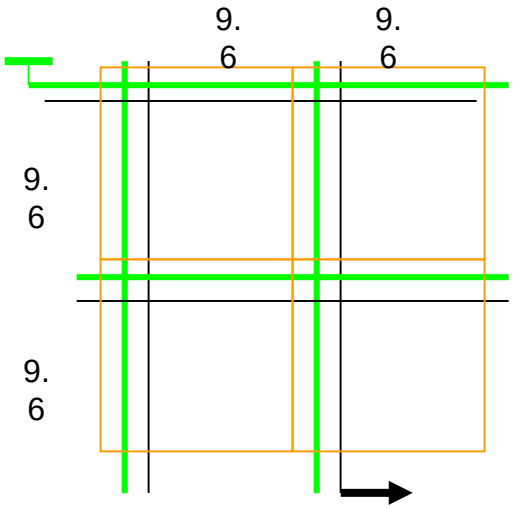
Number Mij:

$$\frac{1}{2} n_H * (n_H - 1) * s_H + \frac{1}{2} n_V * (n_V - 1) * s_V$$

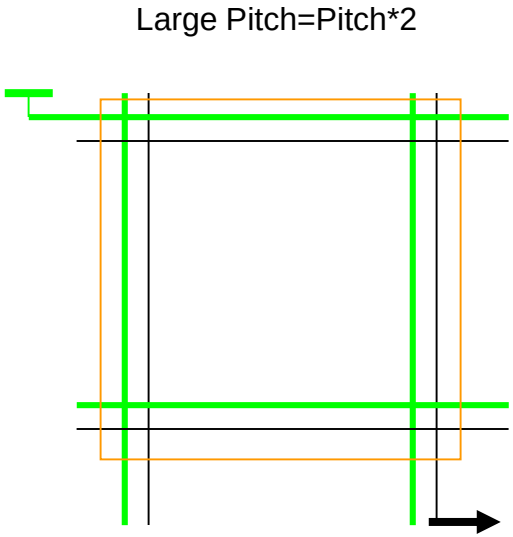
$$n_H, n_V \Rightarrow \#conductors$$

$$s_H, s_V \Rightarrow \#sections$$

Use large templates: merge several ones into large macros



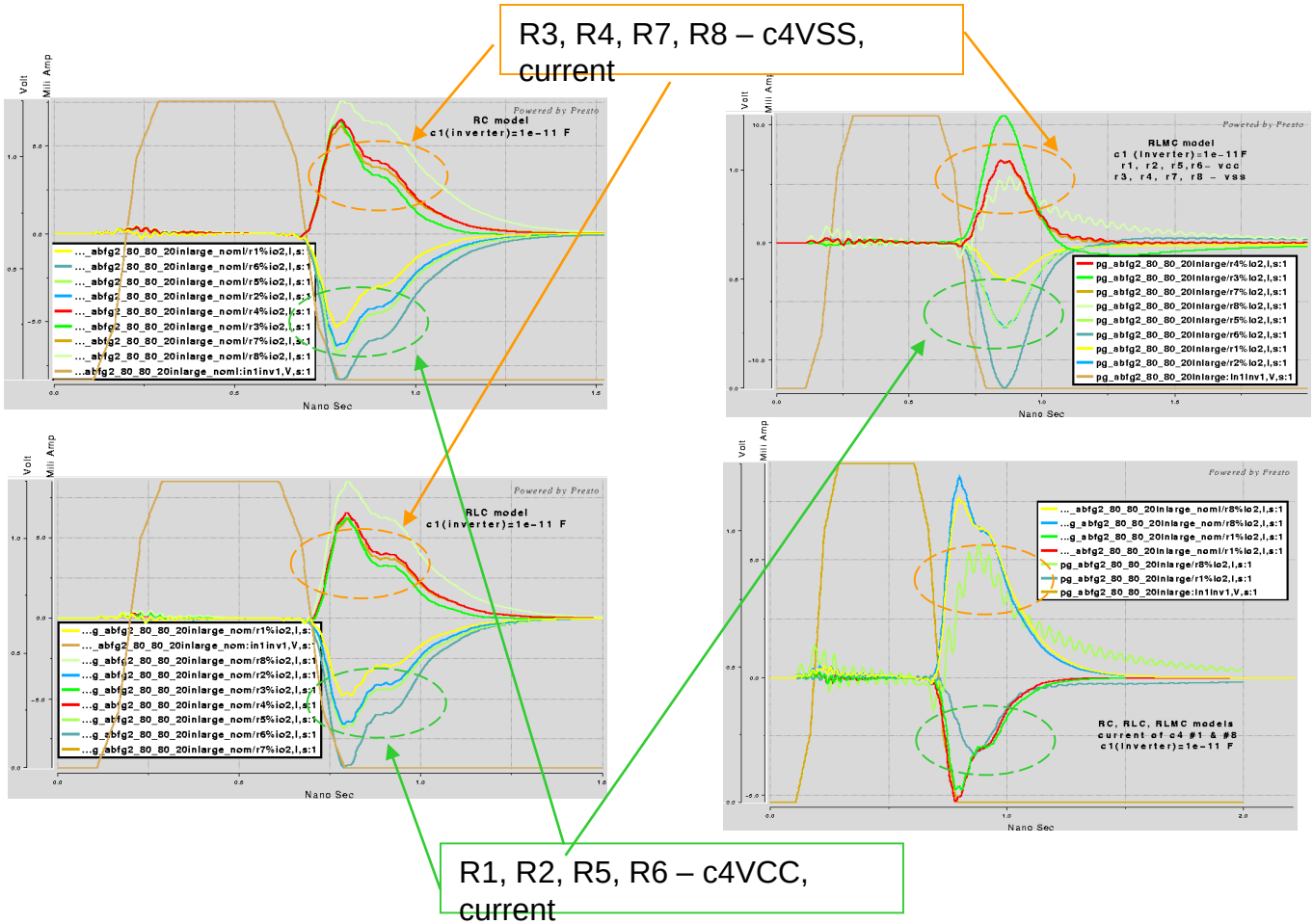
Four basic templates



One Large template

Modeling techniques

(RC, RLC, RLMC models. Example 80*80, 20 in large, 3 passive & 1 active inverter, c4 bumps current)



Summary

We have covered the following topics:

Aspects of power distribution design & factors that complicate the design

Power delivery design methodology:

- Impedance Z concept
- Techniques for lowering | Z |: packaging, PCB stackup, bypass capacitor

Components behavior: conductors, capacitors, transistors

Modeling techniques:

- Package+die 3D model
- Use large template for die
- Results of simulations (current & voltage responses, input impedance)