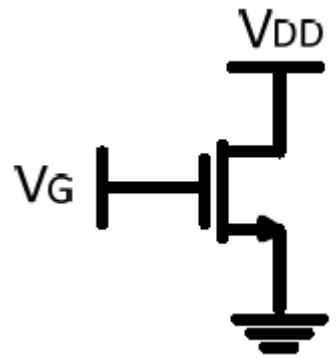
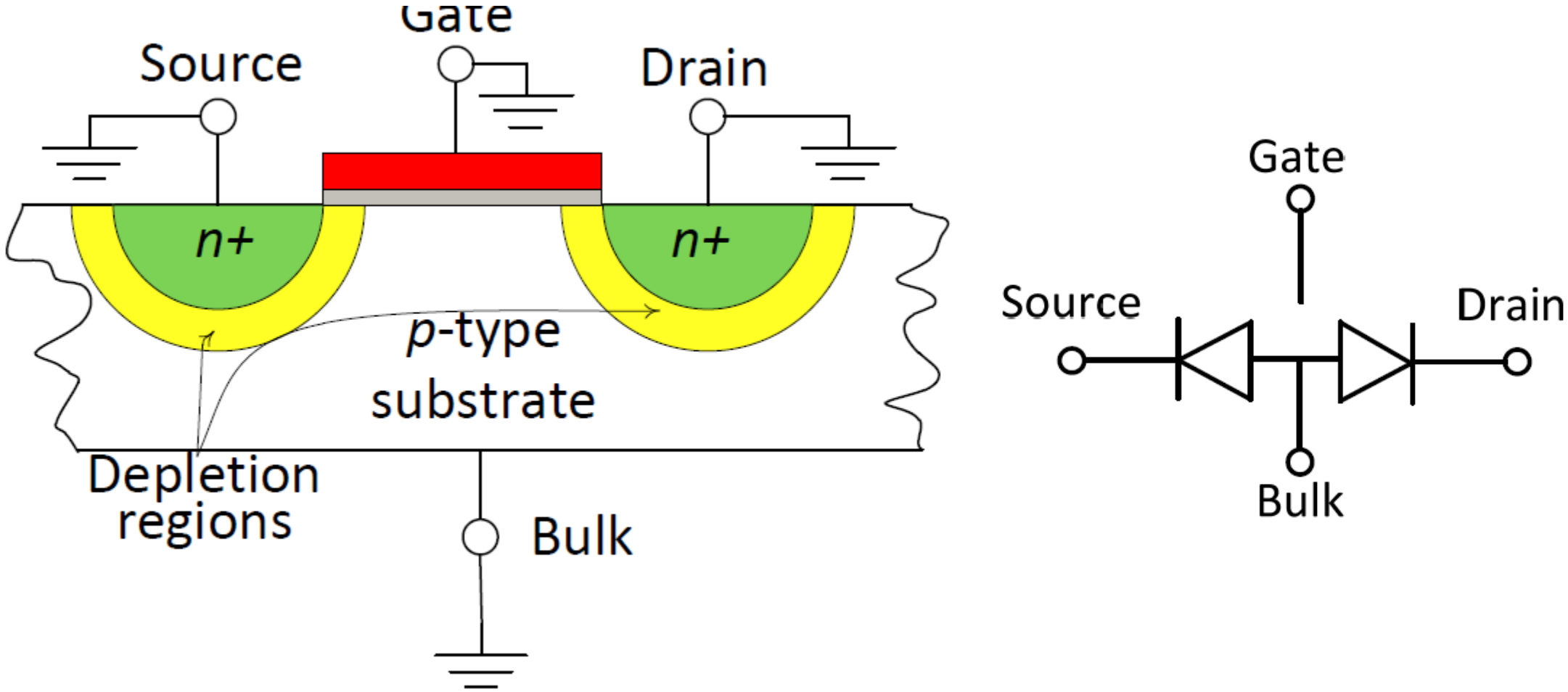
MOS Mode of operation

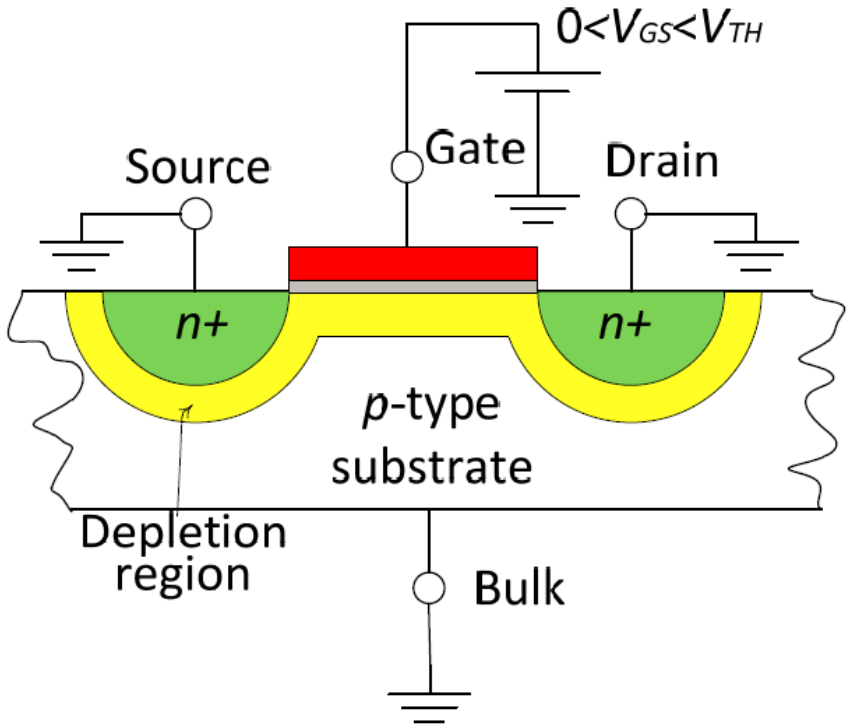


Equivalent circuit of an NMOS transistor with all terminals biased to ground



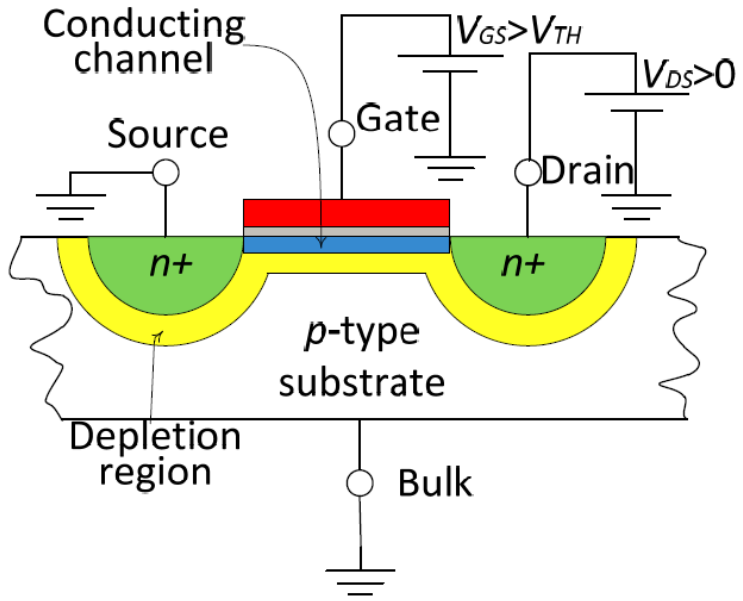
NMOS transistor with a 0<*VGS*<*VTH*.

- current cannot flows between Source and
- Drain, and the device is still in cut-off region.



Linear or triode region

- When *VGS*>*VTH*, the NMOS transistor is on, i.e. the conducting channel is formed, then a current flow
- between Source and Drain can exist.



$$I_{DS} = \frac{N \cdot q}{t_d} = \frac{Q_{ch}}{t_d}$$

$$Q_{ch} = C_{ox} \cdot L \cdot W \cdot (V_{GS} - V_{TH}) = C_{ox} \cdot L \cdot W \cdot V_{ov}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$t_{ox} = \frac{L_{min}}{50}$$

In standard CMOS technologies of the last twenty years t_{ox} is about fifty times lower than the minimum channel length L_{min}

$$t_d = \frac{L}{v_d}$$

Drift time, t_d, is directly proportional to the channel length L, and inversely proportional to the drift velocity of electrons, v_d,

Linear or triode region

$$v_d = \mu_n \cdot \varepsilon_y$$

$$\varepsilon_y = \frac{V_{DS}}{L}$$

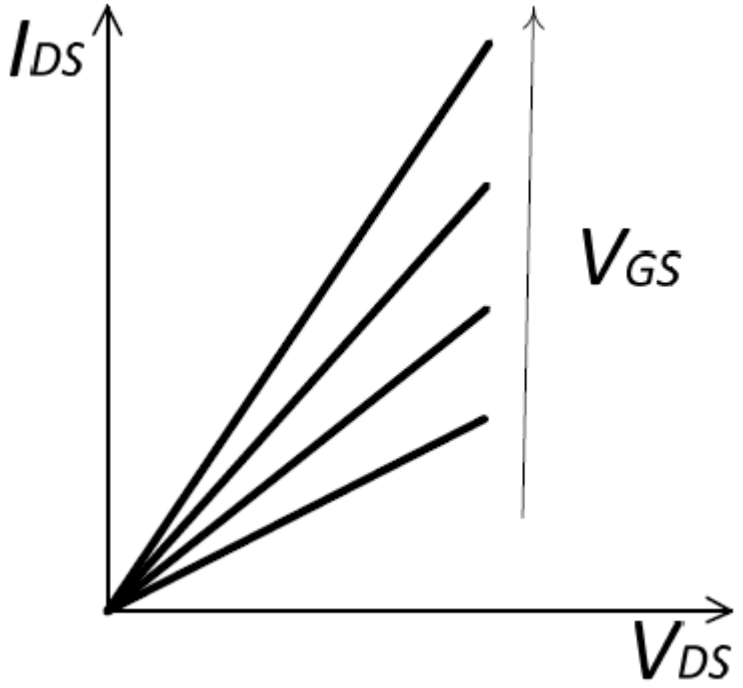
- Drift velocity, *vd*, is proportional to the horizontal electric field, εy,
- where *μn* is the electron mobility in the channel. The value of the horizontal electric field, εy

$$I_{DS} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot V_{DS} = 2 \cdot k_n \cdot V_{ov} \cdot V_{DS}$$

$$k_n = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L}$$

the NMOS transistor acts
like a variable resistance, R_{on}, whose value depends on V_{ov}

$$R_{on} = \frac{1}{2 \cdot k_n \cdot (V_{GS} - V_{TH})} = \frac{1}{2 \cdot k_n \cdot V_{ov}}$$



Linear or triode region

- a more accurate calculation of the channel charge is get by adding $V_{DS}/2$

$$Q_{ch} = C_{ox} \cdot L \cdot W \cdot \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right)$$

$$I_{DS} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) \cdot V_{DS} = 2 \cdot k_n \cdot \left(V_{ov} - \frac{V_{DS}}{2} \right) \cdot V_{DS}$$

Saturation region

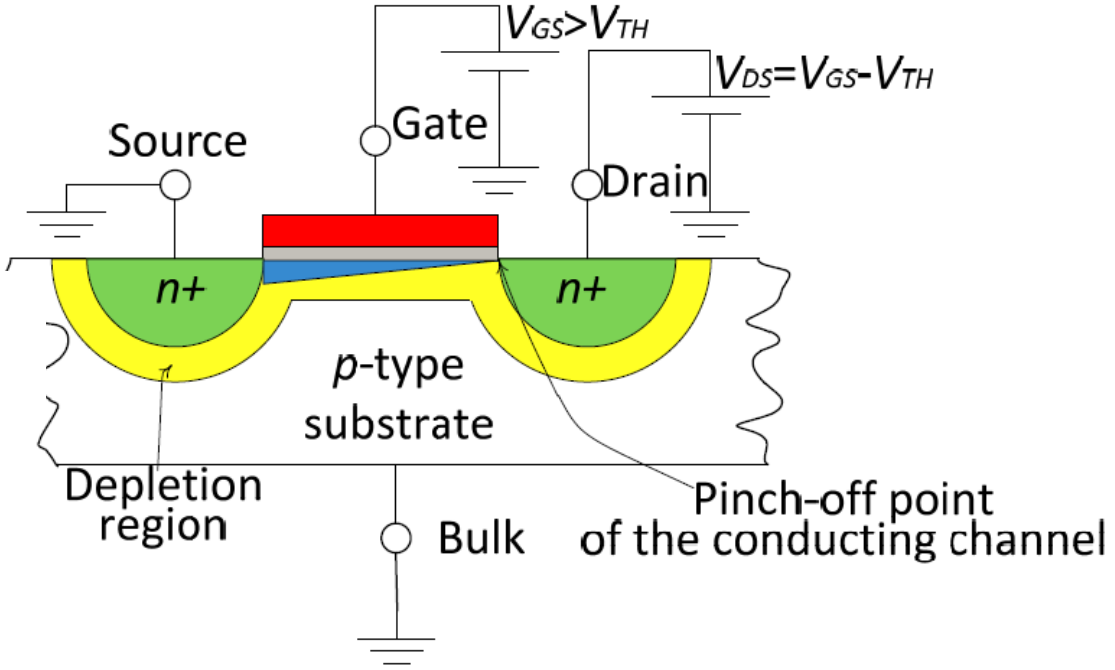
$$V_{GD} = V_{GS} - V_{DS} = V_{GS} - (V_{GS} - V_{\mathrm{TH}}) = V_{\mathrm{TH}}$$

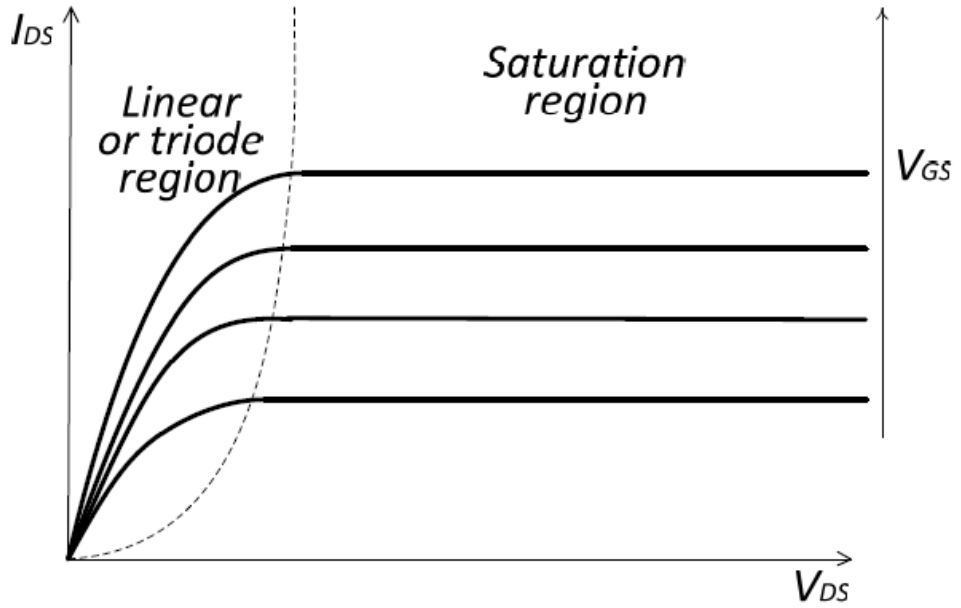
$$I_{DS} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 = k_n \cdot (V_{GS} - V_{TH})^2 = k_n \cdot V_{ov}{}^2$$

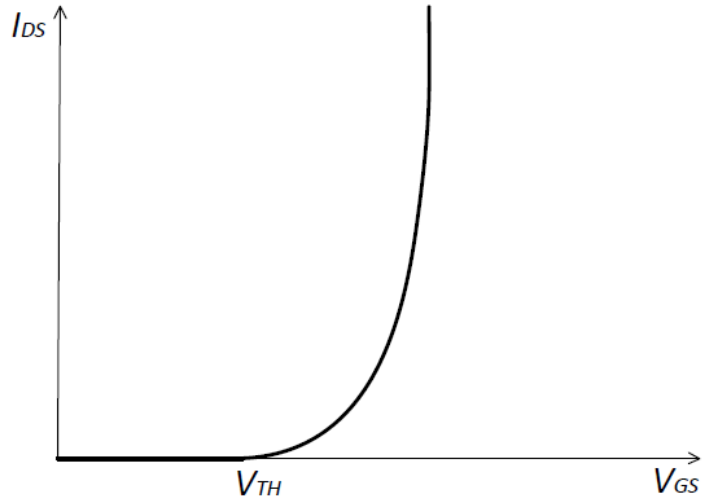
As *VDS* approaches *VGS*-*VTH*, the channel charge approaches zero at the Drain end.

In facts, the channel charge is sustained by a Gate-Drain voltage, *VGD*, at the drain side, which is less than *VGS* at the Source side.

When *VDS* compensates for the overdrive voltage *VGS*-*VTH*, *VGD* results to be equal to the threshold voltage *VTH*





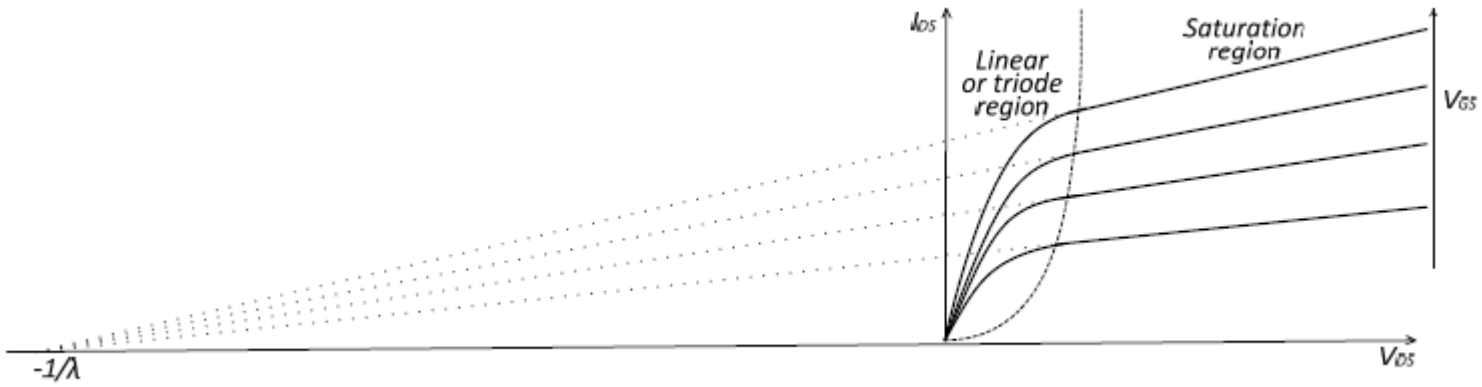


I_{GS}-V_{GS} input characteristic of the NMOS transistor in saturation region

Saturation region

$$L_{eff} = L - \Delta L$$

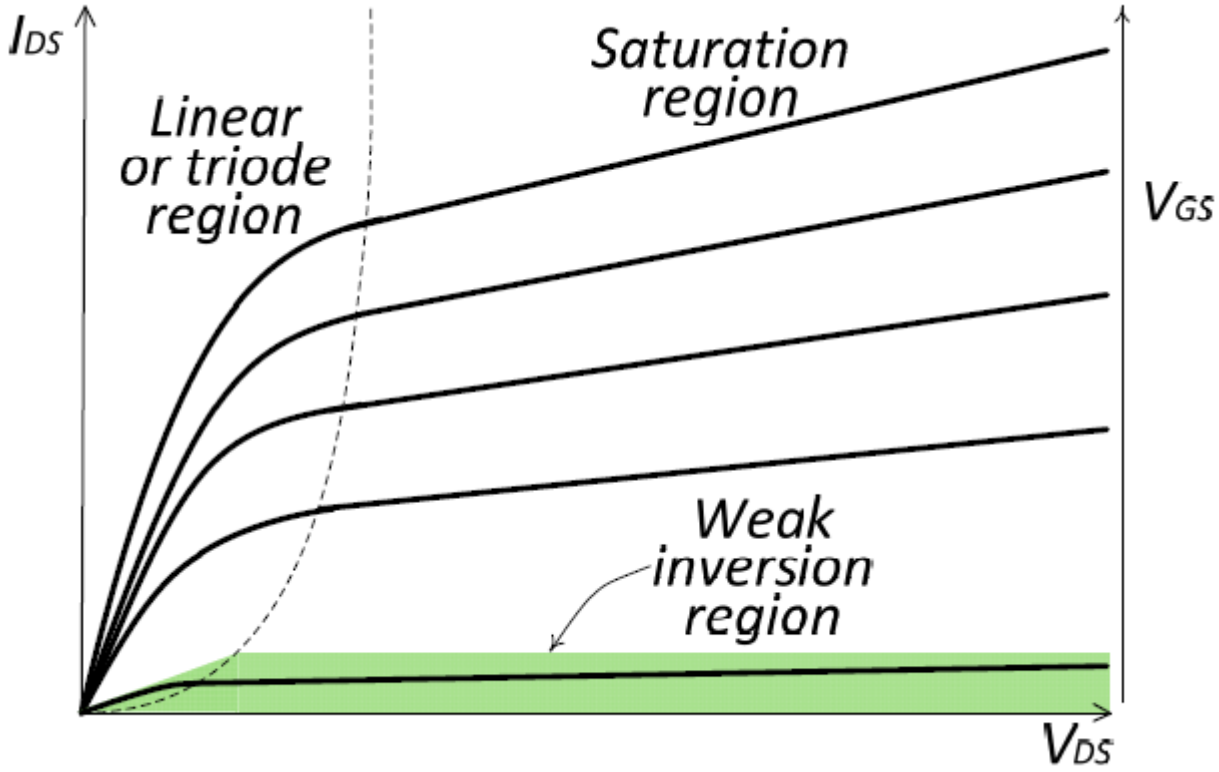
$$I_{DS} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L_{eff}} \cdot (V_{GS} - V_{TH})^2$$



Weak inversion-leakage

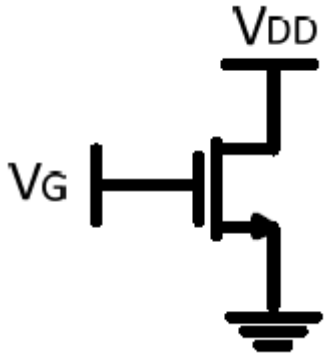
$$I_{DS} = I_S \cdot e^{\frac{V_{sur}}{V_t}}$$

$$I_{DS} = I_0 \cdot e^{\frac{V_{GS}}{n V_t}}$$

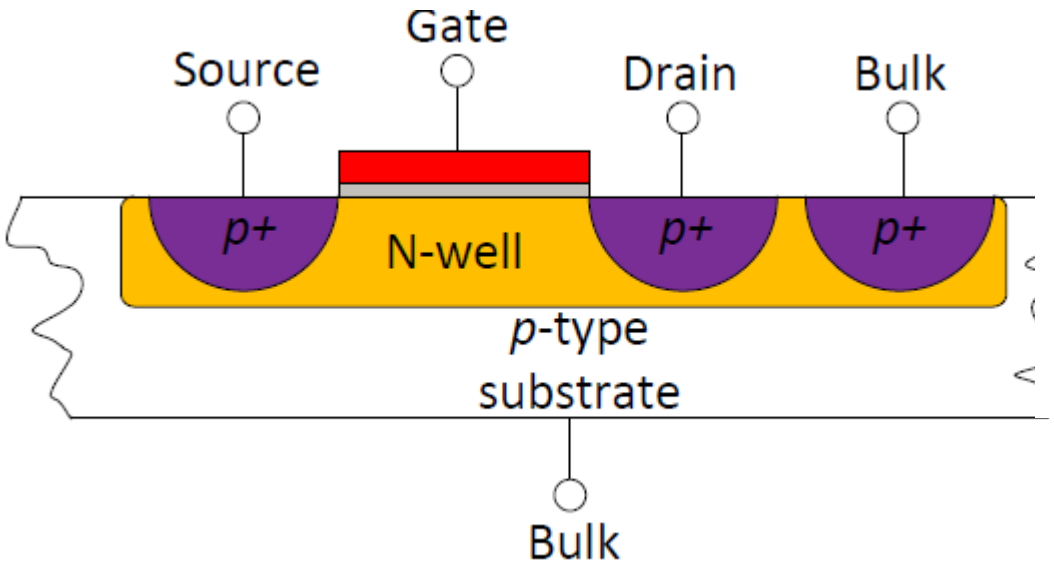


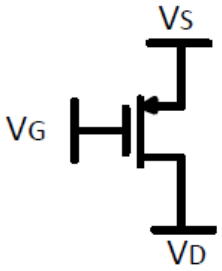
Summary for NMOS

Region of operation	Characteristic equation	V_{GS}	V_{DS}
Cut-off	$I_{DS}=0$	$<V_{TH}$	-
Linear or triode	$I_{DS} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)$	$>V_{TH}$	$<V_{GS}- V_{TH}$
Saturation	$I_{DS} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS})$	$>V_{TH}$	$>V_{GS}- V_{TH}$
Weak inversion	$I_{DS} = I_0 \cdot e^{\frac{V_{GS}}{n \cdot Vt}}$	$\cong V_{TH}$	>0 V



PMOS





Region of operation	Characteristic equation	V_{SG}	V_{SD}
Cut-off	$I_{SD}=0$	$>V_{TH}$	-
Linear or triode	$I_{SD} = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{SG} + V_{TH} - \frac{V_{SD}}{2}\right) \cdot V_{SD}$	$<V_{TH}$	$>V_{SG}+ V_{TH}$
Saturation	$I_{SD} = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{SG} + V_{TH})^2 \cdot (1 + \lambda \cdot V_{SD})$	$<V_{TH}$	$<V_{SG}+ V_{TH}$
Weak inversion	$I_{SD} = I_0 \cdot e^{\frac{V_{SG}}{n \cdot Vt}}$	$\cong V_{TH}$	<0 V

- cut-off;
- linear or triode;
- saturation;
- weak inversion.

NMOS	PMOS
I_{DS}	$\rightarrow I_{SD}$
V_{GS}	$\rightarrow V_{SG}$
V_{DS}	$\rightarrow V_{SD}$
V_{TH}	$\rightarrow -V_{TH}$
μ_n	$\rightarrow \mu_p$

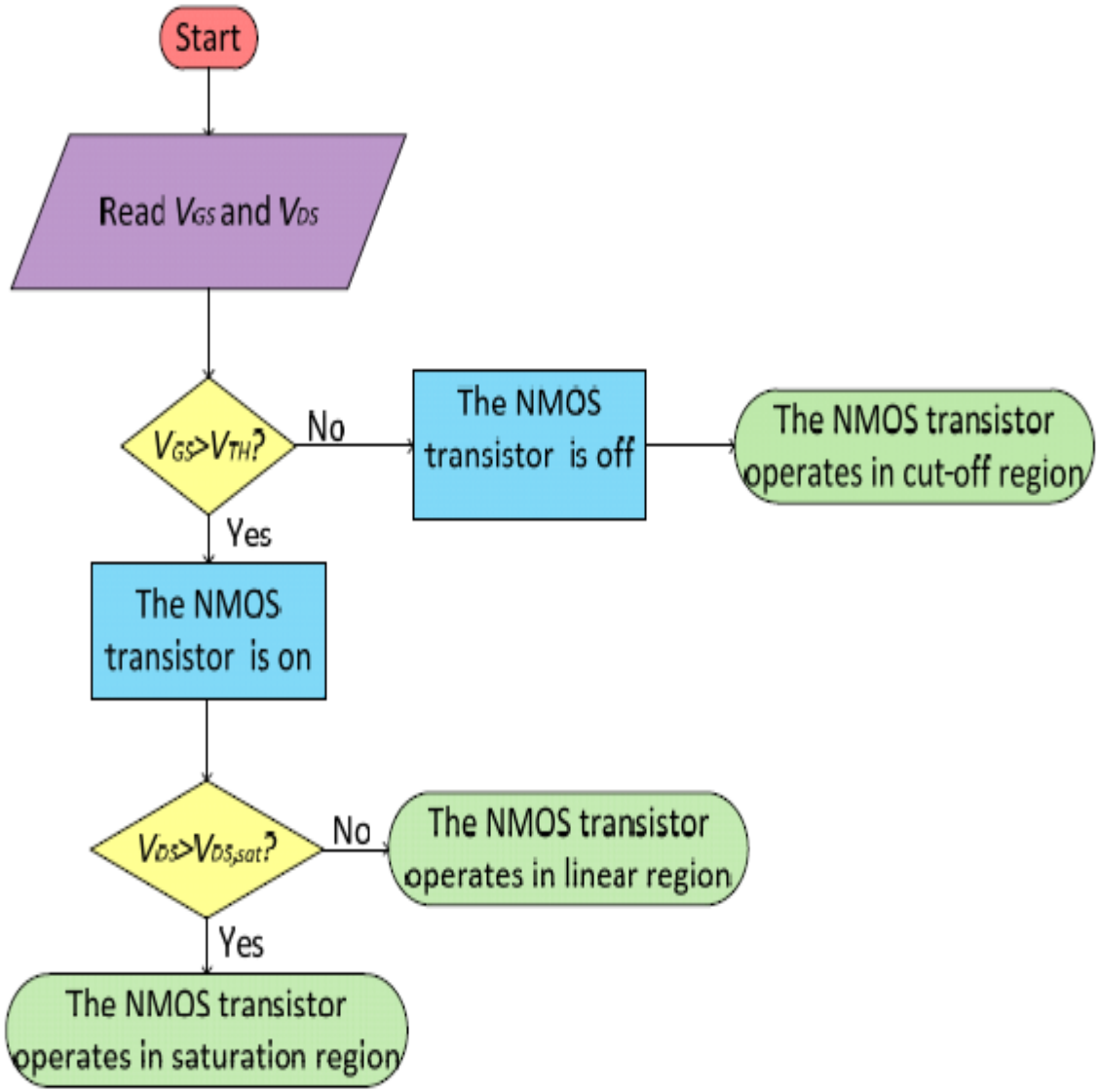
Region of operation	Characteristic equation	$\lvert V_{GS}\rvert$	$\lvert V_{DS}\rvert$
Cut-off	$\lvert I_{DS}\rvert=0$	$<\lvert V_{TH}\rvert$	-
Linear or triode	$\lvert I_{DS}\rvert = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(\lvert V_{GS}\rvert - \lvert V_{TH}\rvert - \frac{\lvert V_{DS}\rvert}{2}\right) \cdot \lvert V_{DS}\rvert$	$>\lvert V_{TH}\rvert$	$<\lvert V_{GS}\rvert - \lvert V_{TH}\rvert$
Saturation	$\lvert I_{DS}\rvert = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (\lvert V_{GS}\rvert - \lvert V_{TH}\rvert)^2 \cdot (1 + \lambda \cdot \lvert V_{DS}\rvert)$	$>\lvert V_{TH}\rvert$	$>\lvert V_{GS}\rvert - \lvert V_{TH}\rvert$
Weak inversion	$\lvert I_{DS}\rvert = I_0 \cdot e^{\frac{\lvert V_{GS}\rvert}{n \cdot Vt}}$	$\cong \lvert V_{TH}\rvert$	>0 V

$\frac{\mu_n}{\mu_p} \cong 2.5$

As in the PMOS transistor, I_{SD} is due to the drift of holes, the hole mobility, μ_p, has to be considered. The mobility of holes is quite less than electrons,

Therefore, a PMOS transistor has to be larger than a NMOS transistor in the same bias conditions in order to provide the same current.

NMOS transistor



Algorithm for solving a circuit including a MOS transistor by hand.