Chapter 3 MOSFET TRANSISTORS

Last year, more transistors were produced —and at a lower cost —than grains of rice.

- SEMI Annual Report'05

MOSFET transistors are the core of today's integrated circuits (ICs). Originally computers used mechanical switches to solve Boolean operations. But the smaller, faster, cooler MOSFET transistors allowed computers to evolve and dominate our lives. Our goal is to acquire the analytical ability and transistor insights that engineers use to design and troubleshoot digital ICs. Abundant examples and self-exercises will develop intuitive responses to transistor circuit operation. Chapter 3 is an important foundation for subsequent chapters.

3.1 Principles of Operation

The two major types of transistors are the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which will be our focus, and the Bipolar Junction Transistor (BJT). Digital integrated circuits almost exclusively use the MOSFET while the BJT has application in analog electronics. Transistors differ from passive resistor, capacitor, inductor, and diode elements in that MOSFET transistor output current and voltage characteristics vary with the voltage on a control terminal. Transistors have three terminals concerned with signal transmission while passive elements have two terminals.

Figure 3-1a sketches a MOSFET transistor. The bottom rectangular block of material is the silicon substrate often referred to as the bulk. There are four electronically active regions that are marked: *gate* (G), *source* (S), and *drain* (D), and the *bulk* terminal (B) to which the gate, drain, and source voltages are typically referenced. The rectangular gate region lies on top of the bulk separated by a thin silicon oxide dielectric with thickness T_{OX}. Two other important dimensions are the transistor gate length and width. The drain and source regions are embedded in the substrate but have an opposite doping to the substrate.

There are two types of MOSFET transistors, the *n*MOS transistor and the *p*MOS transistor, that differ in the polarity of carriers responsible for transistor current. The charged carriers are holes in *p*MOS transistors and electrons in *n*MOS transistors. Figure 3-1b shows symbols commonly used for MOSFETs where the bulk terminal is either labeled (B) or implied (not drawn).

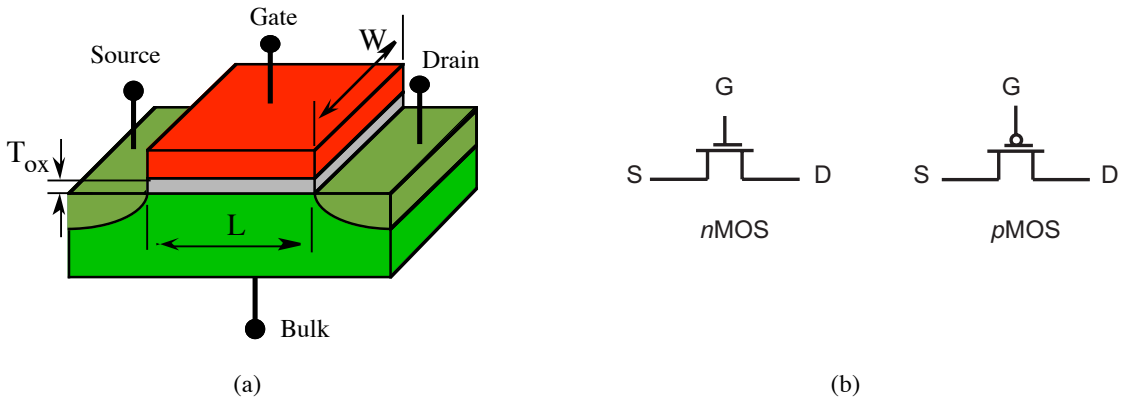


Fig. 3-1. (a) MOS structure (b) Symbols used at the circuit level.

3.1.1 The MOSFET as a Digital Switch

A simple description treats the MOSFET transistor as a switch. The gate terminal is analogous to the light switch on the wall. When the gate has a high voltage, the transistor closes like a wall switch, and the drain and source terminals are electrically connected. Just as a light switch requires a certain force to activate, the transistor gate terminal needs a certain voltage level to switch and connect the drain and source terminals. This voltage is called the *transistor threshold voltage* V_t and is a fixed voltage for *n*MOS and for *p*MOS devices in a given fabrication process.

An ideal transistor has zero ohms between the drain and source when it is in the ON-state and infinite resistance between these terminals in the OFF-state. The ideal device should also switch between ON and OFF-states with a zero delay time as soon as the control variable changes state. Figure 3-2 shows a switch, a resistor, and a 2 V battery. When the mechanical switch closes, V_{logic} = 0 V which is logic-0. When the switch is open V_{logic} = 2 V which is a logic-1 state. If we replace the mechanical switch with the transistor, then the same logic states appear when the gate terminal turns the transistor ON and OFF. A *p*MOS transistor acts similarly as a switch. This transistor principle exists in all logic gates we will study.

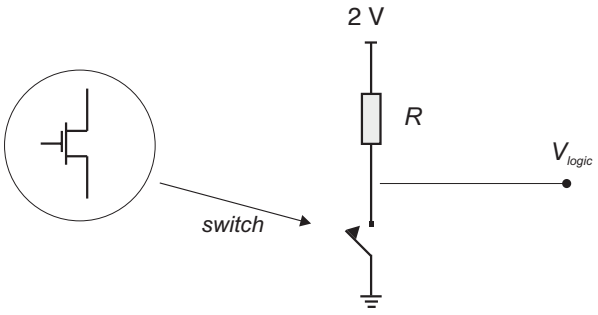


Fig. 3-2. A transistor modeled as a switch.

3.1.2 Physical Structure of MOSFETs

MOS transistor construction begins with a lightly doped host crystalline substrate structure. *n*MOS substrates are doped with *p*-doped silicon, while the *p*MOS substrates use *n*-doped silicon. Figure 3-1 shows the transistor thin oxide (T_{ox}) that electrically isolates the gate terminal from the semiconductor crystalline structures underneath. The gate oxide is made of oxidized silicon forming a non-crystalline, amorphous SiO_2. The gate oxide thickness (T_{ox}) typically ranges from near 15 Å to 100 Å (1 Å = 1 Angstrom = 10^{-10} m). SiO_2 molecules are about 3.2 Å in diameter so that this vital dimension is now a few molecular layers thick. The purpose of the SiO_2 dielectric is to allow an electric field generated by the gate voltage to influence the amount of charge passing between the drain and source. A thinner gate oxide allows the electric field gate to better control the device state and allows faster transistors. The thin gate oxide has sometimes been referred to as the beating heart of the transistor.

Figure 3-3 shows *n*MOS and *p*MOS transistor structures. The *n*MOS transistor has a *p*-doped silicon substrate with *n*-doping for the drain and source. *p*MOS transistors have a complementary structure with an *n*-doped silicon bulk and *p*-doped drain and source regions. The gate region above the thin oxide dielectric is constructed with polysilicon in both transistors. Polysilicon is made of many small silicon crystals. The region between the drain and source just under the gate oxide is called the *channel*, and is where charge conduction takes place. The electronic distinction between the two transistors is that electrons are the channel current in the *n*MOS transistor, and holes are the channel current in the *p*MOS transistor. Since drain and source dopants are opposite to the substrate (bulk), they form *pn* junction diodes that are either reverse or zero biased in normal operation (Fig. 3-3).

(a) *n*MOS transistor (b) *p*MOS transistor

Fig. 3-3. Relative doping and equivalent electrical connections between device terminals for (a) *n*MOS and (b) *p*MOS transistor.

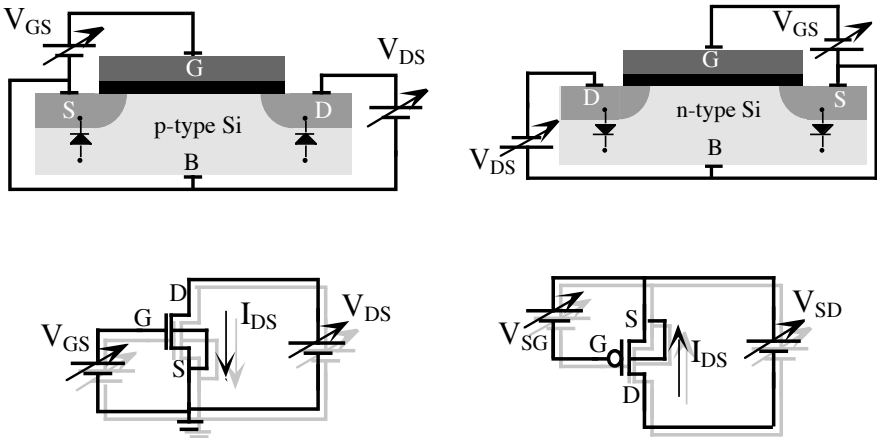
The distance from the drain to the source is a geometrical parameter called the *channel length* (*L*) and the lateral dimension is the transistor *channel width* (*W*) (Fig. 3-1a). Transistor length and width are parameters set by the circuit designer and process engineer. The width to length ratio (*W*/*L*) is linearly related to the drain current capability of the transistor. A wider transistor will pass more current. The gate is the control terminal, while the source provides electron or hole charge carriers that empty into the channel and are collected by the drain.

Other parameters, such as the transistor oxide thickness, threshold voltage, and doping levels depend on the fabrication process and cannot be changed by design. These are technology parameters set by the process and device engineers.

3.1.3 MOS Transistor Operation: a Descriptive Approach

Transistors must have exact terminal voltage polarities to operate (Fig. 3-4). The bulk or substrate of *n*MOS (*p*MOS) transistors must always be connected to the lower (higher) voltage that is the reference terminal. The bulk is usually connected to ground for an *n*MOSFET, and the bulk of a *p*MOSFET is connected to the power supply voltage. We will assume that the bulk and source terminals are shorted to simplify the description. The positive current convention in an *n*MOS

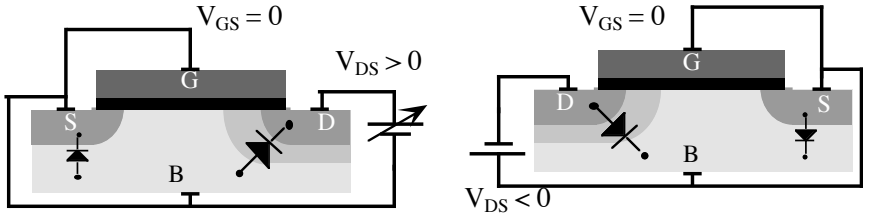
(*p*MOS) device is from the drain (source) to the source (drain), and is referred to as I_{DS} or simply I_D since drain and source current are equal. When a voltage is applied to the drain terminal, the drain current depends on the voltage applied to the gate control terminal. V_{GS}, V_{DS} and I_{DS} are negative values for *p*MOS transistors for reasons explained shortly.



(a) *n*MOS (b) *p*MOS

Fig. 3-4. Normal biasing (a) *n*MOS and (b) *p*MOS.

A channel of free carriers requires a minimum gate to source threshold voltage to induce a sheet of mobile charge. If V_{GS} is zero in an *n*MOS device, then there are no free charges between the drain and source and an applied drain voltage reverse-biases the drain-bulk diode (Fig. 3-5). As a result there is no current when $V_{GS} = 0$ for *n*MOS devices (the same for *p*MOS). This is the OFF, or non-conducting state of the transistor.

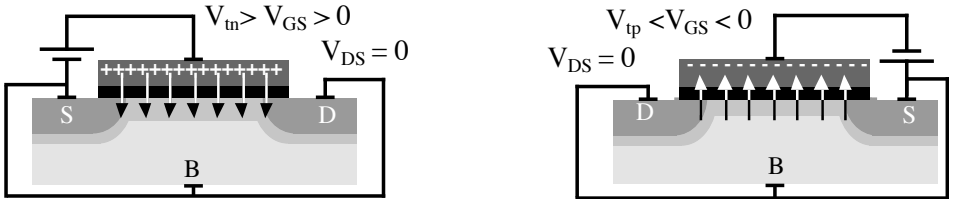


(a) *n*MOS (b) *p*MOS

Fig. 3-5. When the gate-source voltage is zero, the drain-source voltage prevents current from the drain to the source.

We will begin the analysis with the source, drain, and substrate all at 0 V. Then when the gate voltage of an *n*MOS (*p*MOS) transistor is slightly increased (decreased) a vertical electric field exists between the gate and the substrate across the oxide. In *n*MOS (*p*MOS) transistors, the holes (electrons) of the *p*-type (*n*-type) substrate close to the silicon-oxide interface initially "feel repelled" in this electrical field, and move away from the interface. As a result, a depletion region

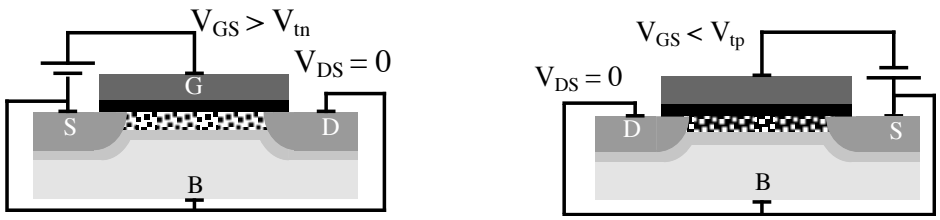
forms beneath the oxide interface for this small gate voltage (Fig. 3-6). The depletion region contains no mobile carriers, so the application of a drain voltage provides no drain current for this low V_{GS}.



(a) *n*MOS (b) *p*MOS

Fig. 3-6. (a) Deplete the *n*MOS channel of holes with small positive values of gate-source voltage, and (b) Deplete the *p*MOS channel of electrons with small negative values of gate-source voltage.

When the gate voltage of the *n*MOS (*p*MOS) device is further increased (decreased), the strong vertical electric field attracts *minority carriers* (electrons in the *n*MOS and holes in the *p*MOS device) from the bulk toward the gate. These minority carriers are attracted to the gate, but the silicon dioxide insulator stops them, and the electrons (holes) accumulate at the silicon to oxide dielectric interface. These carriers form a minority carrier inversion region or conducting channel that can be viewed as a "short-circuit" between the drain and source regions (Figure 3-7. When $V_D = V_S$ and $I_D = 0$, then the channel carrier distribution is uniform along the device.



(a) *n*MOS (b) *p*MOS

Fig. 3-7. Creating the conducting channel for (a) *n*MOS and (b) *p*MOS transistors.

The threshold voltage of an *n*MOS transistor V_{tn} is positive, while V_{tp} is negative for a *p*MOS transistor. An *n*MOS (*p*MOS) transistor has a conducting channel when the gate-source voltage is greater than (less than) the threshold voltage, i.e., $V_{GS} > V_{tn}$ ($V_{GS} < V_{tp}$). The gate of the *p*MOS transistor must be negative with respect to the source and substrate in order to attract a sheet of holes to the SiO_2 surface.

When the channel forms in the *n*MOS (*p*MOS) transistor, a positive (negative) drain voltage with respect to the source creates a horizontal electric field moving the electrons (holes) toward the drain forming a positive (negative) drain current coming into the transistor. The positive current convention is used for electron and hole current, but in both cases electrons are the actual charge carriers. If the channel horizontal electric field is of the same order or smaller than the vertical thin oxide field, then the inversion channel remains almost uniform along the device length. This continuous carrier profile from drain to source puts the transistor in a bias state that is equivalently

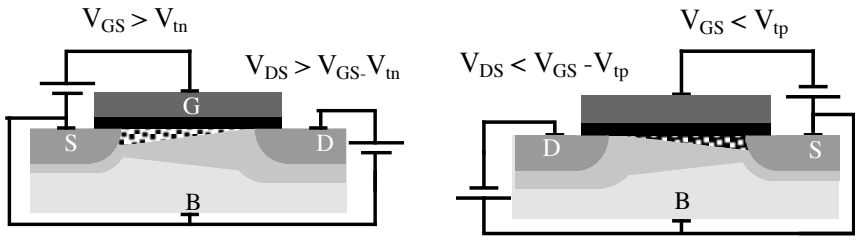
called either the *non-saturated, linear, or ohmic bias state*. The drain and source are effectively short-circuited. This happens when

$$\begin{aligned} V_{GS} &> V_{DS} + V_{tn} \qquad n\text{MOS transistor} \\ V_{GS} &< V_{DS} + V_{tp} \qquad p\text{MOS transistor} \end{aligned} \tag{3-1}$$

Drain current is linearly related to drain-source voltage over small intervals in the linear bias state. These equations state that when the gate to drain oxide voltage is itself greater than the threshold, then a continuous carrier profile exists across the whole channel. Accept these equations for now, and later Eqs (3-1) will be derived.

But if the *n*MOS drain voltage increases beyond the limit of Eq. (3-1) so that $V_{GS} < V_{DS} + V_{tn}$, then the horizontal electric field becomes stronger than the vertical field at the drain end, creating an asymmetry of the channel carrier inversion distribution shown in Fig. 3-8. If the drain voltage rises while the gate voltage remains the same, then V_{GD} can go below the threshold voltage in the drain region. There can be no carrier inversion at the drain-gate oxide region, so the inverted portion of the channel retracts from the drain, and no longer "touches" this terminal. The pinched-off portion of the channel forms a depletion region with a high electric field. The *n*-drain and *p*-bulk form a *pn* junction. When this happens the inversion channel is said to be "*pinched-off*" and the device is in the *saturation region*.

The asymmetric electron distribution in this saturation bias for the *n*MOS transistor is shown in Fig. 3-8a. Channel inversion cannot take place in the drain region when the gate to drain voltage is less than threshold. Figure 3-8b shows the hole inversion channel profile for a *p*MOS transistor that is described later in the chapter. Although there are no inversion charges at the drain end of the channel, the drain region is still electrically active. Carriers leave the source and move under the force of the horizontal field. Once they arrive at the pinchoff point of the channel, they travel from that point to the drain driven by the high electric field of the depletion region.



(a) *n*MOS (b) *p*MOS

Fig. 3-8. Channel pinchoff for (a) *n*MOS and (b) *p*MOS transistor devices.

The *pinchoff point* is the channel location that varies with changes in bias voltages. The drain-channel region forms a reversed bias *pn* junction with a high electric field depletion region. Charges ejected from the high electric field depletion region enter the drain and are ejected from the drain terminal from a reverse bias *pn* junction (drain to substrate). The high impedance current ejection forms a current source, which is a property of the saturated bias state.

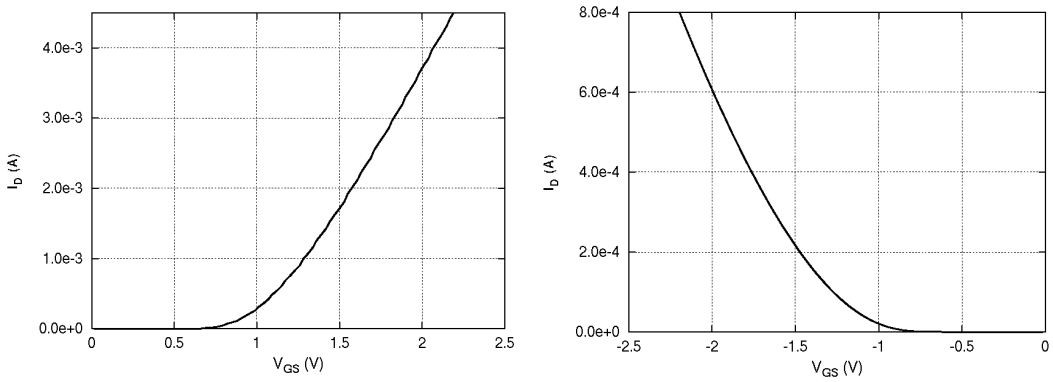
CMOS transistors use all three bias states described here: OFF-state, saturated-state, and the linear-state (ohmic, non-saturated). We will next look at curves illustrating MOS transistor parameters, and learn the analytical equations that predict and analyze transistor behavior. It is important to

work through all examples and exercises. It is instructive to return to this transistor description after acquiring skill in transistor circuit analysis.

3.1.4 MOSFET Input Characteristics

MOS transistors cannot be described with a single current-voltage curve as are diodes and resistors. MOSFETs have four terminals and need two sets of current-voltage curves to be characterized; the input characteristic and the output characteristic. The input characteristic relates drain current response to the input gate-source driving voltage. Since the gate terminal is electrically isolated from the remaining terminals (drain, source, and bulk), the gate current is essentially zero, so that gate current is not part of device characteristics. The input characteristic curve can locate the gate voltage at which the transistor passes current and leaves the OFF-state. This is the device threshold voltage.

Figure 3-9 shows measured input characteristics for an *n*MOS and *p*MOS transistor with a small 0.1 V potential across their drain to source terminals. The transistors are in their non-saturated bias states. As V_{GS} increases for the *n*MOS transistor in Fig. 3-9a, the threshold voltage is reached where drain current elevates. For V_{GS} between 0 V and 0.7 V, I_D is nearly zero indicating that the equivalent resistance between the drain and source terminals is extremely high. Once V_{GS} reaches 0.7 V, the current increases rapidly with V_{GS} indicating that the equivalent resistance at the drain decreases with increasing gate-source voltage. Therefore, the threshold voltage of the *n*MOS transistor is about $V_{tn} \approx 0.7$ V. When a transistor turns on and current moves through a load, then voltage changes occur in a circuit that translate into logic levels.



(a) (b)

Fig. 3-9. Measured input characteristics (I_D vs. V_{GS}) for (a) *n*MOS transistor (b) *p*MOS transistor.

The *p*MOS transistor input characteristic in Fig. 3-9b is analogous to the *n*MOS transistor except the I_D and V_{GS} polarities are reversed. V_{DS} is negative ($V_{DS} \approx -0.1$ V). Additionally, the gate is at a voltage lower than the source terminal voltage to attract holes to the channel surface. The threshold voltage of the *p*MOS device in Fig. 3-9b is $V_{tp} \approx -0.8$ V.

*3.1.5 n*MOS *Transistor Output Characteristics and Circuit Analysis*

MOS transistor output characteristics plot I_D versus V_{DS} for several values of V_{GS}. Figure 3-10 shows this family of curves measurement for an *n*MOS transistor. Two conduction states are

distinguished when the device is ON: the saturated state and the non-saturated state. The saturated curve is the flat portion and defines the *saturation region*. For $V_{GS} < V_{DS} + V_{tn}$, the *n*MOS device is conducting and I_D is independent of V_{DS}. For $V_{GS} > V_{DS} + V_{tn}$, the transistor is in the *non-saturation region* and the curve is a half parabola. When the transistor is OFF ($V_{GS} < V_{tn}$), then I_D is zero for any V_{DS} value.

The boundary of the saturation/non-saturation bias states is a point seen for each curve in Fig. 3-10 as the intersection of the straight line of the saturated region with the quadratic curve of the non-saturated region. This intersection point occurs at the channel pinchoff voltage called V_{DSAT}. The diamond symbol marks the pinchoff voltage V_{DSAT} for each value of V_{GS}. V_{DSAT} is defined as the minimum drain-source voltage that is required to keep the transistor in saturation for a given V_{GS}. In the non-saturated state, the drain current initially increases almost linearly from the origin before bending in a parabolic response. Thus the name ohmic or linear for the non-saturated region.

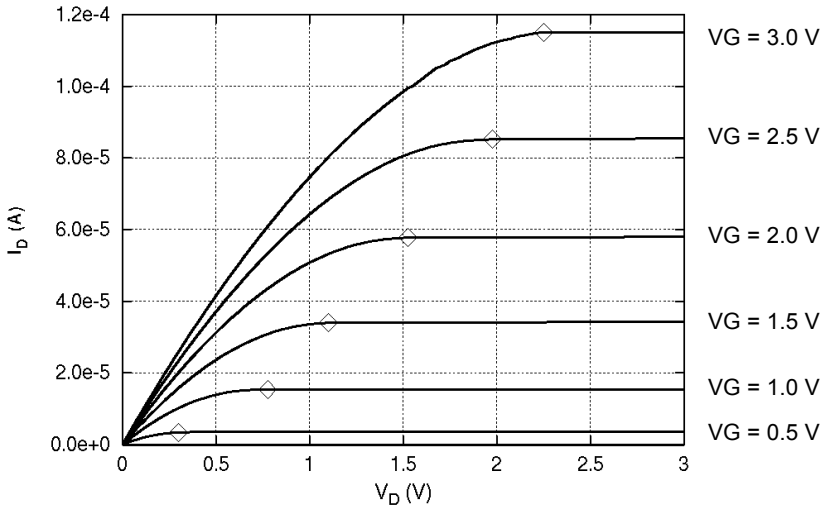


Fig. 3-10. *n*MOS transistor output characteristics as family of curves. The diamond symbol marks the pinchoff voltage V_{DSAT}.

The drain current in saturation is virtually independent of V_{DS} and the transistor acts as a current source. This is because there is no carrier inversion at the drain region of the channel. Carriers are pulled into the high electric field of the drain/substrate *pn* junction and ejected out of the drain terminal. A near constant current is driven from the transistor no matter the drain to source voltage. *p*MOS transistor I_D versus V_{DS} curves have a shape similar to that in Figure 3-10, but the voltage and current polarities are negative to account for hole inversion and drain current that enters the transistor (*p*MOS device curves are shown later).

We next develop skills with the equations that predict voltages and currents in a transistor for any point in the family of curves in Fig. 3-10. MOS equations can be derived by calculating the amount of charge in the channel at each point, and integrating this expression from the drain to the source. This procedure is found in several books [Nea03, Pie96, Tsi99], and leads to equations for the drain current in the saturated and linear states (Eqs (3-2) and (3-3)).

$$I_D = \frac{\mu_n \varepsilon_{ox}}{2T_{ox}} \frac{W}{L} \left(V_{GS} - V_{tn} \right)^2 \qquad \text{(Saturated State)} \qquad (3\text{-}2)$$

$$I_D = \frac{\mu_n \varepsilon_{ox}}{2T_{ox}} \frac{W}{L}\left[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2\right] \qquad \text{(Non-Saturated State)} \qquad (3\text{-}3)$$

μ_n is the electron mobility, ε_{ox} is the thin oxide (SiO_2) dielectric constant, T_{ox} is transistor thin oxide thickness, and W and L are transistor effective gate width and length. A constant K is introduced to indicate the current drive strength of the transistor as

$$K = \frac{\mu \varepsilon_{ox}}{2T_{ox}} \qquad (3\text{-}4)$$

We often use K_n as a current drive symbol for *n*MOS transistors. If all constants are known, then Eq. (3-2) can predict I_D for any value of V_{GS} in the saturated region, and Eq. (3-3) can predict I_D in the non-saturated region if V_{GS} and V_{DS} are specified. Eq. (3-2) is a square law relation between I_D and V_{GS} that is independent of V_{DS}. It is a flat line for a given V_{GS} since there is no V_{DS} term in Eq. (3-2). These two MOS equations allow calculations of transistor voltages and current, and their use although more complicated, is similar to what the linear Ohm's Law does for resistors, i.e. Eq. (3-2 and 3-3) relate transistor current to applied voltage.

The saturated and non-saturated states intersect at V_{DSAT} where either equation describes the current and voltage relations. We can solve for this important bias condition where the saturated and non-saturated states intersect (V_{DSAT}). This knowledge is essential for solving problems that follow. Figure 3-11 plots three parabolas of Eq. (3-3) at V_{GS} = 2.0 V, 1.6 V, and 1.2 V. Only the left-hand side of the parabolas is used to predict the curves in Fig. 3-10, but the parabola also has a right hand side. The dotted lines on the right hand side of the curves are part of the continuous solution to the parabola, but are electronically invalid as examples will show.

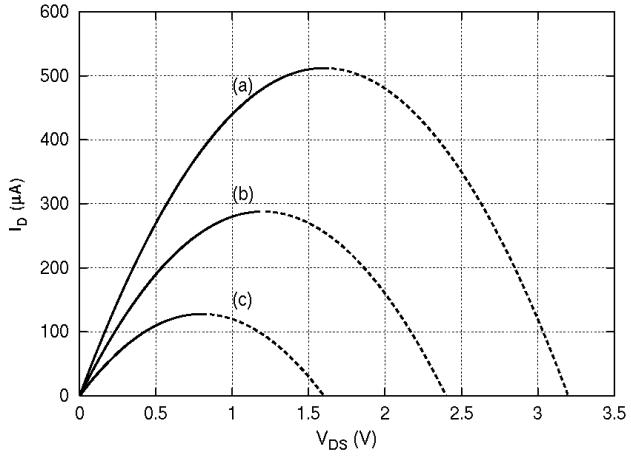


Fig. 3-11. Plot of parabola of non-saturation state equation (Eq. (3-3)). K_n = 100 μA/V^2, V_{tn} = 0.4 V, and W/L = 2. The solid line is the valid region, but dotted line is not. (a) V_{GS} = 2.0 V, (b) V_{GS} = 1.6 V, (c) V_{GS} = 1.2 V.

The midpoint at zero slope defines the useful upper region of Eq. (3-3), and also defines the boundary between the saturated and non-saturated bias states. We can define the boundary bias condition by differentiating Eq. (3-3) with respect to V_{DS}, setting the expression to zero, and then solving for the conditions. Eq. (3-5) shows the derivative of Eq. (3-3) set to zero

$$\frac{dI_D}{dV_{DS}} = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}\left[2\left(V_{GS} - V_{tn}\right) - 2V_{DS}\right] = 0 \tag{3-5}$$

Terms cancel giving the important bias condition at the transition between saturation and non-saturation states as

$$V_{GS} = V_{DS} + V_{tn} \tag{3-6}$$

This equation holds for each of the intersection points in Fig. 3-11 denoted at the peak of each curve. Eq. (3-6) can be extended to define the *n*MOS saturated bias condition

$$V_{GS} < V_{DS} + V_t \quad \text{or} \quad V_{DS} > V_{GS} - V_t \tag{3-7}$$

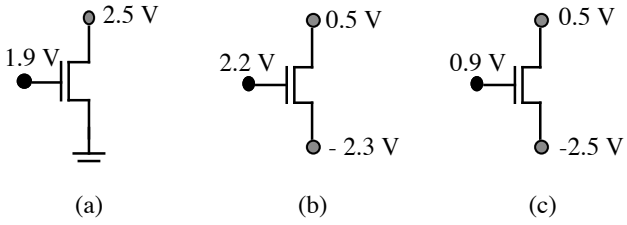
and the *n*MOS non-saturated condition

$$V_{GS} > V_{DS} + V_t \quad \text{or} \quad V_{DS} < V_{GS} - V_t \tag{3-8}$$

These relations hold for V_{GS} greater than the threshold voltage. The transistor must be ON.

Example 3.1

Determine the bias state for the three circuit conditions if V_{tn} = 0.4 V. The source voltage is always lower than the drain voltage in an *n*MOS transistor. First identify the correct terminals.



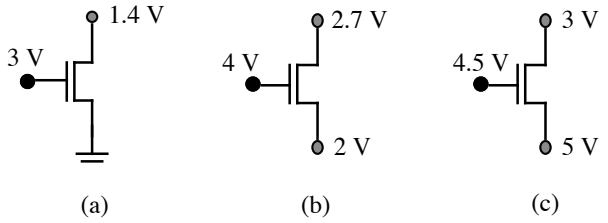
(a) V_{GS} = 1.9 V, V_{DS} = 2.5 V, V_{tn} = 0.4 V, therefore V_{GS} = 1.9 V < 2.5 V + 0.4 V = 2.9 V. Eq. (3-7) is satisfied, and the transistor is in the saturated state described by Eq. (3-2).

(b) $V_{GS} = V_G - V_S$ = 2.2 V – (– 2.3 V) = 4.5 V. $V_{DS} = V_D - V_S$ = 0.5 V – (–2.3) = 2.8 V. Therefore, V_{GS} = 4.5 V > 2.8 V + 0.4 V = 3.2 V. Eq. (3-8) is satisfied, and the transistor is in non-saturation.

(c) $V_{GS} = V_G - V_S$ = 0.9 V – (– 2.5 V) = 3.4 V. $V_{DS} = V_D - V_S$ = 0.5 V – (– 2.5 V) = 3 V. Therefore, V_{GS} = 3.4 V = $V_{DS} + V_{tn}$ = 3 V + 0.4 V = 3.4 V, and the transistor is at the boundary of the saturated and non-saturated regions. Either Eq. (3-2) or (3-3) can be used to calculate I_D.

Self-Exercise 3.1

Determine the bias state for the three circuit conditions if $V_{tn} = 0.4$ V.

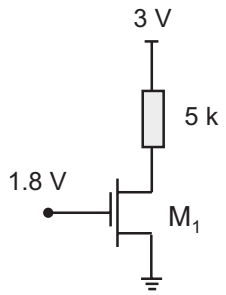


After determining the proper bias state equations in Example 3.1 and Exercise 3.1, you may check part of your work by referring to the *n*MOS transistor family of curves in Fig. 3-10. Find the coordinates in the example and exercise, and verify that the bias state is correct. A series of examples and exercises with the *n*MOS transistor will reinforce these important relations.

Example 3.2

Calculate I_D and V_{DS} if $K_n = 100\ \mu$A/V^2, $V_{tn} = 0.6$ V, and $W/L = 3$ for transistor M1.

The bias state of M1 is not known so we must initially assume one of the two states, then solve for bias voltages and check for consistency against that transistor bias condition. Initially, assume that the transistor is in the saturated state so that



$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tn})^2 = K_n\frac{W}{L}(V_{GS} - V_{tn})^2$$
$$= (100\ \mu A)\ (3)\ (1.5 - 0.6)^2$$
$$= 243\,\mu\text{A}$$

Using Kirchhoff's Voltage Law (KVL)

$$V_{DS} = V_{DD} - I_D R$$
$$= 5 - (243\text{ mA})(15\text{ k}\Omega)$$
$$= 1.355\,\text{V}$$

We assumed that the transistor was in saturation, so we must check the result to see if that is true. For saturation

$$V_{GS} < V_{DS} + V_{tn}$$
$$1.5\,V < 1.355\,V + 0.6\,V$$

so the transistor is in saturation, and our assumption and answers are correct.

Example 3.3

Repeat Example 3.2 above finding I_D and V_{DS} if $V_G = 1.8$ V.

Assume a transistor saturated state and

$$\begin{aligned} I_D &= (100\ \mu\text{A})\,(3)\,(1.8-0.6)^2 \\ &= 432\ \mu\text{A} \\ V_{DS} &= 5-(675\ \mu\text{A})(15\ \text{k}\Omega) \\ &= -1.48\ \text{V} \end{aligned}$$

This value for V_{DS} is clearly not reasonable since there are no negative potentials in the circuit. Also the bias check gives

$$\begin{aligned} &V_{GS} > V_{DS} + V_{tn} \\ &1.8\,\text{V} > -1.48\,\text{V} + 0.6\,\text{V} \end{aligned}$$

The initial saturated state assumption was wrong, so we repeat the analysis using the non-saturated state assumption

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}\left[2(V_{GS}-V_{tn})V_{DS}-V_{DS}^2\right]$$

$$\begin{aligned} I_D &= K_n\frac{W}{L}\left[2(V_{GS}-V_{tn})V_{DS}-V_{DS}^2\right] \\ &= (100\ \mu\text{A})\ (3)\left[2(1.8-0.6)V_{DS}-V_{DS}^2\right] \\ &= 300\ \mu\text{A}\left[2.4V_{DS}-V_{DS}^2\right] \end{aligned}$$

This equation has two unknowns, so another equation must be found. We will use the KVL

$$V_{DD} = I_D R + V_{DS}$$

$$I_D = \frac{(V_{DD}-V_{DS})}{R}$$

$$I_D = \frac{(5-V_{DS})}{15\ \text{k}\Omega}$$

The two equations can be equated to their I_D solution giving

$$\frac{(5-V_{DS})}{15\ \text{k}\Omega} = 300\ \mu\text{A}\left[2.4\ \text{V}_{DS}-V_{DS}^2\right]$$

The solutions are $V_{DS} = 0.531$ V, 2.09 V

The valid solution is $V_{DS} = 0.531$ V, since this satisfies the non-saturation condition that was used in its solution.

$$\begin{aligned} &V_{GS} > V_{DS} + V_{tn} \\ &1.8\,\text{V} > 0.531\text{V} + 0.6\,\text{V} \end{aligned}$$

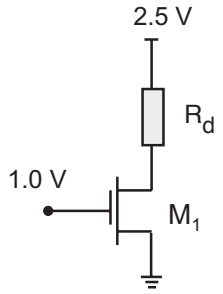
and

$$I_D = \frac{(V_{DD} - V_{DS})}{15\ \text{k}\Omega}$$
$$= \frac{(5\ \text{V} - 0.531\ \text{V})}{15\ \text{k}\Omega}$$
$$= 298\ \mu\text{A}$$

Example 3.4

What value of R_d will drive transistor M1 just at non-saturation if $K_n = 50\ \mu\text{A/V}^2$, $V_{tn} = 0.4$ V, and $W/L = 10$? Since the bias state is at the boundary, either Eq. (3-2) or (3-3) can be used. Eq. (3-2) is simpler so

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tn})^2 = K_n\frac{W}{L}(V_{GS} - V_{tn})^2$$
$$= (50\ \mu\text{A})\ (10)\ (1.0 - 0.4)^2$$
$$= 180\ \mu\text{A}$$



The bias boundary condition

$$V_{GS} = V_{DS} + V_{tn}$$

becomes

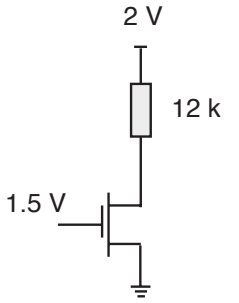
$$V_G - V_S = V_D - V_S + V_{tn}$$
$$V_D = V_G - V_{tn}$$
$$V_D = 1.0\text{V} - 0.4\text{V} = 0.6\text{V}$$

Then

$$R_d = \frac{V_{DD} - V_D}{I_D}$$
$$= \frac{2.5 - 0.6}{180\ \mu\text{A}}$$
$$= 10.56\ \text{k}\Omega$$

Self-Exercise 3.2

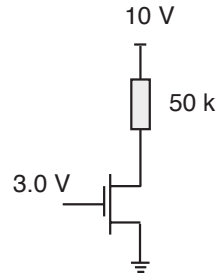
Find I_D and V_D and verify the bias state consistency of your choice of MOS drain current model for $V_{tn} = 0.5$ V, $K_n = 25\ \mu\text{A/V}^2$, $W/L = 2$.



Answer: $I_D = 50\ \mu$A, $V_D = 1.4$ V

Self-Exercise 3.3

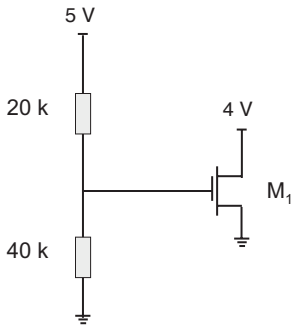
Find I_D and V_D and verify the bias state consistency of your choice of MOS drain current model for $V_{tn} = 0.5$ V, $K_n = 25\ \mu A/V^2$, $W/L = 3$.



Answer: $I_D = 188.7\ \mu A$, $V_D = 0.562$ **V**

Self-Exercise 3.4

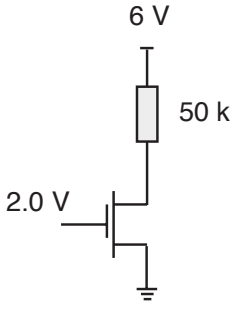
Calculate V_{GS} and give the correct bias state for transistor M1 where $V_{tn} = 0.5$ V.



Answer: $V_{GS} = 3.333$ V

Self-Exercise 3.5

Find I_D and V_D and verify the bias state consistency of your choice of MOS drain current model for $V_{tn} = 0.5$ V, $K_n = 50\ \mu A/V^2$, $W/L = 2$



Answer: $V_D = 0.434$ V, $I_D = 111.3\ \mu A$

3.1.6 pMOS Transistor Output Characteristics and Circuit Analysis

*p*MOS transistor analysis is similar to the *n*MOS transistor with a major exception; care must be taken with the polarities of the drain current and node voltages. The *p*MOS transistor major carrier is the hole that emanates from the source into the channel, and exits the drain terminal as a negative network convention current. The gate to source threshold voltage V_{tp} needed to invert an *n*-substrate is negative with respect to the source to attract holes to the channel surface. The equations to model the *p*MOS transistor in saturation and non-saturation have a form similar to the *n*MOS device, but have polarity considerations. We will choose a *p*MOS transistor equation form that is close to the *n*MOS transistor equations. Eqs (3-9) and (3-10) describe the current *magnitude* of a *p*MOS device.

$$I_D = \frac{\mu\varepsilon_{0x}}{2T_{0x}}\frac{W}{L}\left(V_{GS} - V_{tp}\right)^2 \qquad \text{(Saturated State)} \tag{3-9}$$

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}\left[\,2\left(V_{GS} - V_{tp}\right)V_{DS} - V_{DS}^2\right] \quad \text{(Non-saturated State)} \tag{3-10}$$

The form of the equations is identical to the *n*MOS transistor, but V_{GS}, V_{DS} and V_{tp} have negative values for the *p*MOS transistor. Figure 3-12 shows a measured *p*MOS transistor family of curves with all voltages given with respect to the source. The plot is shown in quadrant-1 even though the drain current and voltage are negative. This is an author's choice made to retain similarity to the *n*MOS transistor family of curves and to minimize confusion with signal polarity.

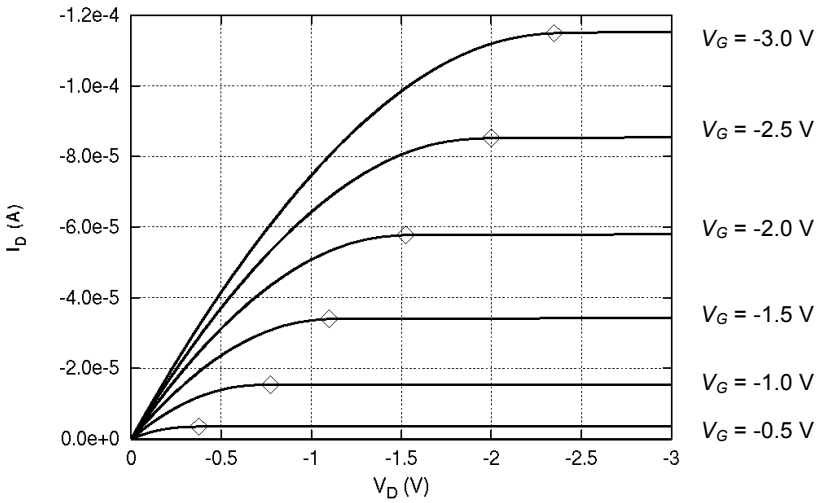


Fig. 3-12. *p*MOS transistor family of curves. The diamond symbol marks the pinchoff voltage V_{DSAT}.

The boundary of the bias states is again found by differentiating Eq. (3-10), setting the result to zero, and solving for the conditions to get

$$V_{GS} = V_{DS} + V_{tp} \tag{3-11}$$

The condition for *p*MOS transistor saturation is

$$V_{GS} > V_{DS} + V_{tp} \quad \text{or} \quad V_{DS} < V_{GS} - V_{tp} \tag{3-12}$$

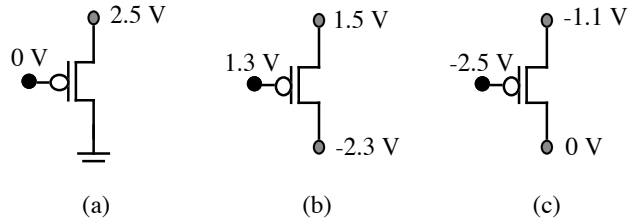
and the condition for *p*MOS transistor non-saturation is

$$V_{GS} < V_{DS} + V_{tp} \quad \text{or} \quad V_{DS} > V_{GS} - V_{tp} \tag{3-13}$$

An example will illustrate the polarity issues.

Example 3.5

Determine the bias state for the *p*MOS transistors where V_{tp} = -0.4 V. It is helpful with *p*MOS transistors to first identify and label the source and drain terminals. The source terminal in a *p*MOS transistor has a higher voltage than the drain terminal.



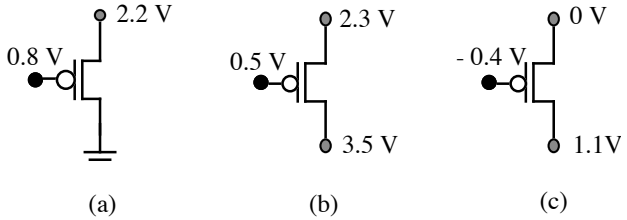
(a) V_{GS} = – 2.5 V, V_{DS} = – 2.5 V, therefore $V_{GS} > V_{DS} + V_{tp}$, or – 2.5 V > – 2.5 + (– 0.4) V, so the transistor is in saturation.

(b) The gate voltage is not sufficiently more negative than either drain or source terminal to invert holes at the oxide interface, so that the transistor is in the off-state.

(c) V_{GS} = – 2.5 – (– 1.1) = – 1.4 V, V_{DS} = 0 – (– 1.1) = 1.1 V. What is wrong? The gate voltage is sufficiently negative to turn on the transistor, but the source to drain voltage is negative. Holes must leave the source and flow to the drain, but they can't under this conclusion. The answer is that the drain terminal with a lower voltage is on the top and the source on the bottom so that V_{GS} = – 2.5 – 0 = – 2.5 V, V_{DS} = – 1.1 – 0 = – 1.1 V. Therefore $V_{GS} > V_{DS} + V_{tp}$, or – 2.5 V < – 1.1 + (– 0.4) V, so the transistor is in non-saturation. *The pMOS source terminal always has a higher voltage than the drain terminal.*

Self-Exercise 3.6

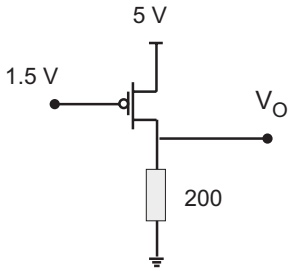
Give the correct bias state for the three *p*MOS transistors where $V_{tp} = -0.4$ V.



After determining the proper bias state equations in Example 3.5 and Self-Exercise 3.6, you may check your work by referring to the *p*MOS transistor family of curves in Fig. 3-12. Find the coordinates in the example and exercise, and verify that the bias state is correct. A series of examples and exercises with the *p*MOS transistor will reinforce these important relations.

Example 3.6

Calculate I_D and V_{DS} for $V_{tp} = -1.0$ V, $K_p = 100\ \mu$A/ V^2, and $W/L = 4$.



Assume a saturated bias state

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tp})^2 = 100\mu A(4)\left[-3.5 - (-1)\right]^2$$
$$= 2.5 \text{ mA}$$
$$V_0 = I_D(200\ \Omega) = (2.5\ m\text{A})\ (200\ \Omega) = 0.5 \text{ V}$$

then

$$V_{DS} = 0.5\ V - 5\ V = -4.5\ V$$

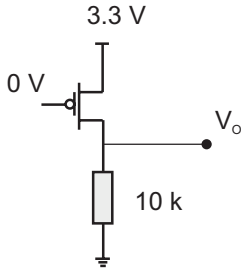
The bias state check is

$$V_{GS} > V_{DS} + V_{tp}$$
$$-3.5 > -4.5 + (-1.0)$$

so the transistor is in saturated bias state and the solutions are correct.

Example 3.7

Calculate I_D and V_{DS} for $V_{tp} = -0.6$ V, $Kp = 80\ \mu$A/ V^2, and $W/L = 10$.



Assume a saturated bias state

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tp})^2 = 80\ \mu\text{A}(10)\left[-3.3 - (-0.6)\right]^2$$
$$= 5.832\ \text{mA}$$

then

$$V_0 = I_D(10\ \text{k}\Omega) = (5.832\ \text{mA})\ (10\ \text{k}\Omega)$$
$$= 58.32\ \text{V}$$

This voltage is beyond the power supply value, and is not possible. The saturated state assumption was wrong, so we must start again using the non-saturated state equation

$$I_D = -\frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}\left[2(V_{GS} - V_{tp})V_{DS} - V_{DS}^2\right] = -80\ \mu\text{A}(10)\left[2(-3.3 + 0.6)V_{DS} - V_{DS}^2\right]$$

Another equation is required so using the KVL (Ohm's Law here)

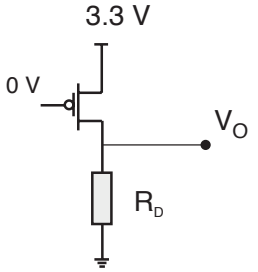
$$I_D = \frac{V_D}{R_d} = \frac{V_{DD} + V_{DS}}{10\ \text{k}\Omega}$$
$$= \frac{3.3 + V_{DS}}{10\ \text{k}\Omega} = 80\ \mu\text{A}(10)\left[2(-3.3 + 0.6)V_{DS} - V_{DS}^2\right]$$

The two solutions are: $V_{DS} = -75.70$ mV and -5.450 V. The valid solution is $V_{DS} = -75.70$ mV. Therefore

$$V_O = V_{DD} - V_{SD} = 3.3\ \text{V} - 75.70\ \text{mV} = 3.224\ \text{V}$$

Self-Exercise 3.7

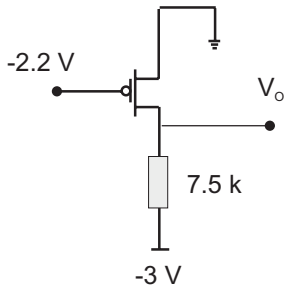
What value of Rd will raise VO to half of the power supply voltage (i.e., $V_O = 0.5\ V_{DD}$). Vtp = –0.7 V, $K_p = 80\ \mu$A/V^2, and $W/L = 5$.



Answer: $R_d = 704.5\ \Omega$

Self-Exercise 3.8

Find I_D and V_O for V_{tp} = –0.6 V, K_p = 20 μA/V^2, and W/L = 3.



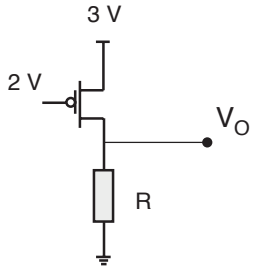
Answer: I_D = 153.6 μA, V_O = -1.848 V

Self-Exercise 3.9

V_{tp} = – 0.6 V, and K_p = 75 μA/V^2, and W/L = 2

(a) What value of R will place the transistor on the boundary between saturation and non-saturated?

(b) If R doubles its value, what are I_D and V_o?



Answer:

(a) R = 108.3 kΩ

(b) V_D = 2.867 V

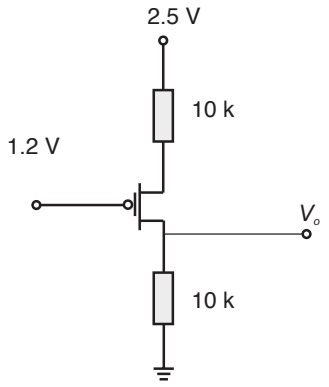
I_D = 13.3 μA

3.2 MOSFET with Source and Drain Resistors

We close the MOSFET analysis with circuits having source and drain resistors and either single or dual power supplies. This is circuit is often called a phase splitter since the waveforms at the source and drain nodes are 180^o out of phase. If the resistors are equal then the voltages changes are equal at the source and drain nodes as the gate voltage changes.

Example 3.8

Calculate I_D, V_{DS}, and verify the assumed bias state of transistor M1 for $V_{tp} = -0.4$ V, $K_p = 60\ \mu$A/V^2, and $W/L = 2$.



Assume a saturated bias state and

$$I_D = \frac{\mu\varepsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tp})^2$$

Since V_{GS} is not known, we must search for another expression to supplement this equation.

We can use the KVL statement

$$\begin{aligned} V_{GS} &= 1.2 - (V_{DD} - (I_D R_S)) \\ &= 1.2 - 2.5 + I_D R_S \\ &= -1.3 + (10\ \text{k}\Omega) I_D \end{aligned}$$

We substitute this into the saturated current expression to get

$$\begin{aligned} I_D &= 60\ \mu\text{A}(2)\left[-1.3 + (10\ \text{k}\Omega) I_D + 0.4\right]^2 \\ &= 120\ \mu\text{A}\left[-0.9 + (10\ \text{k}\Omega) I_D\right]^2 \end{aligned}$$

This quadratic equation in I_D gives solutions

$$I_D = 35.56\ \mu\text{A},\ 227.8\ \mu\text{A}$$

The valid solution is $I_D = 35.66\ \mu$A, since the other solution for I_D when multiplied by the sum of the two resistors gives a voltage greater than the power supply. V_{DS} is then

$$\begin{aligned} V_{DS} &= I_D(20\ \text{k}\Omega) - V_{DD} \\ &= (35.56\ \mu\text{A})\ (20\ \text{k}\Omega) - 2.5\ \text{V} \\ &= -1.789\ \text{V} \end{aligned}$$

and

$$\begin{aligned} V_S = V_{DD} - I_D R_S &= 2.5 - (35.56\mu A)\ (10k\Omega) \\ &= 2.144\ V \end{aligned}$$

Verify the bias state

$$V_{GS} = V_G - V_S = 1.2 - 2.144 = -0.944\ \text{V}$$

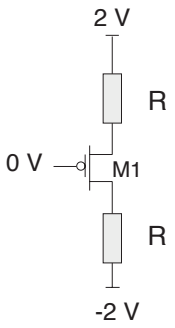
Transistor M1 is in saturation since

$$\begin{aligned} V_{GS} &> V_{DS} + V_{tp} \\ -0.944\,\text{V} &> -1.789\,\text{V} - 0.4\,\text{V} \end{aligned}$$

Self-Exercise. 3-10

The voltage drop across each of the two identical resistors and V_{DS} are equal. If V_{tp} = -0.5 V, K_p = 100 μA/V^2, and W/L = 2, find the value of the resistors. Note the negative -2 V power supply.

Answer: R = 239.0 kΩ



These many examples and exercises with MOS transistors have a purpose. These problems when combined with transistor family of curves plots should now allow you to think in terms of transistor reaction to its voltage environment. This is basic to transistor instruction. The techniques to solve these transistor-resistor problems should become reflexive.

3.3 Threshold Voltage in MOS Transistors

The bulk terminals are always connected to either GND (*n*MOS) or V_{DD} (*p*MOS). However, when *n*MOS (*p*MOS) transistors are stacked in series, the source terminal of the upper (lower) transistors is not connected to the bulk. A major effect is on the threshold voltage, and it is called the *body effect*.

Figure 3-13 shows a cross section of two *n*MOS and one *p*MOS transistors connected in series. All devices are constructed on the same *p*-type silicon substrate. Since *p*MOS transistors are formed on an *n*-type substrate, there must be a region of the circuit that is oppositely doped to the initial *p*-doped substrate. This region is called a *well*. The *p*-type substrate for *n*MOS transistors is connected to zero volts (or ground, GND) while the *n*-type well is connected to V_{DD}, since the *n*-well forms the bulk of the *p*MOS transistors.

The source of the *n*MOS device N_1 is connected to ground, so that V_{tn} for the previous equations is valid for this device. Transistor N_2 source is connected to the drain of N_1 to make a series connection. The source of transistor N_2 is not grounded, and it can acquire voltages close to V_{DD} while its substrate is connected to ground. Therefore the condition V_{SB} = 0 will not hold in some bias cases for transistor N_2.

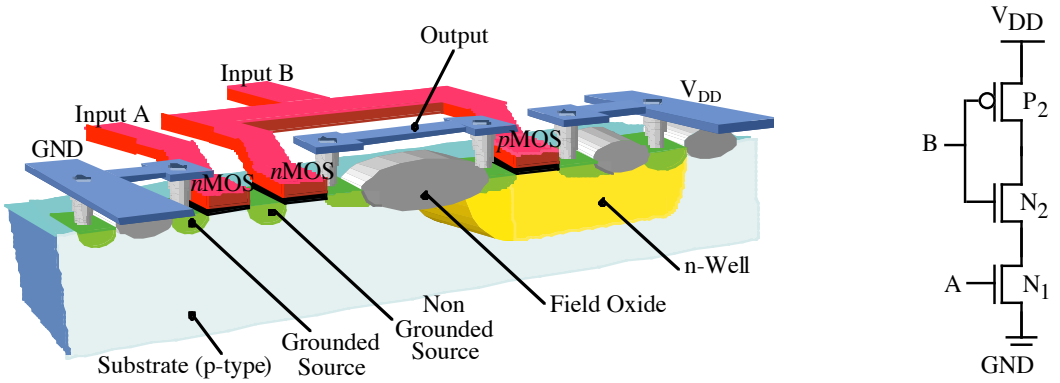


Fig. 3-13. (a) Structure for two series connected *n*MOS transistors and one *p*MOS transistor, (b) Circuit schematic.

When the source and substrate voltages differ, the gate-source voltage is not fully related to the vertical electric field responsible for creating the channel. The effect of the higher source voltage above the substrate for an *n*MOS transistor is to lower the electric field induced from the gate to attract carriers to the channel. The result is an effective elevation of the transistor threshold voltage. The threshold voltage can be estimated as

$$V_t = V_{to} \pm \gamma\left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right) \tag{3-14}$$

where

$$\gamma = \frac{\sqrt{2q \times N_A \times \varepsilon_{ox}}}{C_{ox}} \tag{3-15}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} = \frac{\varepsilon_r \varepsilon_0}{T_{ox}} = \frac{3.9\left(8.85 \times 10^{-14}\right)}{T_{ox}} = \frac{3.45 \times 10^{-13}}{T_{ox}}\left(\frac{\text{F}}{\text{cm}^2}\right) \tag{3-16}$$

$$\phi_F = -\left(\frac{kT}{q}\right)\ln\left[\frac{N_A}{n_i}\right] \tag{3-17}$$

V_{to} is the threshold voltage when the source and the substrate are at the same voltage, γ is the body-

effect coefficient parameter dependent on the technology, ϕ_F is the Fermi potential, and V_{SB} is the source-bulk voltage. The positive sign is used for *n*MOS transistors, and the negative sign for *p*MOS transistors. N_A is the *p*-substrate doping concentration. The Fermi potential is a semiconductor variable relating electron energy state distribution and temperature. A nominal calculation at room temperature (300K) for $N_A = 10^{16}$ cm^{-3} is $\phi_F \approx$ -0.35 V. ϕ_F is negative in *n*MOS transistors and positive in *p*MOS transistors. V_{SB} is positive in *n*MOS transistors and negative in *p*MOS transistors. We will examine only the *n*MOS transistor body effect.

When the source and substrate are tied together, $V_{SB} = 0$, and the threshold voltage is constant. The significance of the threshold body effect lies with certain circuit configurations whose transistor thresholds will be altered leading to changes in transistor delay time.

Example 3.9

(a) Calculate γ if substrate concentration is 3 x 10^{17}cm^{-3} and C_{ox} is 3.5 x 10^{-7} F/cm^2.

$$\gamma = \frac{\sqrt{2 \times \left(1.6 \times 10^{-19}\right)\left(3 \times 10^{17}\right)\left(3.45 \times 10^{-13}\right)}}{\left(3.5 \times 10^{-7}\right)} = 0.520\, V^{1/2}.$$

(b) Calculate V_t for this γ if V_{t0} is 0.55 V, the Fermi voltage is -0.45 V, and $V_{SB} = 0.5$ V.

$$V_t = 0.55 + 0.520\left(\sqrt{\left|-2 \times -0.45 + 0.5\right|} - \sqrt{\left|2 \times -0.45\right|}\right) = 0.672\, V$$

Self-Exercise 3.11

$V_{t0} = 0.5$ V, $V_t = 0.59$ V, $\Phi_F = -0.48$, $V_{SB} = 0.8$ V. What is γ?

Answer: $\gamma = 0.232\, V^{1/2}$

Self-Exercise 3.12

$V_{t0} = 0.5$ V, $V_t = 0.53$ V, $N_A = 10^{18}$, $\Phi_F = -0.48$, $V_{SB} = 0.8$ V.

(a) What is C_{ox}?

(b) What is T_{ox}?

Answer:

(a) $C_{ox} = 3.864 \times 10^{-6} \frac{\text{F}}{\text{cm}^2}$

(b) $T_{ox} = 1604$ Å

3.4 Conclusion

The transistor-resistor circuit analysis should become reflexive through the numerous problems in the chapter. Engineers intuitively think in these concepts when designing, debugging, and testing CMOS ICs. The body effect is an important alteration and must be understood. Chapter 5 will combine the *n*MOS and *p*MOS transistors to form the most fundamental logic gate called the inverter.

References

[Nea10] D. A. Neamen, Semiconductor Physics and Devices – Basic Principles, 3rd Ed., McGraw-Hill, 2010.

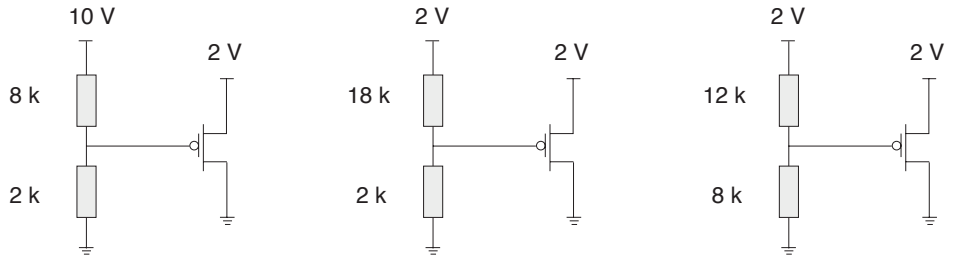
[Pie96] R. F. Pierret, *Semiconductor Device Fundamentals,* Addison-Wesley Pub. Co., 1996.

[Tsi03] Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd Edition, McGraw-Hill Co. Inc., 2003.

Exercises

nMOSFET Biasing and Current-Voltage Analysis

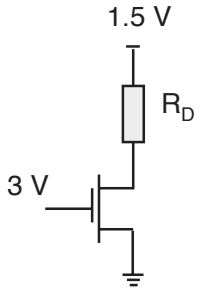
3.1. For the three circuits, (a) Give the transistor bias state, (b) Write the appropriate model equation, (c) Calculate I_D, where $W/L = 2$, $V_{tn} = 0.4$ V and $K_n = 200\ \mu A/V^2$.



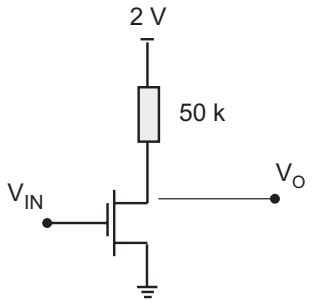
3.2. Given $K_n = 200\ \mu A/V^2$, $W/L = 4$, $V_{tn} = 0.5$ V, and $V_D = 0.8$ V. Find

(a) Drain current I_D

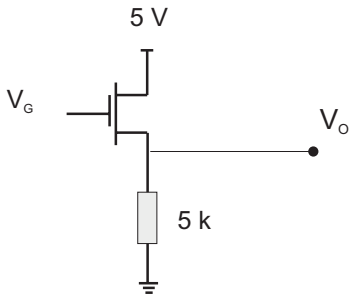
(b) Find the value of R_D to satisfy these constraints



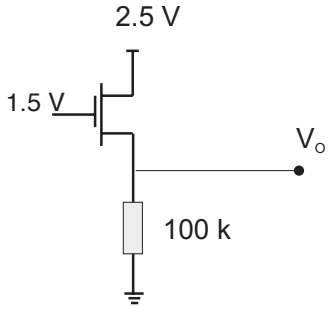
3.3. The transistor parameters in the circuit below are: $V_{tn} = 0.5$ V, $K_n = 75\ \mu A/V^2$, and $W/L = 4$. If $V_o = 1.2$ V, what is V_{IN}?



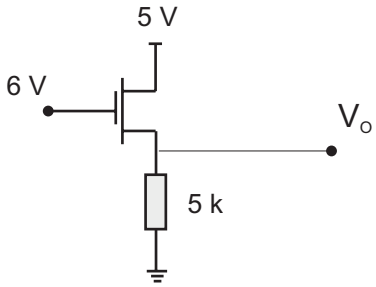
3.4. Calculate V_G so that $I_D = 200$ µA, given that if $V_{tn} = 0.8$ V and $K_n = 100$ µA/V^2, and $W/L = 4$.



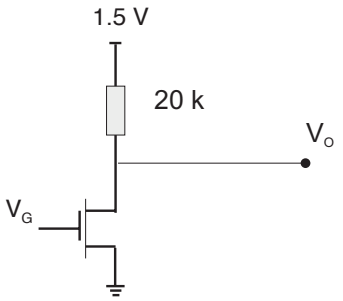
3.5. Given that $W/L = 3$, $V_{tn} = 0.6$ V and $K_n = 75$ µA/V^2.
Calculate V_O and I_D.



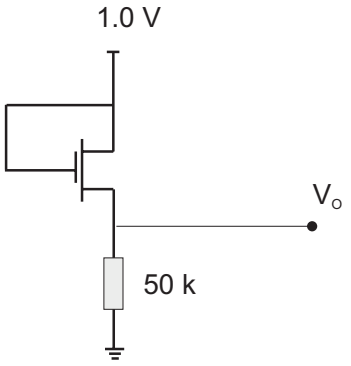
3.6. Given $V_{tn} = 0.8$ V, $K_n = 200$ µA/V^2, and $W/L = 4$.
Calculate V_O.



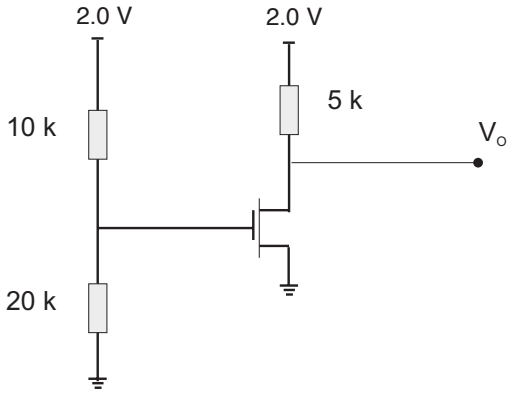
3.7. Given that $W/L = 2$, $V_{tn} = 0.4$ V and $K_n = 80$ µA/V^2.
What value of V_G sets $I_D = 50$ µA.



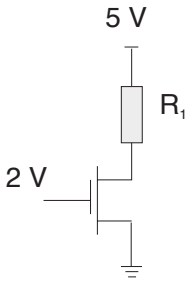
3.8. Given that $W/L = 5$, $V_{tn} = 0.25$ V and $K_n = 110\ \mu A/V^2$. Find V_O and I_D.



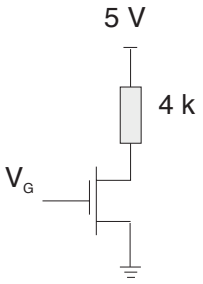
3.9. Given that $W/L = 20$, $V_{tn} = 0.5$ V and $K_n = 120\ \mu A/V^2$. Find V_O and I_D.



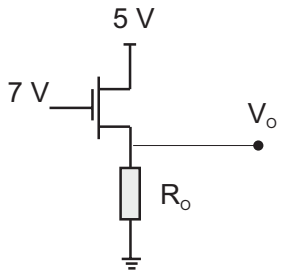
3.10. Given that $K_n = 250\ \mu A$, $V_{tn} = 0.5$ V, and $W/L = 3$. Find R_1 so that the transistor is on the saturated/non-saturated bias boundary.



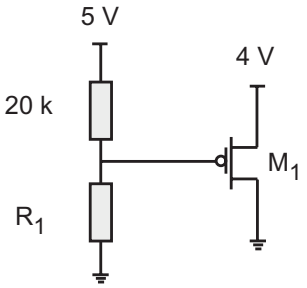
3.11. Given that $K_n = 250\ \mu A$, $V_{tn} = 0.5$ V, and $W/L = 3$. What V_G makes transistor biased at the saturated/non-saturated boundary.



3.12. Calculate R_O so that $V_O = 2.5$ V. Given: $K_n = 300\ \mu A/V^2$, $V_{tn} = 0.7$ V, and $W/L = 2$.



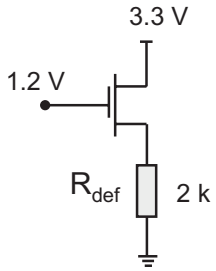
3.13. Adjust *R1* so that M1 is on the saturated/non-saturated border where $V_{tn} = 0.5$ V.



3.14. Transistors emit light from the drain depletion region when they are in the saturated bias state.

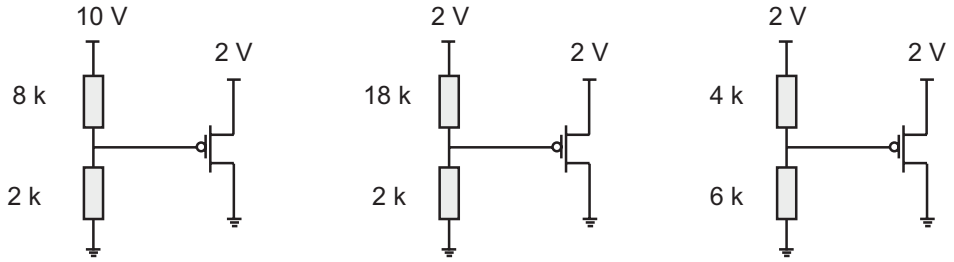
(a) Show whether this useful failure analysis technique will work for the circuit. $V_{tn} = 0.6$ V, $K_n = 75\ \mu A/V^2$, and $W/L = 2$.

(b) Find I_D, V_{GS}, and V_{DS}

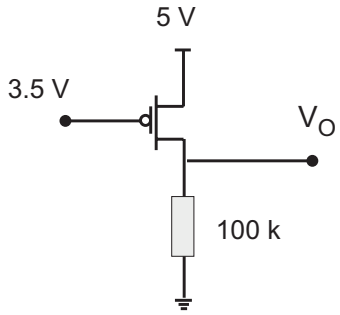


p MOSFET Biasing and Current-Voltage Analysis

3.15. For the three circuits, (a) Give the transistor bias state, (b) Write the appropriate model equation, (c) Calculate I_D, where $V_{tp} = -0.4$ V, $W/L = 4$, and $K_p = 100\ \mu A/V^2$. The *p*MOS source is higher voltage than drain.

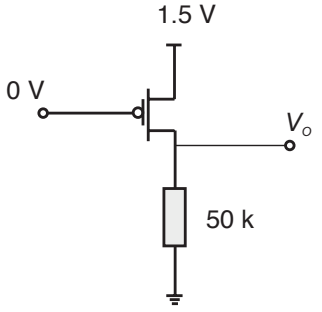


3.16. Calculate I_D and V_O for circuit where $V_{tp} = -0.8$ V, $K_p = 30\ \mu A/V^2$, and $W/L = 2$.

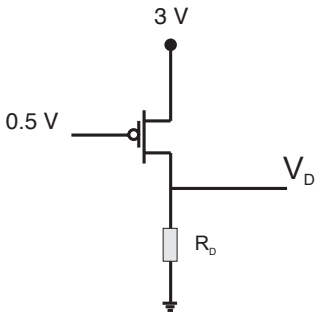


3.17. Repeat Problem 3.16 for $V_G = 1.5$ V

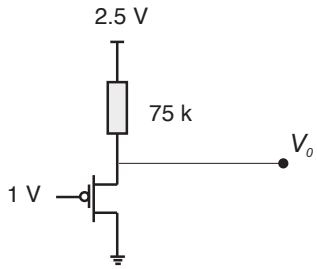
3.18. Given that $W/L = 5$, $V_{tp} = -0.4$ V and $K_p = 50\ \mu A/V^2$. Calculate V_O and I_D.



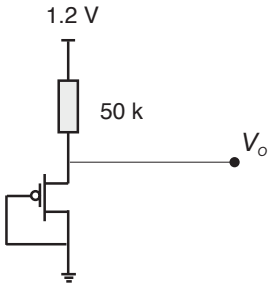
3.19. What value of R_D will place V_D = 1.5 V. Given: K_p = 25 μA/V^2, V_{tp} = -0.8 V, W/L = 3.



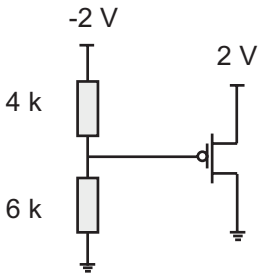
3.20. Given that W/L = 20, V_{tp} = -0.6 V and K_p = 30 μA/V^2. Calculate V_O and I_D.



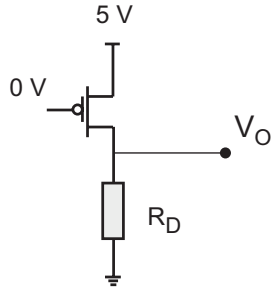
3.21. Given that W/L = 6, V_{tp} = -0.3 V and K_p = 40 μA/V^2. Calculate V_O and I_D.



3.22. V_{tp} = – 0.4 V, W/L = 4, and K_p = 100 μA/V^2. (a) Give the transistor bias state, (b) Calculate I_D.



3.23. Given $V_{tp} = -0.8$ V and $K_p = 75\ \mu A/V^2$. What is the required W/L ratio and what is R_D if M1 is to pass 0.25 A and keep $V_{SD} < 0.2$ V.

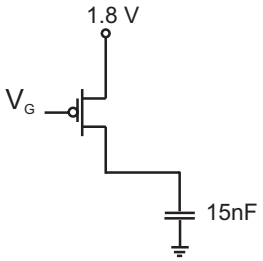


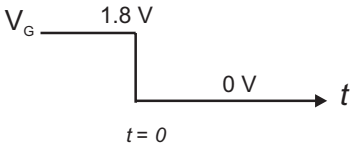
3.24. Given:

$K_p = 40\ \mu A/V^2$

$V_{tp} = -0.4$ V

$W/L = 5$





(a) The capacitor is initially uncharged at $t = 0$. At $t = 0^+$ the gate voltage has changed state from 1.8 V to 0 V. What is the initial surge of current at $t = 0^+$.

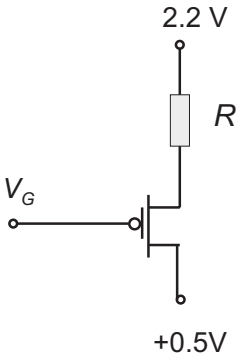
(b) At $t = \infty$ what is the bias state on the transistor?

(c) How much energy is dissipated in the charge and where does the heat loss occur?

3.25. $V_{tp} = -0.4$, $K_p = 50\ \mu A/V^2$, $W/L = 8$.

The transistor is biased at the sat/non-sat boundary.

The power in the resistor is 10 μW. What is the value of the resistor R ?

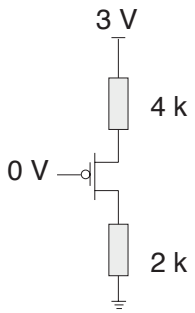


Two Resistor MOSFET Circuits

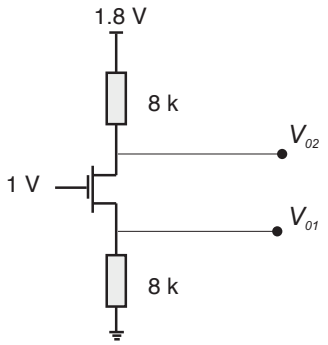
3.26. Given $V_{tp} = -0.6$ V and $K_p = 75\ \mu A/V^2$, and $W/L = 5$.

(a) Solve for source voltage V_s.

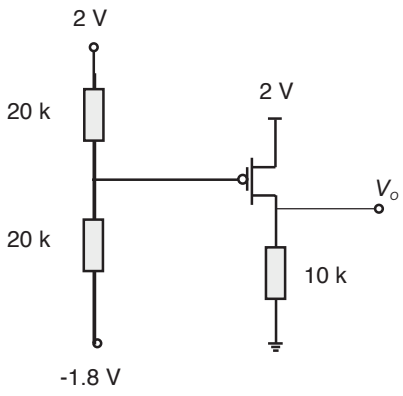
(b) Solve for drain voltage.



3.27. Given that $W/L = 4$, $V_{tn} = 0.4$ V and $K_p = 95\ \mu A/V^2$.
Calculate V_{o1}, V_{o2} and I_D.



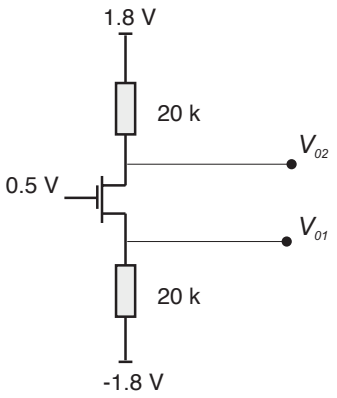
3.28. Given that $W/L = 8$, $V_{tp} = -0.5$ V and $K_p = \ \mu A/V^2$.
Calculate V_O and I_D.



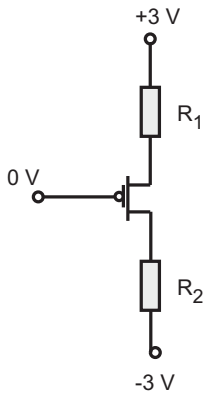
3.29. Given that $W/L = 4$, $V_{tn} = 0.4$ V and $K_p = 95$ μA/V^2. Calculate V_{o1}, V_{o2} and I_D. for

(a) $V_G = +0.5$ V

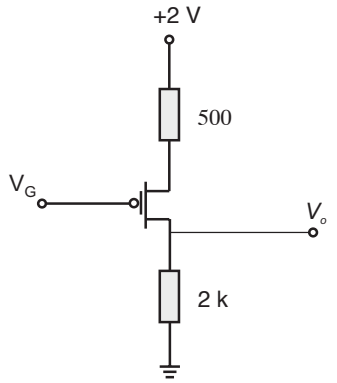
(b) $V_G = -0.3$ V



3.30. Given that $R_1 = R_2$, $W/L = 3$, $V_{tn} = 0.6$ V, and $K_n = 200$ μA/V^2, determine the resistance values so that $V_D = 1$ V and $V_S = -1$ V.



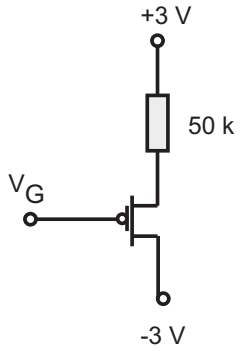
3.31. $V_{tp} = -0.5$ V, $W/L = 5$, $K_p = 50$ μA/V^2. Design a value for V_G such that $V_O = 0.3$ V.



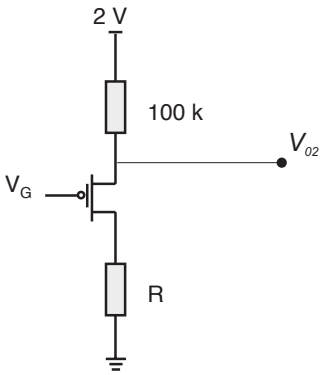
3.32. Given that V_{tp} = -0.6 V, K_p = 75 μA/V^2, and W/L = 4.

(a) What gate voltage will put the transistor at the saturated/non-saturated bias state boundary? Calculate V_S.

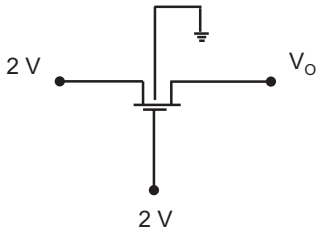
(b) Calculate the drain current.



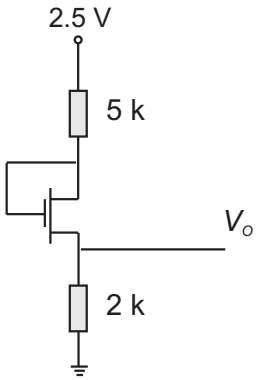
3.33. Given : V_{tp} = -0.6 V, K_p = 50 μA/V^2, and W/L = 3, and V_D = 0.8 V. If V_o = 1.2 V. What are R and V_G?



3.34. Given : V_{tp} = -0.6 V, K_p = 50 μA/V^2, and W/L = 3, and V_D = 0.8 V. If V_o = 1.2 V. What is R?

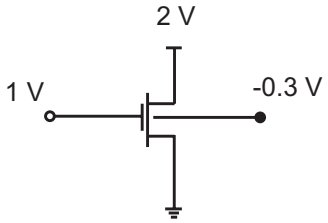


3.35. $K_n = 90\ \mu A/V^2$, $V_{tn} = 0.5$ V, W/L = 10. Calculate I_D and V_O.



Body Effect and Threshold Voltage

3.36. The *n*MOSFET has: $V_{tn0} = 0.5$ V, $K_n = 200\ \mu A/V^2$, $\phi_F = -0.35$ V, $W/L = 3$, and the body effect constant $\gamma = 0.1\ V^{1/2}$. The bulk voltage is at – 0.3 V with respect to the source. Calculate I_D.



3.37. An *n*MOSFET threshold voltage is measured as 0.62 V when it should be 0.60 V. A parasitic source to substrate voltage is suspected of raising V_{tn}. If $\gamma = 0.4$ and $\phi_F = 0.35$ V, what would the V_{BS} of this suspected mechanism?

3.38. $V_{t0} = 0.6$ V, $\gamma = 0.25$, and $\phi_F = 0.35$ V. Calculate V_O.