= ملاحظة مهمة :

التلخيص مش شامل ، في عدد من المحاضرات ماحضرتها أكتب فيها

+ اذا حد انتبه على أي غلط يبقه يعدل النوتس و اذا عندكم اشياء نضيفها بصي برضو.

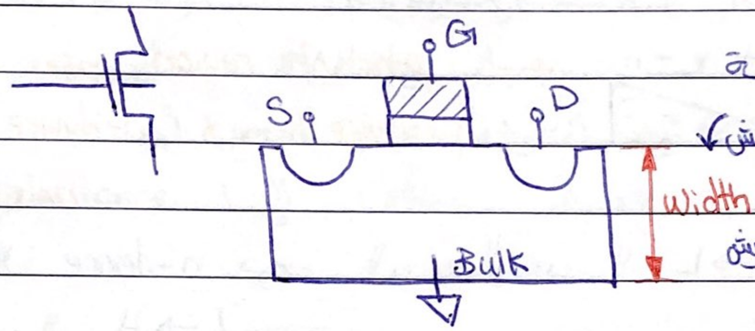
و شكرا .

Lec 4 : Cont

• ال Source بيرتبط مع الفولتج الأعلى و ال Drain مع الفولتج الأقل

• ال Bulk بيشبك على الجراوند فممكن ما نرسم التيرمنال الرابع.

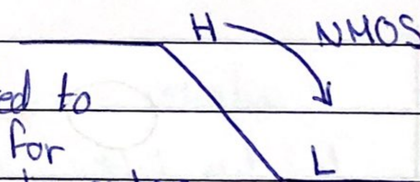
• في Capacitor بتولد بين ال gate و ال oxide.



في رسمة قبل مكانش الويدث هون أبصرليش

• Increasing V_T causes the device to be slower

• بتعامل مع ال device بس بيسكر السويتش كانه R. اللي هي بتتأثر على الوقت (تقليل V_T

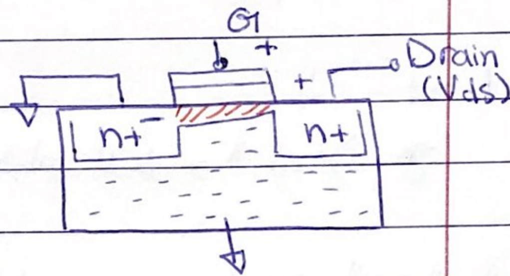


Related to R_{on} for the transistor

• برفع V_T عشان السويتش دو أقلع).

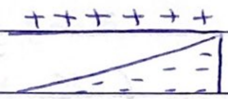
• for NMOS, when $V_{gs} > V_T$, $V_{DS} = 0$
↳ cutoff region (بعمل ليكج بور)

• when $V_{gs} - V_T > V_{ds} > 0$
↳ linear region



• ليش المنطقة الحمرة هيك منظرها ؟

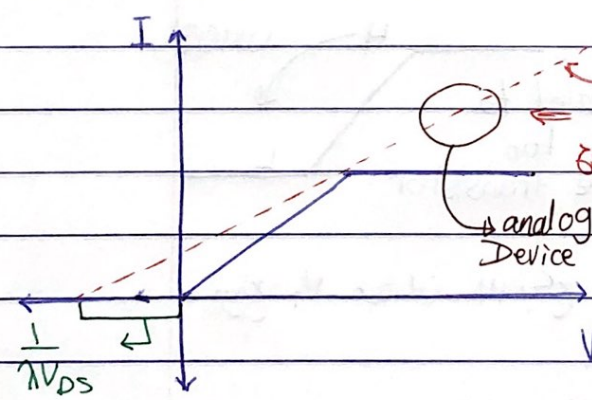
- ال gate بتجذب الالكترونات اللي بال Substrate و بتجذب الالكترونات بتعون ال Source فبصير المنظر هيك



← بس بصير pinchoff region بال n-device عكس ال p-device في holes.

• ال n-device بوخذ السيقنال من ال H → L ال p-device من ال L → H.

• We treat the device as constant current source in the saturation region.



slope = λ (عادة صغير)

مرات بصير هيك بس ارفع V_{DS} و بتعتمد على نوع الدارة.

بعتبره analog signal فلو بهم analog بشتغلوا بهاد ال region "مش موضوعنا"

If we consider CLM it exists, if not we don't use it

$$I = \mu \cdot \frac{W}{L}(V_{gs} - V_t)^2 \frac{(1 + \lambda V_{DS})}{2}$$

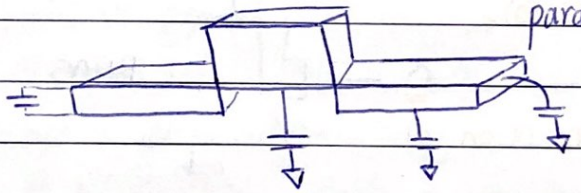
• النقطة اللي بتفصل بين ال Saturation وال linear region هي $V_{DS} = V_{GS} - V_T$

• شكله ال Ron باللينير بس "والله أعلم بس"

• ال cutoff فيها leakage current.

- ال Drain و ال Source بنعتبروا كانه ~~cutoff~~ فبضيف عندي منهم تحت ال gate عشان كمان ال length يتبع ال Device بقى.
- ال p-device أبطأ من ال n-device لأنه ال holes أبطأ من ال electrons.
- بنكبر ال p-device width عشان نسرعه و دليا" ال p أكبر من ال n عشان ال mobility تتساوى.
- كل ما تزيد الحرارة الجهاز بصير أبطأ.
- كل مادة في ال CMOS إلها capacitance.

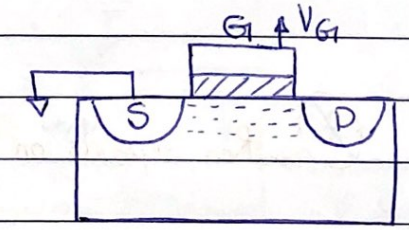
Lec 5:

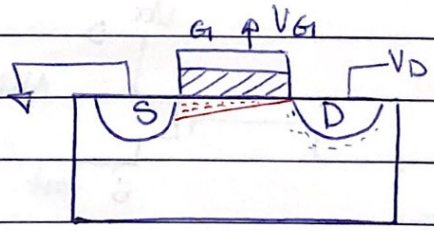


parasetic capacitance

- How to make the device more reliable?

لما تزيد الجهد على ال Drain بصير في Hot electrons





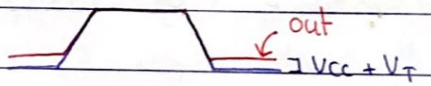
الشرح ورا

لما يرفع الـ V_D وتصير تساوي V_G بصير صفر تنافر بين الالكترون حوالين الـ D و اللي بيجوا من جهة الـ S ، بصير التنافر و الـ Channel بتصير أقل و الالكترون بتصير بتخلى الـ oxid اللي هو بنقول عنه pinch off

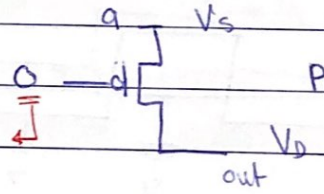
[channel length modulation] اللي هو بأثر على V_T و بيغيرها.

بس تنافر الالكترون مع بعض بتكسب طاقة و "it pinch off the oxide" التيار بصير أبطأ بس بقل الـ width اللي الالكترون بتمشي فيه الـ oxide أول بعدها بتوصل الـ terminal التاني

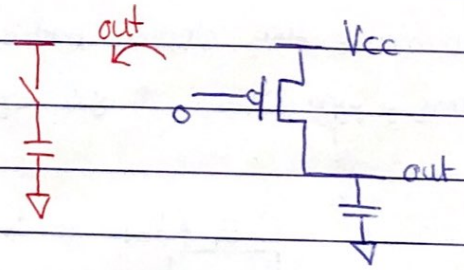
a Guess the output a



good (1) and poor (0)

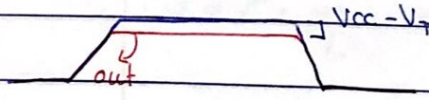


the device is on



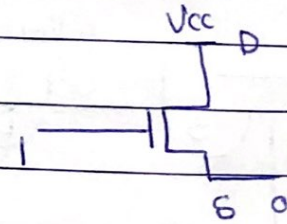
PMOS L → H

② Ron depends on the width



Poor (1) and good (0)

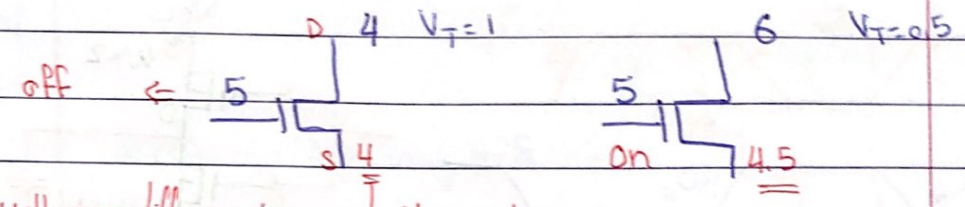
device is on



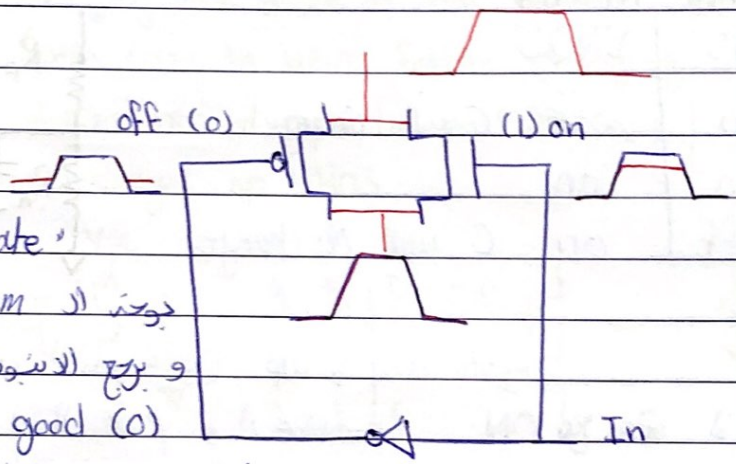
$V_{gs} = V_g - V_s > V_T$

$V_s < V_g - V_T$

أكبر قيمة ممكن تاخدها



Voltage difference بين Source ال , Drain ال ← Max value $V_{GT}-V_T$



"pass gate"

بوابة ال maximum من كل وحدة

و بترجع الاشارة زي ما هي

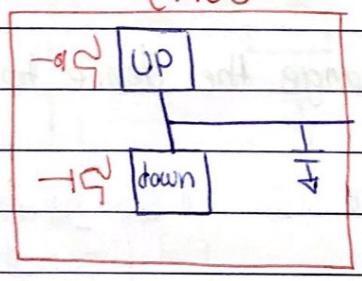
good (1) and good (0)

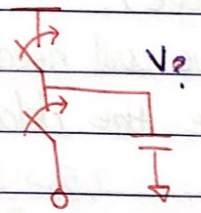
"When we want to pass data only"

بنشيك ع ال inverter ال output عشان تغير ال output ما يأثر

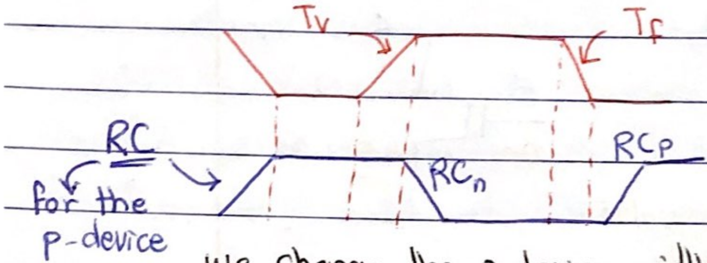
ع ال input (يعكس ال D و ال S)

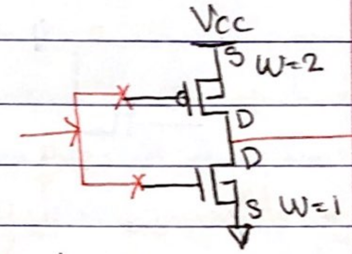
Lec 6.





V depends on the switches

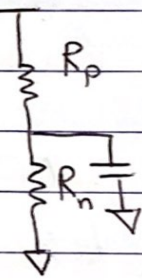


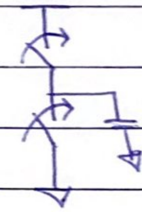


Invertor

we change the p-device width such that $R_P = R_n$

V_{in}	PMOS	NMOS	
0	on	off	C will charge
$0.5V_{cc}$	on	on	
V_{cc}	off	on	C will discharge





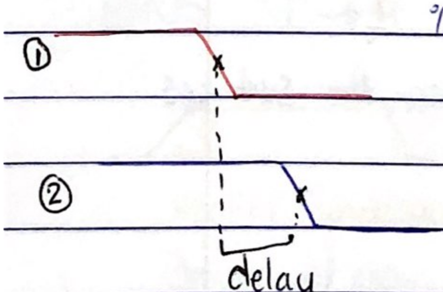
- بعرف النسبة بين wp و wn بالتجريب.
لو معنا ال p-device و ال n-device ON مع بعض اذا ال
capacitor مشحون بمر في I_{short} و اذا مش مشحون
بمشي التيار بمسارين

- changing C from 1nF to 2nF will increase the delay (slope).

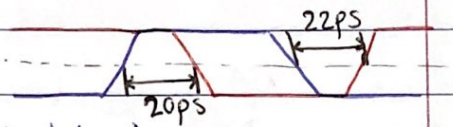
⇒ thus, we will need to change the device to minimize the delay.

◦ الديلي بين ال 50% للأولى و ال 50% التانية.

◦ ال slope بين ال 80% وال 20%



Question:

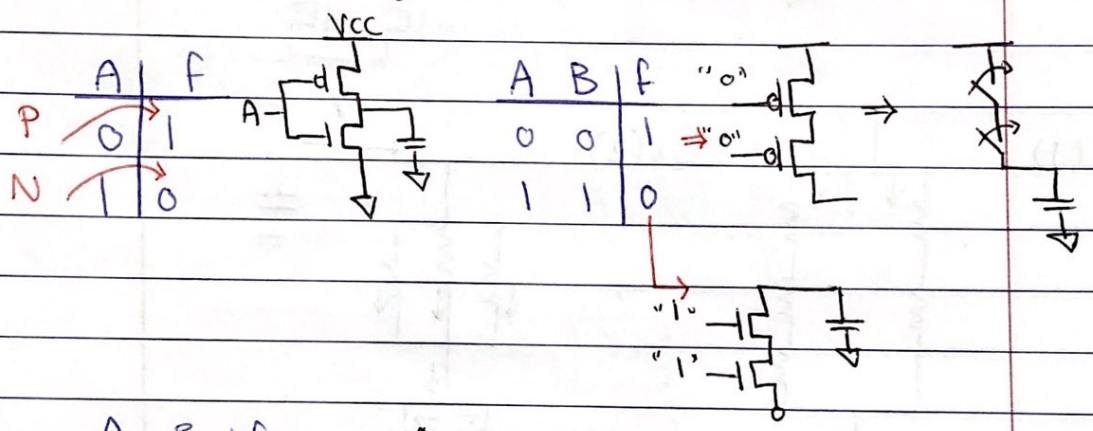


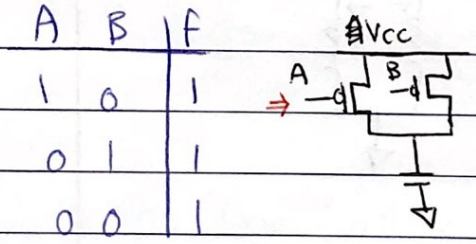
delay = max(p-delay , N-delay)

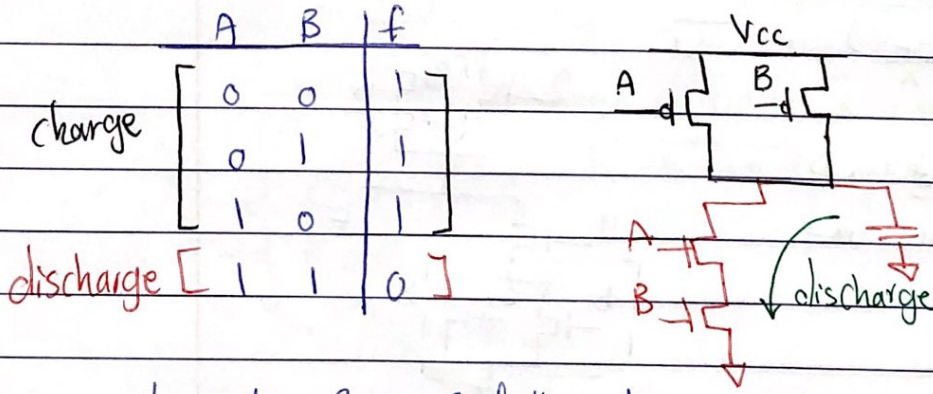
= 22 ps

changing the width of the p-device from w=1 to w=2. faster charging Higher internal capacitor on PMOS so it discharges on NMOS

skew making on edge faster than the other



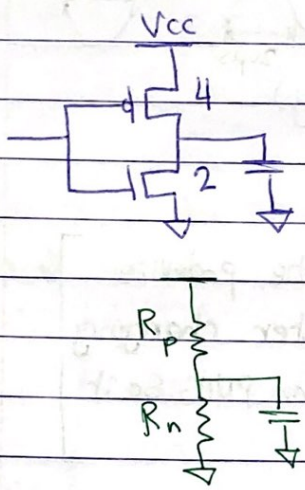


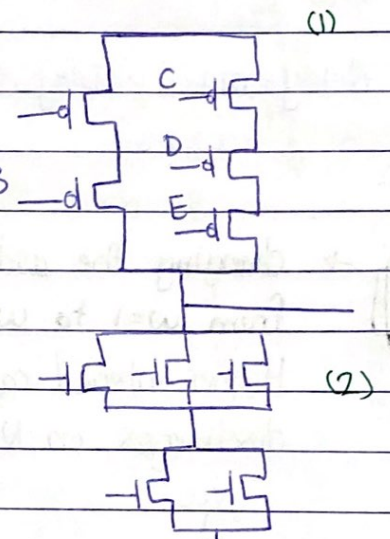


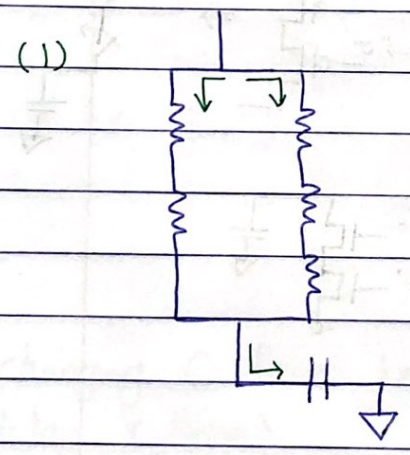
to make Rising & falling time equal

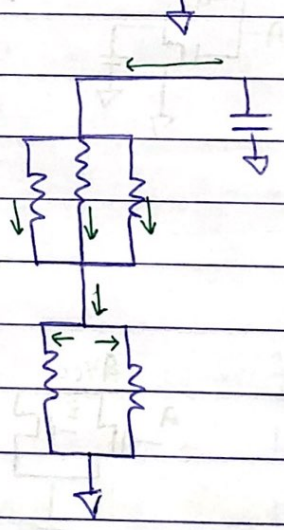
Series → Wxn → R_{in}

Parallel → no change → worst case (only one device is on)

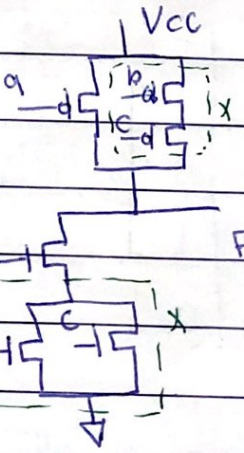






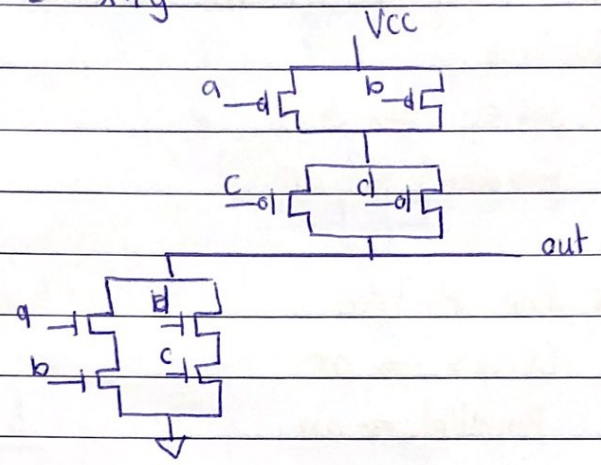


$$F = \overline{a.(\underbrace{b+c}_{x})} = \overline{a.x}$$

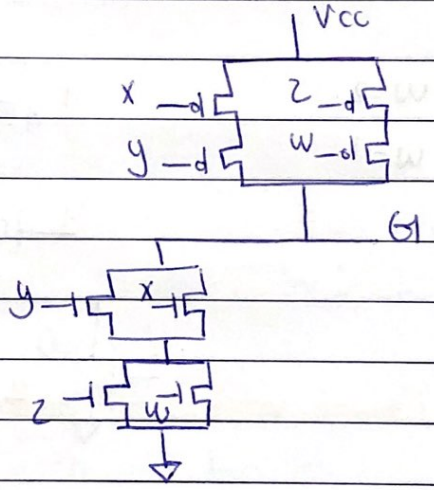


كما في طريقة طويلة
بس هاد أحسن

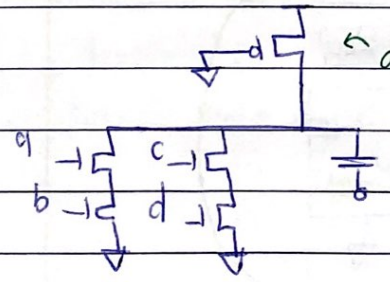
$$F = \overline{\underbrace{a.b}_{x} + \underbrace{c.d}_{y}} = \overline{x+y}$$



$$G1 = \overline{(x+y).(z+w)}$$



NMOS logic (will be discussed later)



← always on, but it is a weak device

$F = \overline{a.b + c.d}$ نفس الشيء

- We can extract the function using the

* N-tree

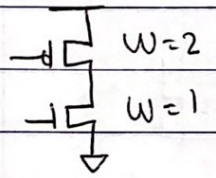
  Series ⇒ and

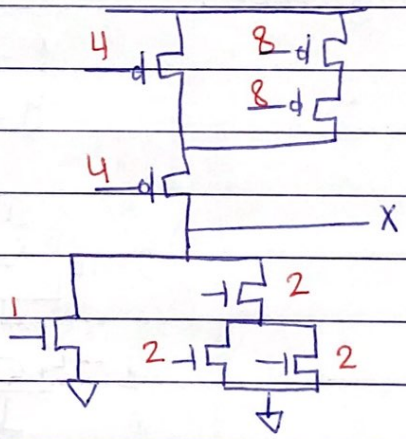
  Parallel ⇒ or

* For P-tree

  Series ⇒ or

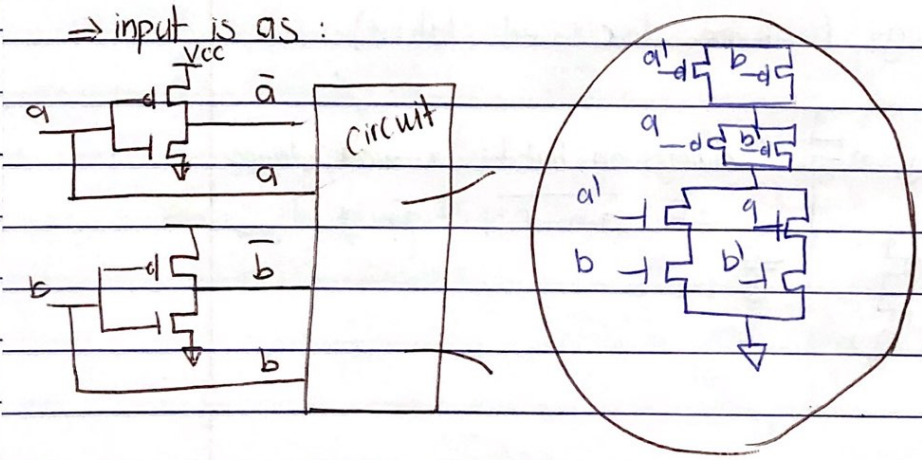
  Parallel ⇒ on



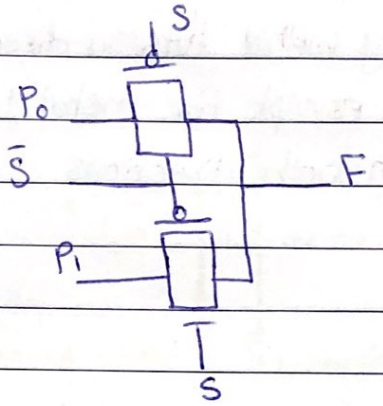


$F = a \oplus b = \bar{a}.b + a.\bar{b}$

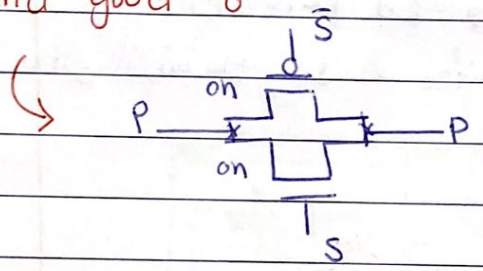
⇒ input is as :



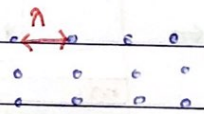
- 2-to-1 Mux



Constructed from two "pass-gates"
⇒ discussed previously
⇒ aims to get good "1" and good "0"

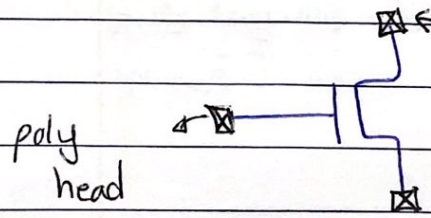


- Structured layout

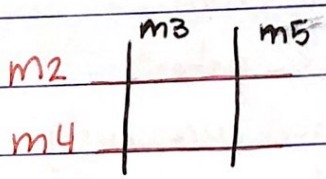


1) process
2) DRC [design roles check]
3) λ ⇒ 2λ = L [allows for scalable device]
   ↳ n+, metal, P+, di ⇒ each one has its design roles

- Contact : poly او مع ال diffu او مع ال metal بستبك ال — poly: gate
  ↳ device / poly / diffu (N, P)
- Vias: metal layers بستبك بين ال

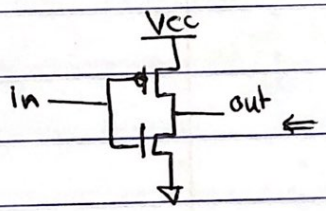


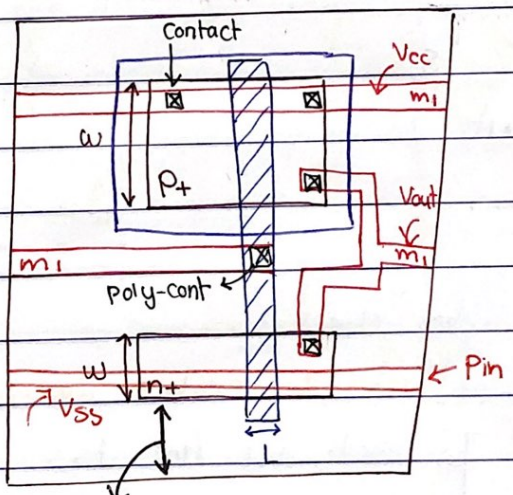
- every metal has a direction [horizontal / virtical]
  - # except for metal 1, where it can go in both directions



- برتب الـ p-device بجهة و الـ n-device بجهة من مبدأ انو الـ استبيك عن الـ Vcc و الـ Vss أسهل

- Inverter:





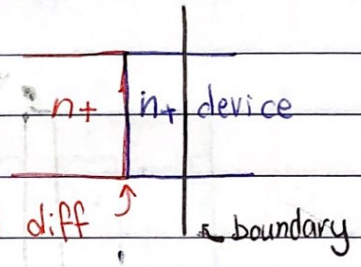
المسافة هاي بنجيبها من الـ [half-design rule]

المسافة بين الـ device و الـ boundries

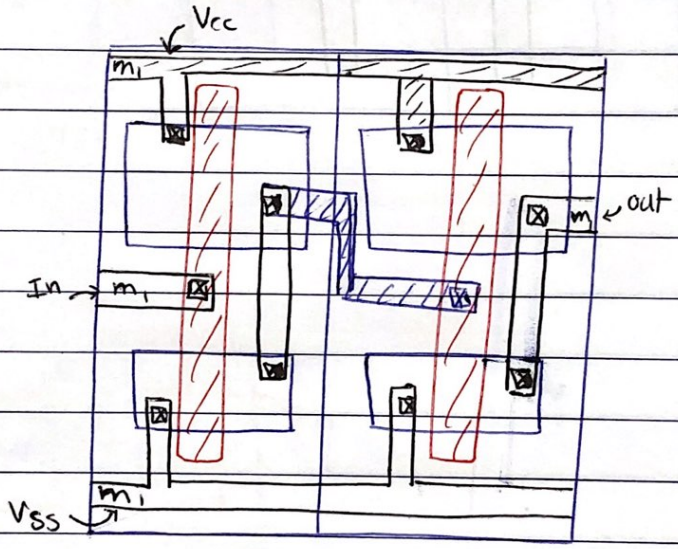
- لي اشي يوصل حوف الـ cell اسمه Pin
- اي اشي مش واصل لحوف بس بدي استخدمه [اشبك عليه] مدفون سميه Port .

- مرات الـ boundary بتكون لحوا و الـ device طالع لبرا

Shared diffusion:
two devices عشان أقدر أشبك
أقل Capacitance ←



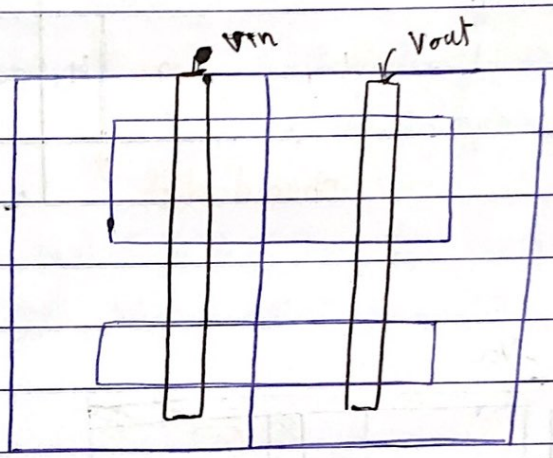
- Buffer:



- أحياناً بتزيد المسافة بين الـ NMOS و الـ PMOS عشان اذا اضطريت أكبر الـ Device مستقبلاً أقدر أزي أكبر الـ width مثلاً عشان اعمل الـ R في الـ trees مساويات.

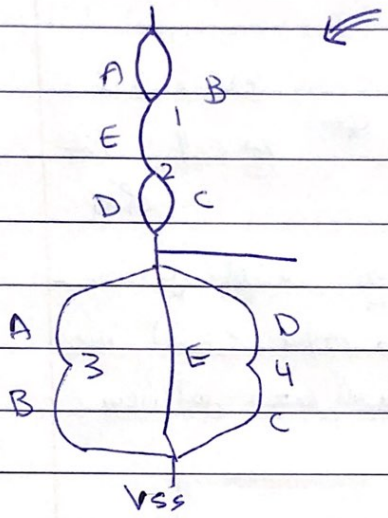
[ما بتكون مشغول بالـ Design rules]

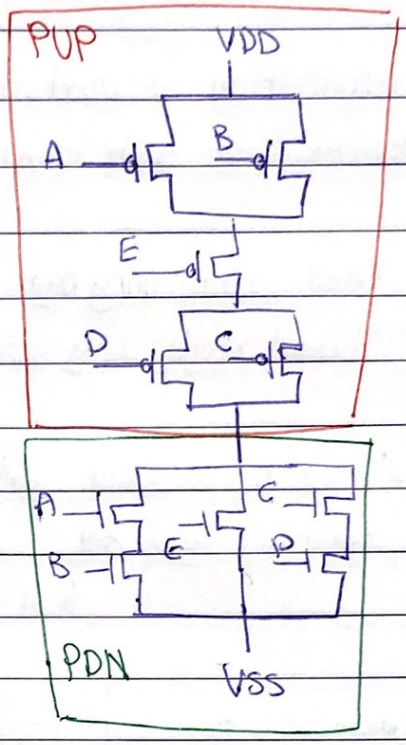
• الأفضل أرسم أو أصمم ال Buffer بطريقة تانية عشان أوفر مساحة ويصير الجهاز أصغر.

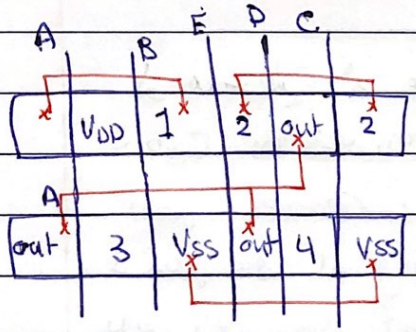


الرسمة مش كاملة

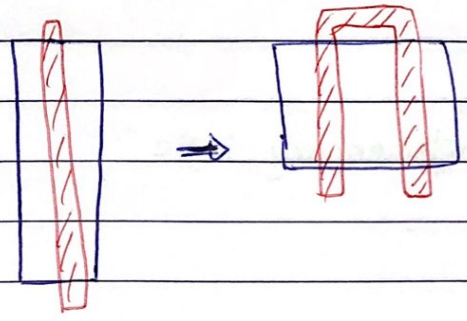
• Stick Diagram







• linking or fingers:

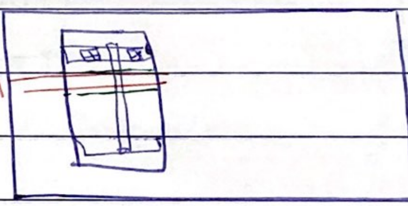


- Instantiation is used to distinguish the devices from each others.

- fixed width, vary high or fixed high, vary width ⇐ عشان نشبك كدا مع cell بعضها

- بنتعامل بالشكل مع الشي abstract إلا إذا اضطريت مثلاً أشيل metal فوق cell تانية ، لازم أعرف الـ layout عشان أقرر بقدر أشيل او لا :

zone: خلي عندي سبيس عشان أقدر أضيف layers بالخطوات لقدام.



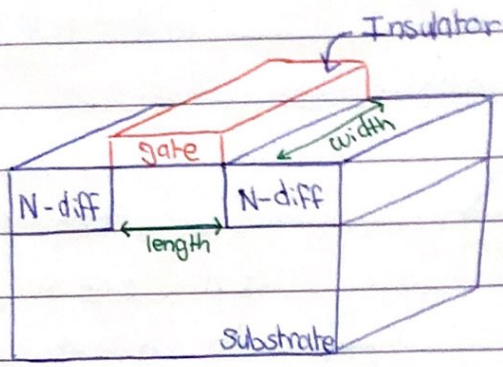
لو ما حطيت الـ zone مثلاً يبقى ممكن أعمل short circuit لو حطيت m1 فوق m1 .

- بعمل channel عشان أحط فيها metal layers عشان تسهل على الـ routing لأنه بقدرش أشيل فوق الـ cells بلاش يحصل عندي short .

* بنختار نوع الـ metal حسب المسافة وحسب قديش معي مساحة (track)

• "CMOS Complementary logic"

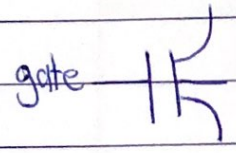
- Previous lecture



كانه سويتش

- oxide الـ فوق [gate or polysilicon] gate الـ
- اسمه NMOS كانه الترانزيستور N على P.
- اقل فولتج بصير عندي تيار ← V_T

- NMOS $V_d > V_s$ ⇒ to detect which terminal is the drain and which is the source



$V_{gs} < V_t$ ⇒ off

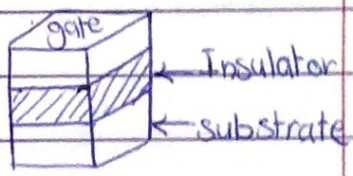
$V_{gs} > V_t$ ⇒ on

↳ linear region

$V_{DS} < (V_{gs} - V_t)$

$Q = C \cdot V$

↳ $\frac{\varepsilon_0 \cdot A}{t_{ox}}$ $(L \cdot W)$



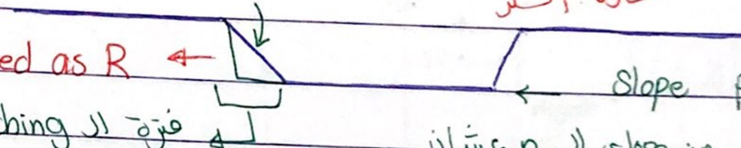
$\frac{dQ}{dt} = C \cdot \frac{dV}{dE} \Rightarrow i_d = \frac{\varepsilon \cdot W L}{t_{ox}} \cdot \frac{\frac{1}{2}(V_{gs}-V_t)(V_{gs}-V_t)}{L^2}$ ← $\frac{1}{2}(V_{gs}-V_t)$

$\frac{\text{السرعة}}{\text{الحركة}} \rightarrow \frac{L}{\mu_e E} = \frac{L}{\mu_e \frac{(V_{gs}-V_t)}{1}} = \frac{L^2}{\mu_e (V_{gs}-V_t)}$

$$i_d = \frac{1}{2} \frac{\epsilon_o \mu_e W (V_{gs} - V_t)^2}{t_{ox} \cdot L}$$

$$i_{d_n} = \frac{1}{2} C_{ox} \cdot \frac{W}{L} \cdot (V_{gs} - V_t)^2$$

اذا لما id أسرع بتكون حارة أكثر ← بنضعف W غالباً عشان تمشي حارة أكثر.



NMOS treated as R ←

← فترة الـ Switching

ال P Slope ← أقل من slope ال n عشان هيك بلعب بال width ليصيروا زي بعض.

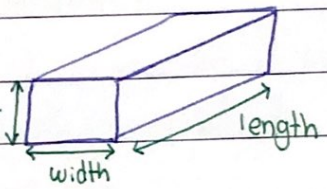
Notes: - How to evaluate performance of a digital circuit?

- Cost
- Reliability
- Speed / Performance (delay, frequency)
- Power

"hight is fixed"

$R_{line} = \frac{\rho \cdot l}{A}$

Resistance = $\frac{\text{length} \times \text{resistivity}}{\text{width} \times \text{hight}}$



Ω/square

$R_S = \frac{\rho}{\text{thickness}}$ $\quad R_{line} = R_S \cdot \frac{L}{W}$

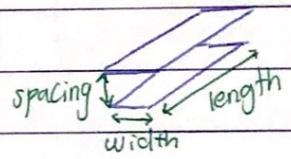
- Contacts are used to shrink standard cells.
- ~~Parallel plate capacitance:~~

$C_{line} = \frac{\varepsilon_{ox} \cdot (W \cdot L)}{t_{ox}}$ ← Area

- RC time constant of interconnect line

$\tau = R_{line} \times C_{line}$

- Parallel plate capacitance $\propto \frac{\text{width} \times \text{length}}{\text{spacing}}$



- Via Resistance Model:

$R = res * (1 + (te * (temp - 25)))$

" are given "

- process node: length of Gate

- Cost per IC = variable cost per IC + fixed cost / volume

  ↓

  cost of die + cost of die test + cost of packaging / final test yield

- cost of die = cost of wafer / (dies per wafer * die yield)

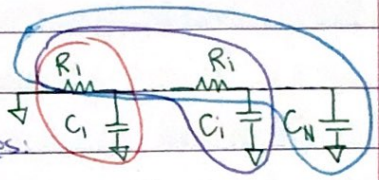
- Yield = # of good chips per wafer / total # of chips per wafer × 100%

- Dies per wafer = $\frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$

- die Yield = $\left[1 + \frac{\text{defect per unit area} \times \text{die area}}{\alpha}\right]^{-\alpha}$ $\alpha \approx 3$

die cost $\propto$ $\frac{1}{(\text{die/wafer} \propto \text{die area}^{-1})(\text{yeild} \propto \text{die area}^{-3})}$ $\propto \text{die area}^4$

- RC delay estimates:



→ Penfield-Rubenstein model estimates:

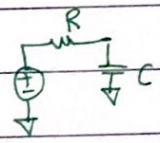
$$\text{Delay} = \sum_i \left(\sum_{j=1}^{j=i} R_j \right) C_i$$

- Cross capacitance: any capacitance between nets, which are non DC nets.

attacking: signal that has cross capacitance
victim: signal we are analyzing.

$i(t) = C \boxed{\frac{dV(t)}{dt}}$ → bigger or smaller than the DC case it depends on the switching direction of the victim and the attacking

- Miller effect: the effective capacitance between the line and the ground changes



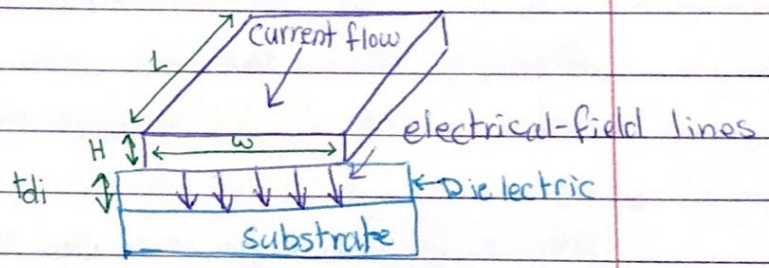
- Lumped line model: assumes all the capacitance line and load, is located at the end of the line
  - as the RC delay increases, the lumped RC model is less accurate.

- Fring capacitance: as the process dimensions get smaller the ratio (T/W) and (T/H) increases.
  → T has to increase for better resistance
  → fring capacitance become more significant

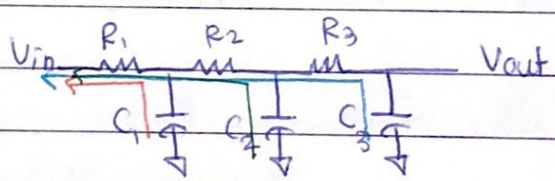
- Distributed RC line model; "more accurate"
  → is built of many segments, and each segment is modeled as lumped RC model.
  "a simulation is needed to calculate the RC delay"

- Capacitance: Parallel Plate Model

$$C_{int} = \frac{\varepsilon_{di} \cdot W \cdot L}{t_{di}}$$



- Elmore delay



$$\tau_{Elmore} = R_1C_1 + (R_1+R_2)C_2 + (R_1+R_3+R_2)C_3$$

- Basic steps for CMOS IC fabrication:

1) - Wafer Production
   - Epitaxial Growth

2) Masking: to protect other parts when working on specific place or area of the wafer.

3) Etching: it removes material selectively from the surface of wafer to create patterns.
- patterns are defined by etching mask

4) - Doping: to alter the electrical character of Silicon with atom with one less electron and atom with one more electron

- Atomic diffusion:
  p and n regions are created by adding dopants into the wafer. the wafers are placed in an oven made of quartz and is surrounded with heating elements.

- Ion implame implantation:
  another method for doping.
  → dopant gas will be ionized, then it provides a beam of high energy dopant ions to the specified regions of wafer