Faculty of Information Technology

Electrical and Computer Engineering Department

DIGITAL INTEGRATED CIRCUITS (ENCS333)

Introduction to Microwind and DSCH 3.5

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➢ Objective

- ❖ Download Microwind and DSCH tools.
- ❖ Identify some icons and components.
- ❖ Do some tasks using Microwind and DSCH.

➢ Introduction

- ❖ Microwind:

  is a tool for designing and simulating circuits at layout level. allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate.

- ❖ DSCH:

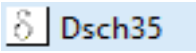
  is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures.

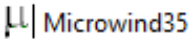
➢ Downloading microwind3.5 & DSCH3.5

Download the **"Microwind 3.5 with DSCH 3.5"** folder from following link:

https://drive.google.com/open?id=1nB6mmeM36nudDxUaITYaG82PqU61tTqg

❖To open the program, follow these steps:

- Extract the folder that you download it.
- Open it. You will see two folders, one for the DSCH and another for the Microwind.
- To open the DSCH program, open "**dsch35 full"** folder. Then, open **"system"** folder. After that, you will see the program with name **"DSCH35"** and its icon 

. Click on it to open the program and the screen will be as the Figure1 below.
- To open the Microwind program, open **"microwind35 full"** folder. Then, open **"system"** folder. After that you will see the program with name **"Microwind35"** folder. After that, you will see the program with name **"Microwind35"** and its icon 

. Click on it to open the program and the screen will be as the Figure2 below.

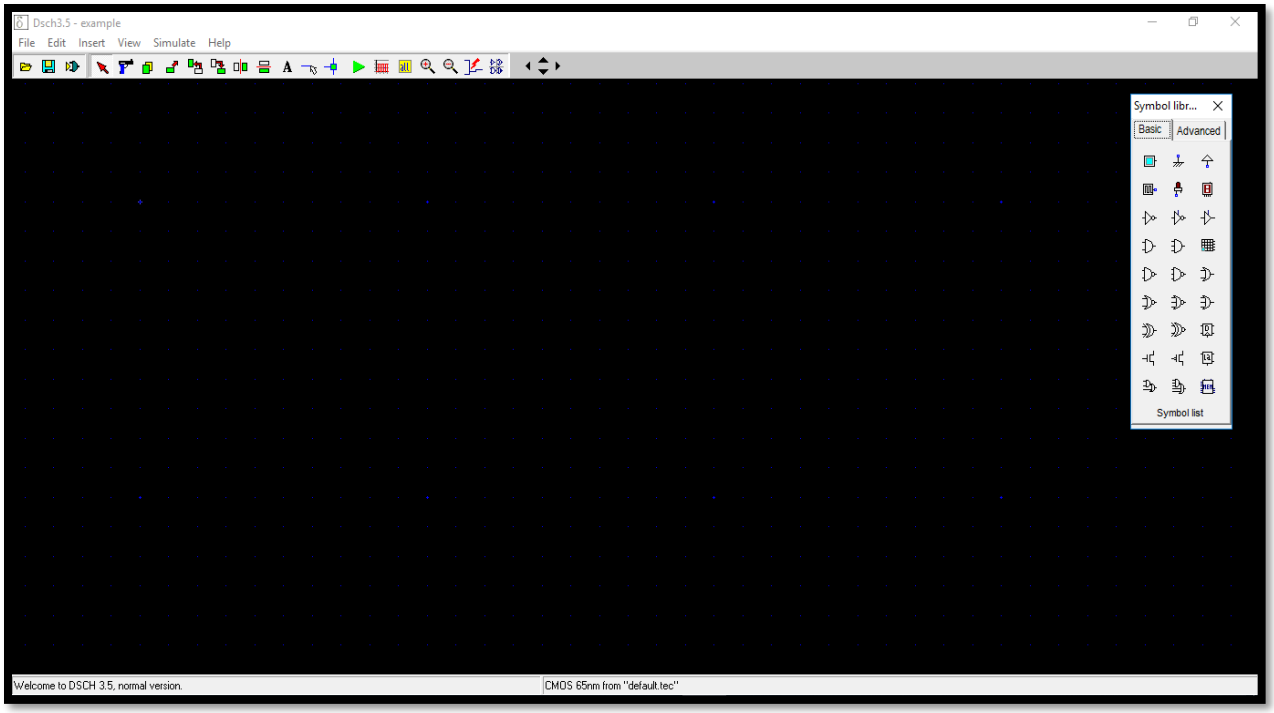


Figure 1: DSCH35_Tool

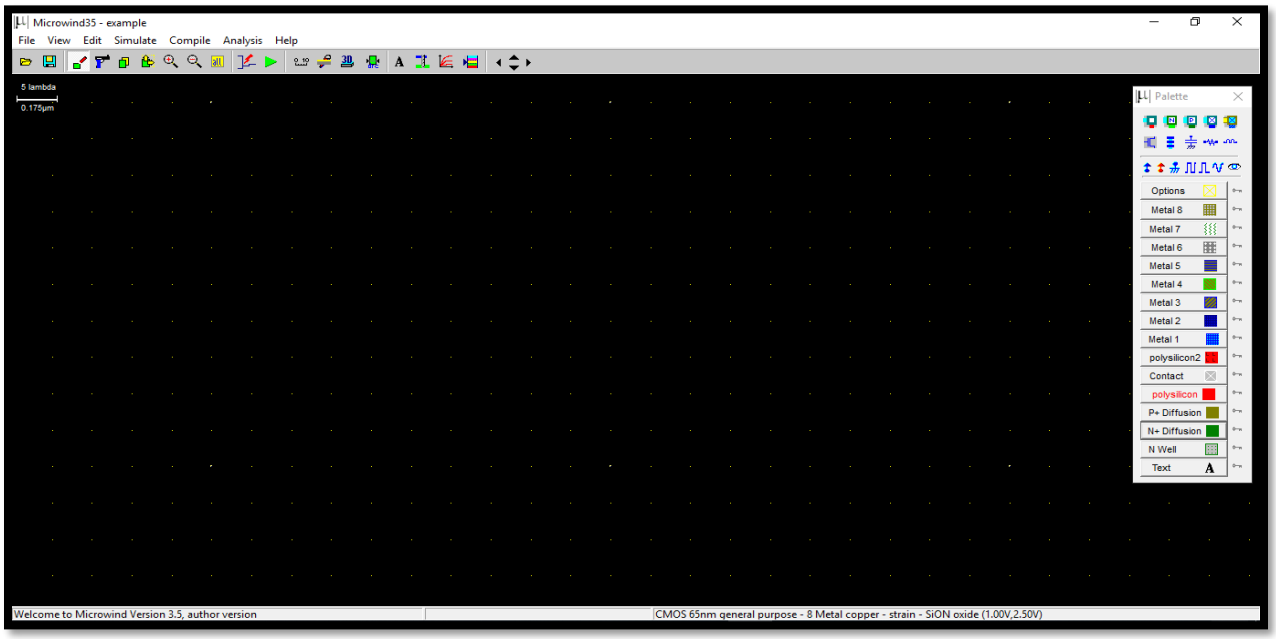


Figure 2: microwind35_tool

➢ Identify some icons in the Microwind35 & DSCH35

❖ DSCH35 menus:

- Symbol Palette:

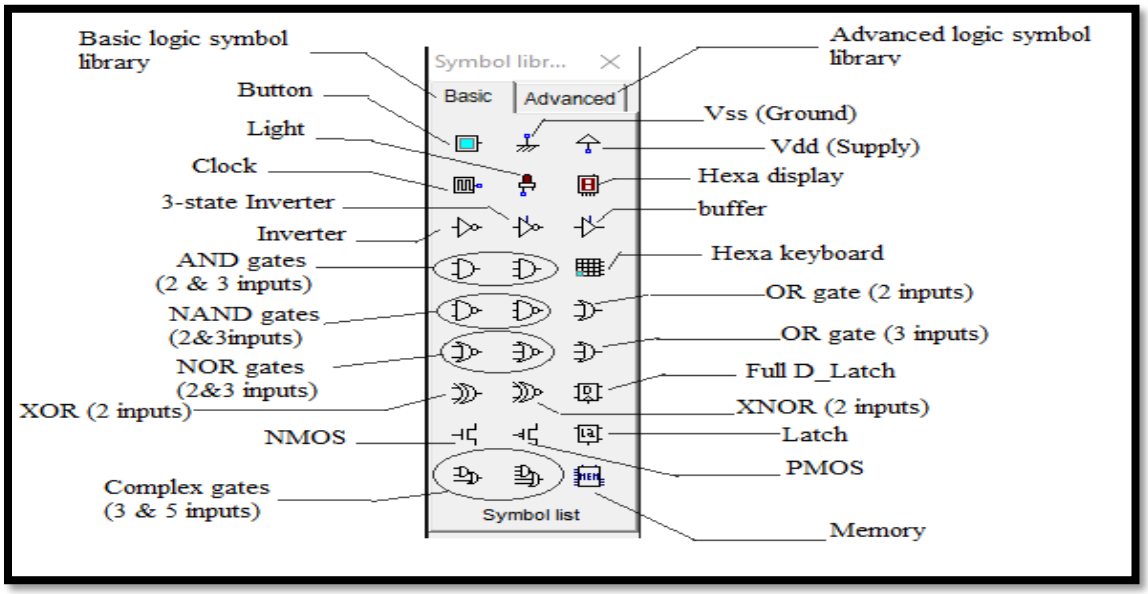


Figure 3: Symbol list

- File Menu:

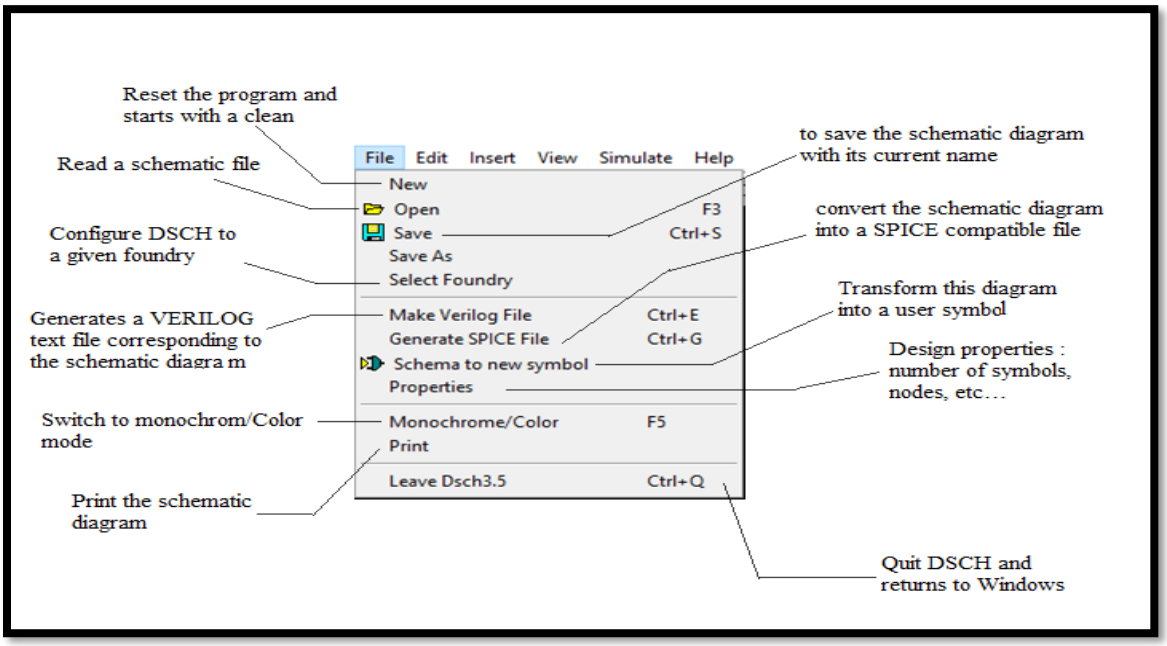


Figure 4: File menu

- Edit Menu

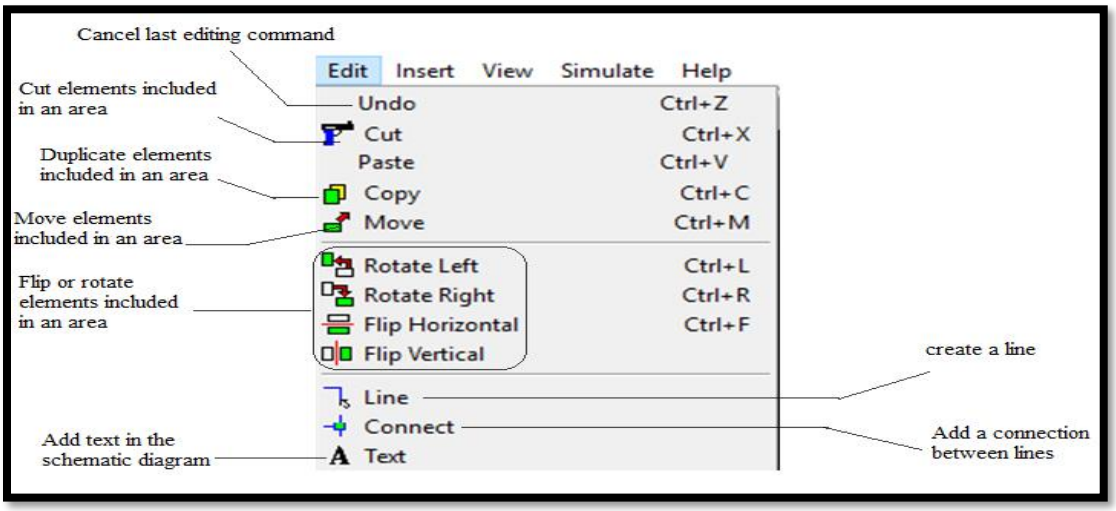


Figure 5: Edit menu

- Insert Menu

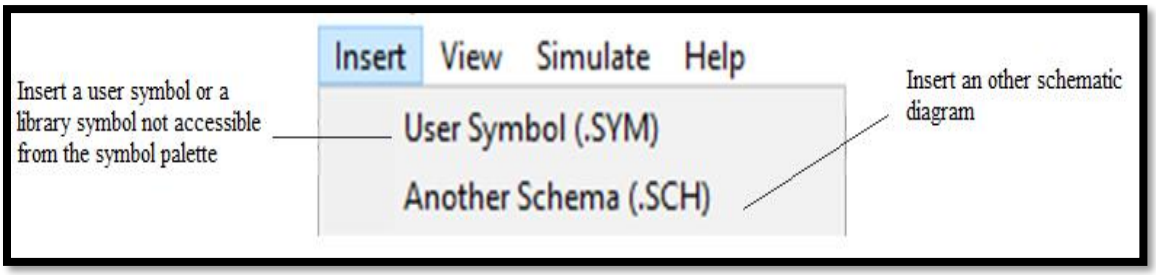


Figure 6: Insert Menu

- View Menu

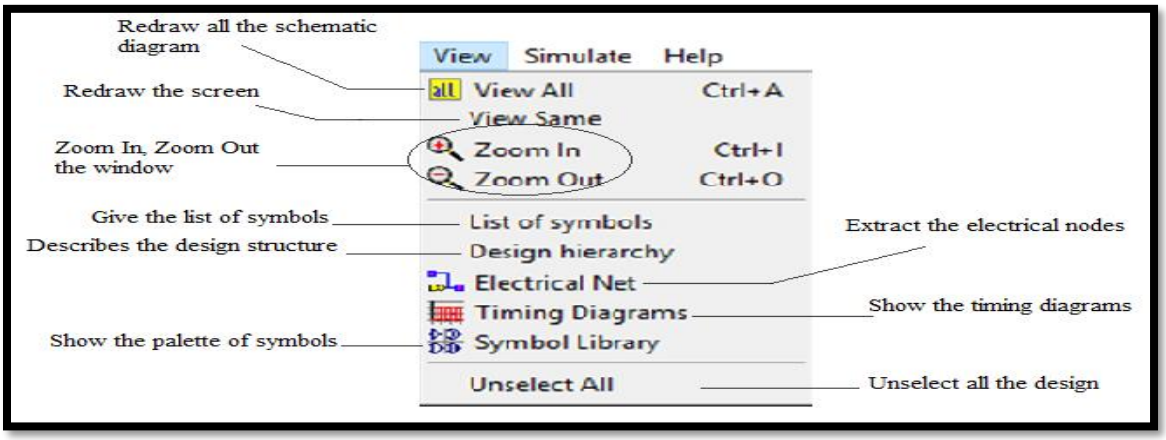


Figure 7: View Menu

- Simulate Menu

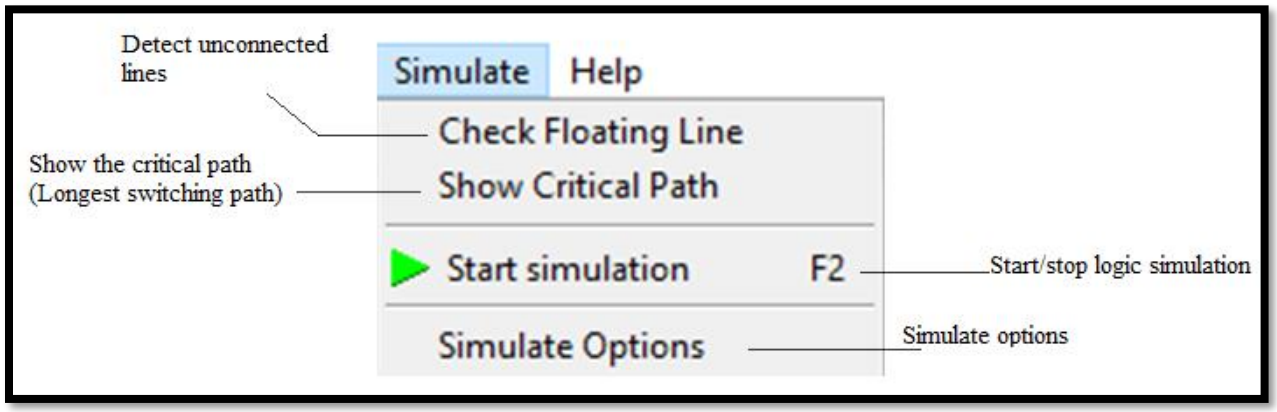


Figure 8: Simulate menu

- List of icons

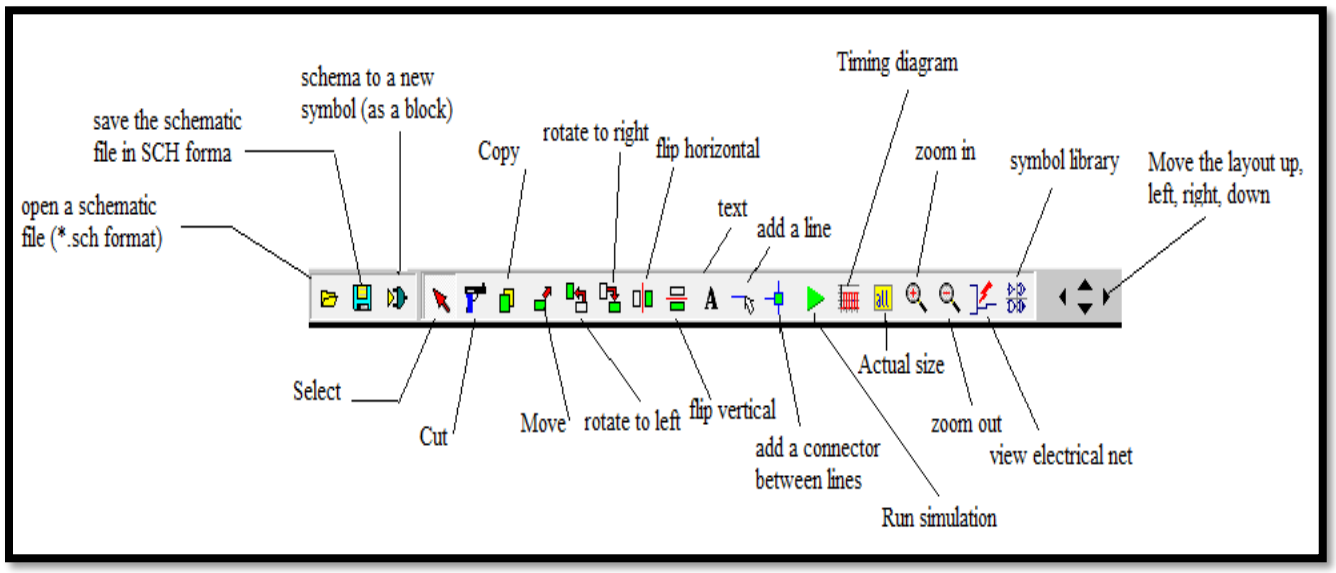


Figure 9: list of icons

❖ Microwind 3.5 menus:

- Palette

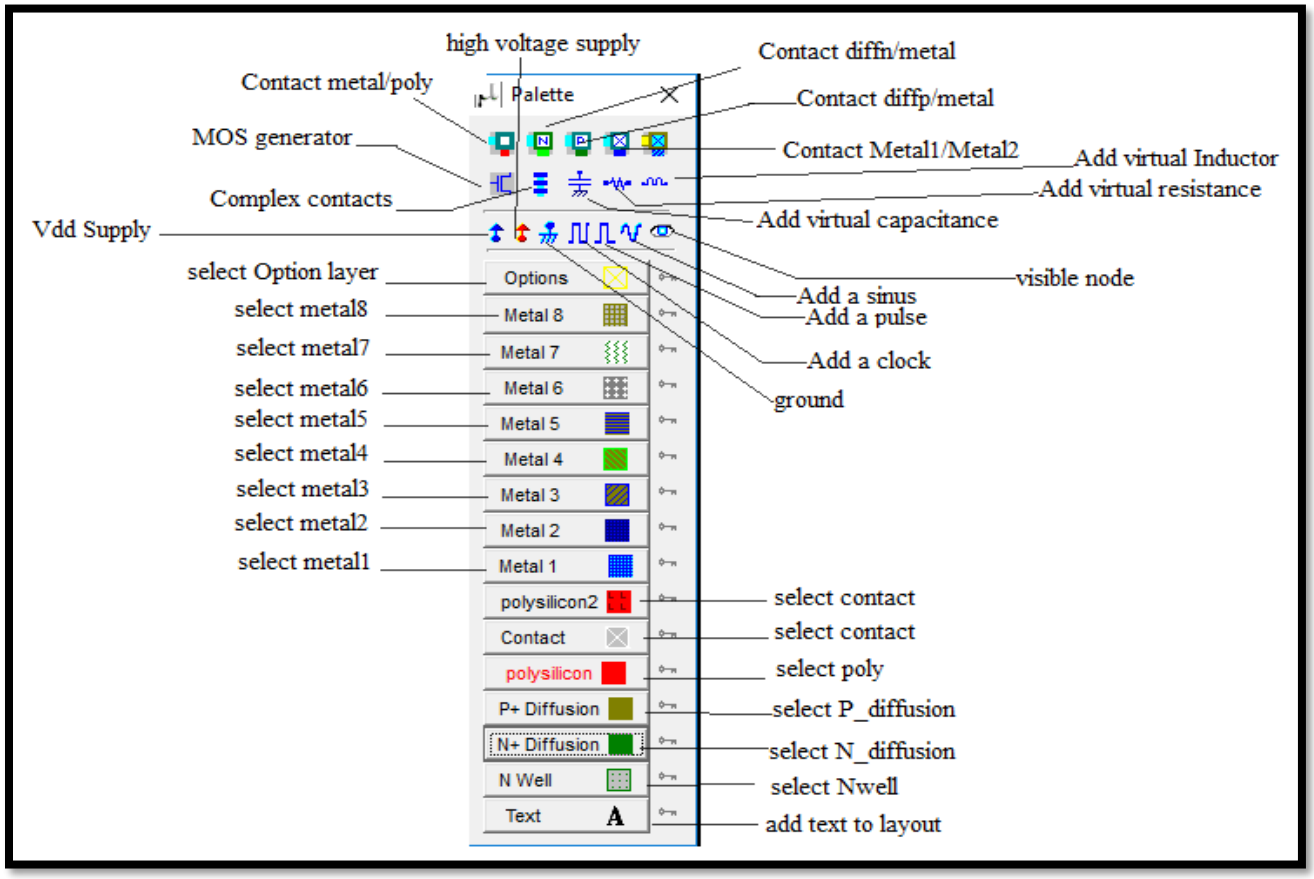


Figure 10: Palette

- File Menu

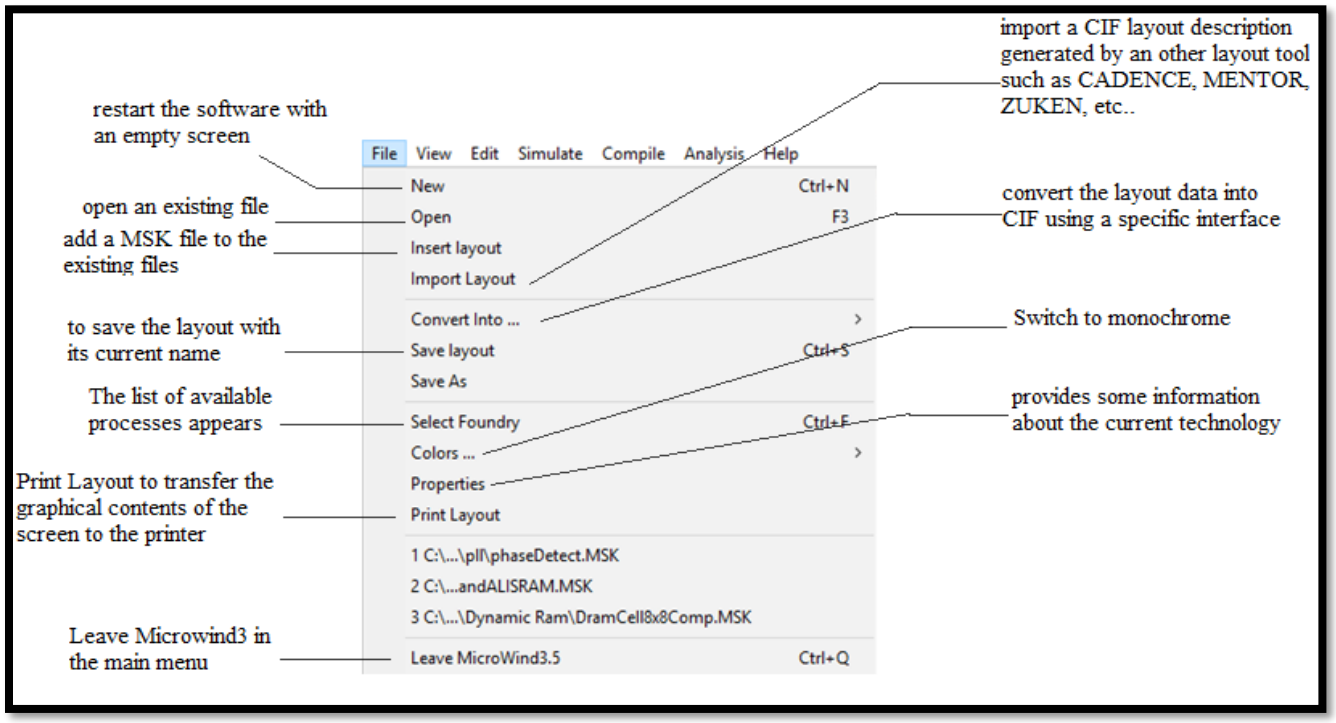


Figure 11: File Menu

- View Menu

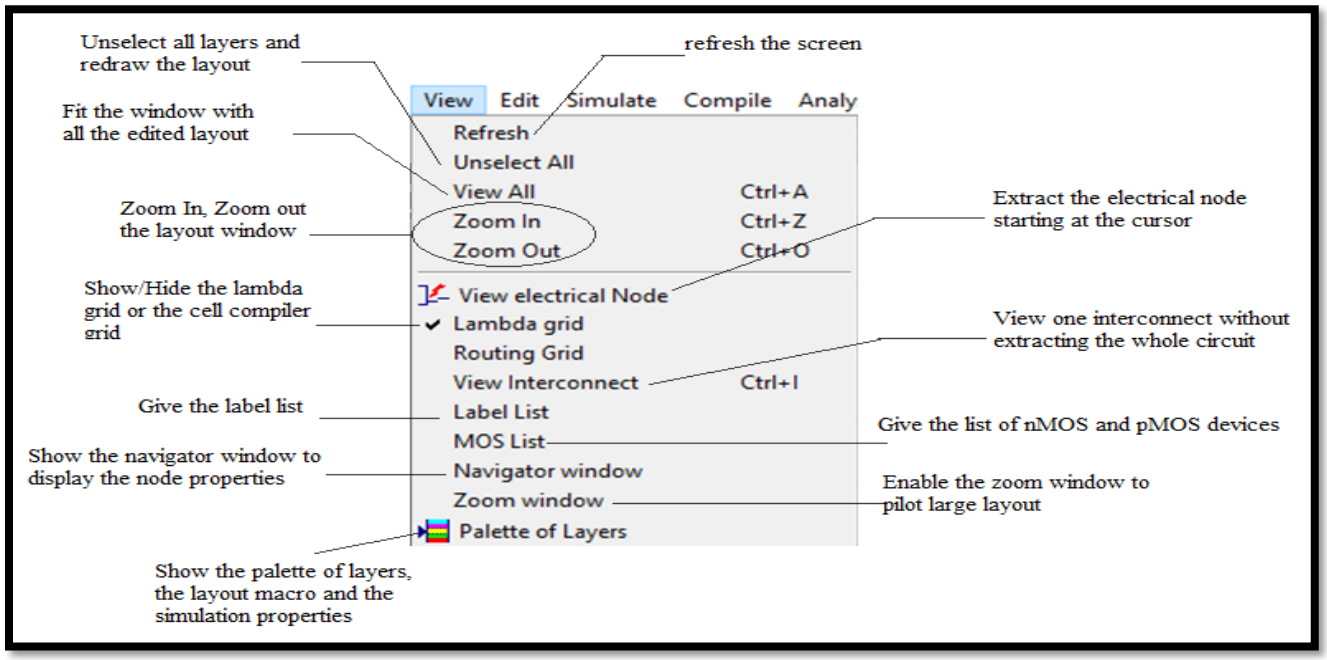


Figure 12: View menu

- Edit Menu

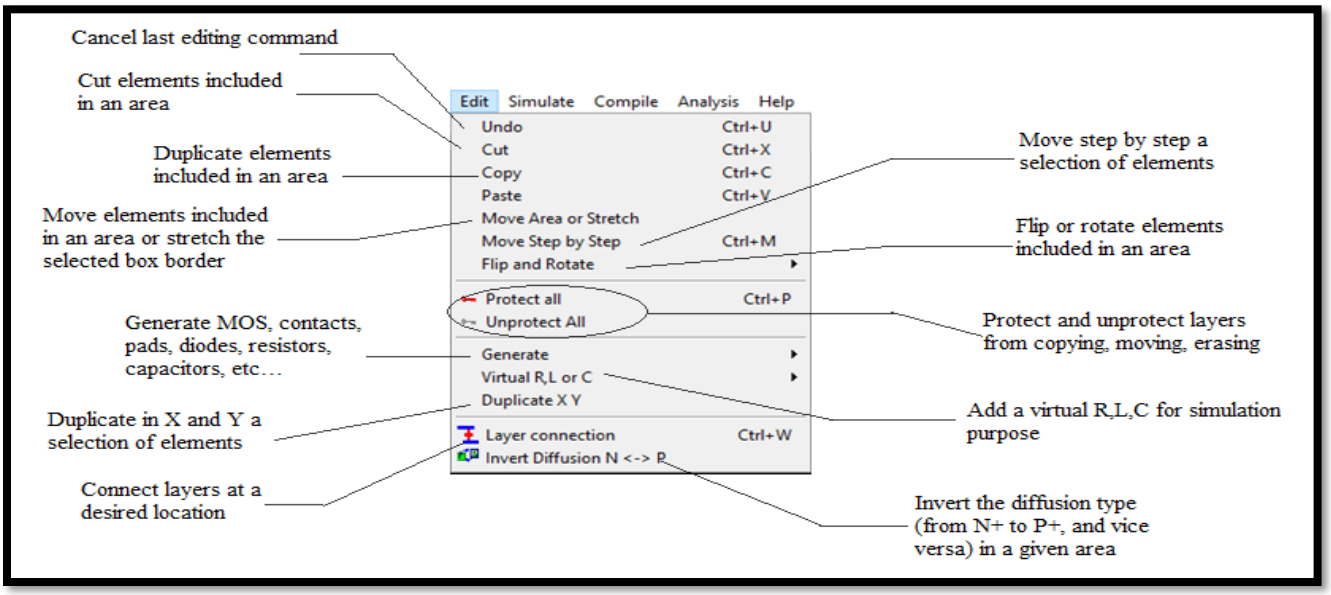


Figure 13: edit menu

- Simulate Menu

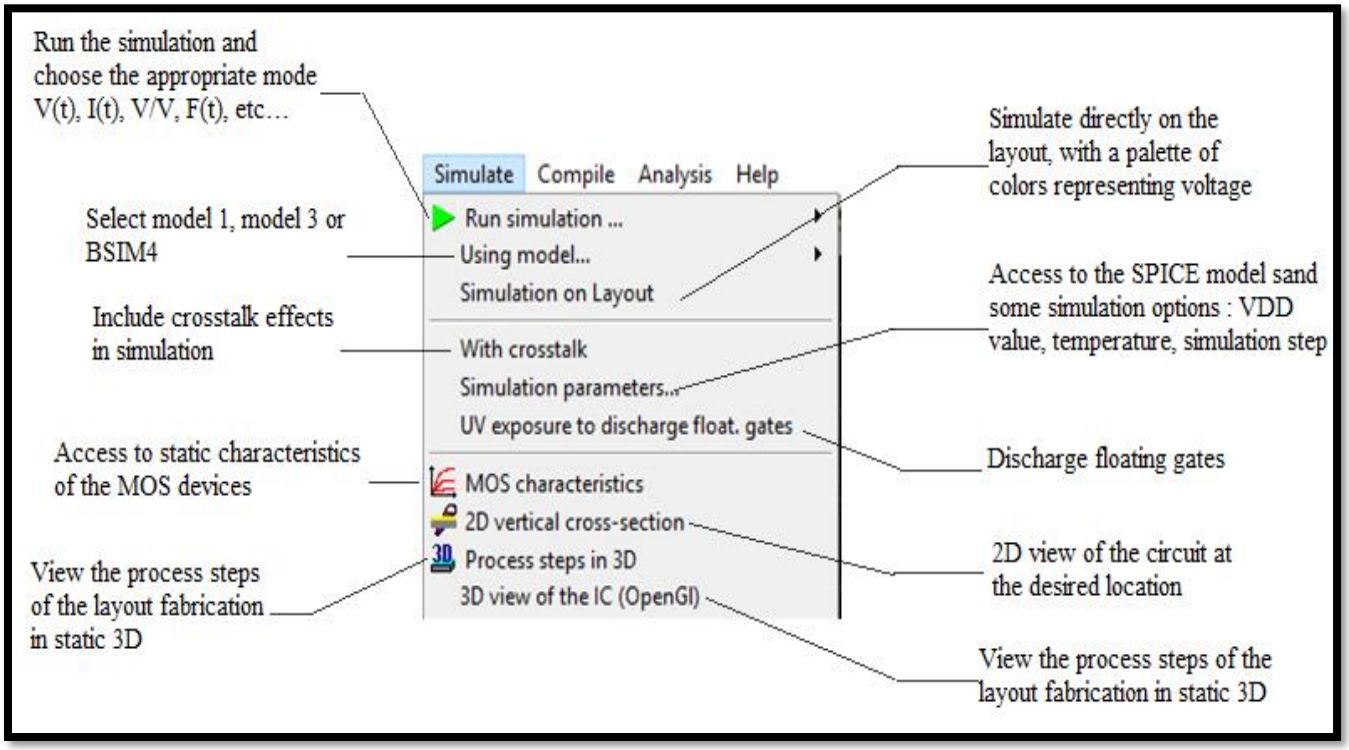


Figure 14: simulate menu

- Compile Menu

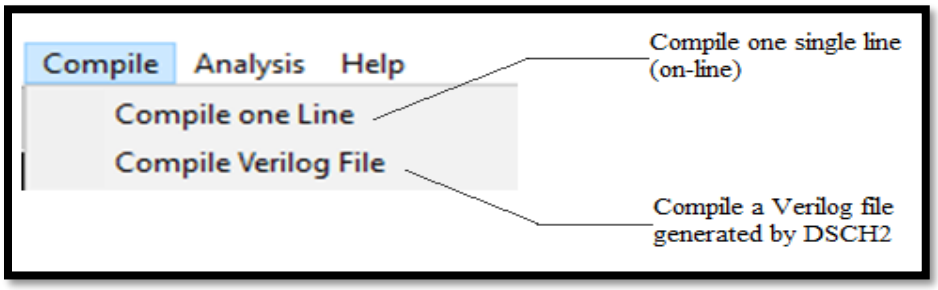


Figure 15: compile menu

- Analysis Menu

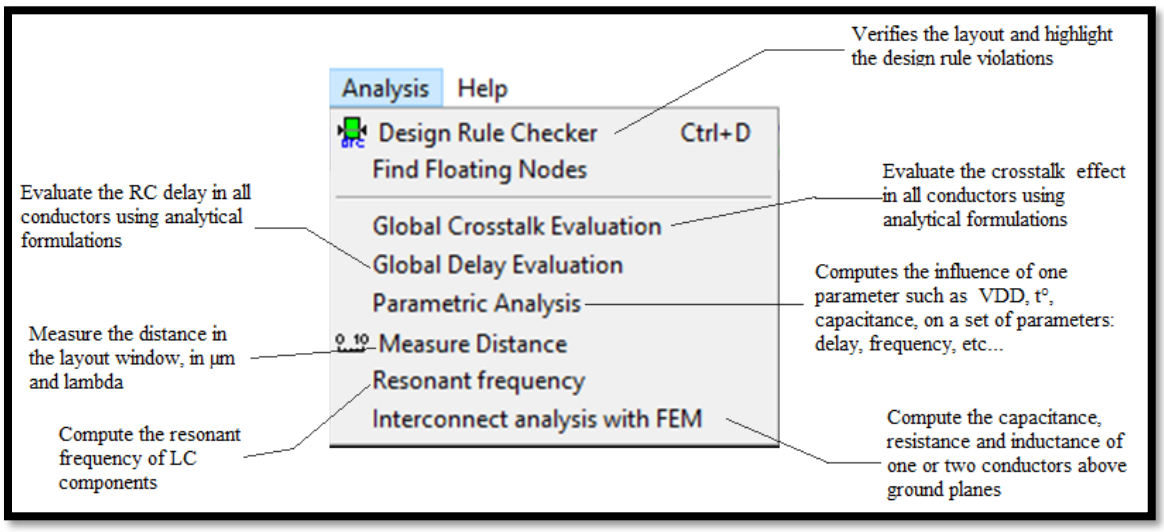


Figure 16: Analysis Menu

- List of icons

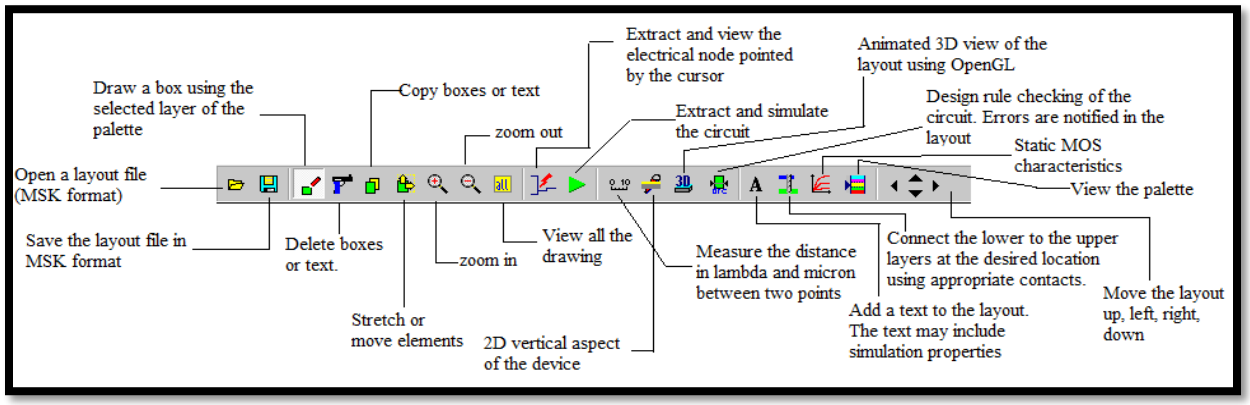


Figure 17:list of icons

➢ Microwind/DSCH NOR example:

- Open the DSCH tool.
- Click on the NMOS transistor from the symbol library and place it in the editor window. As you see in the figure 16 below.

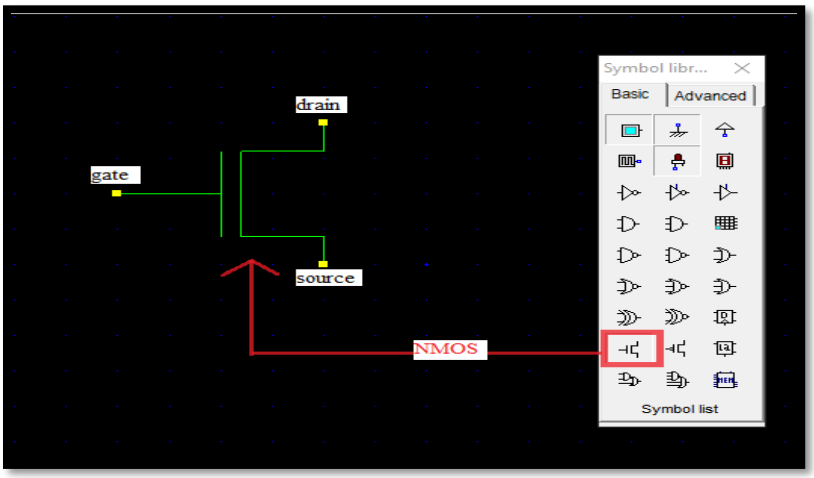


Figure 18: NMOS transistor symbol

- The same way for PMOS transistor. See figure17.

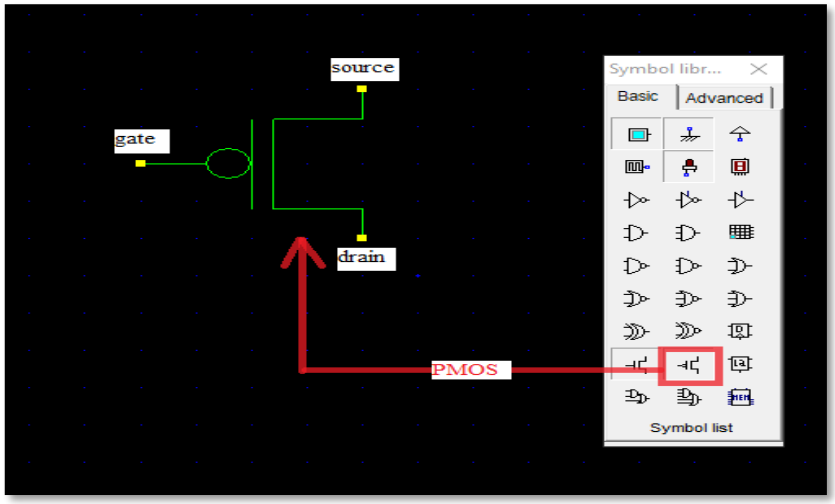


Figure 19: PMOS transistor symbol

- Instantiate 2 NMOS and 2 PMOS transistors. Then, connect the drains and sources of transistors (Press on the node and then drag)as figure 18.

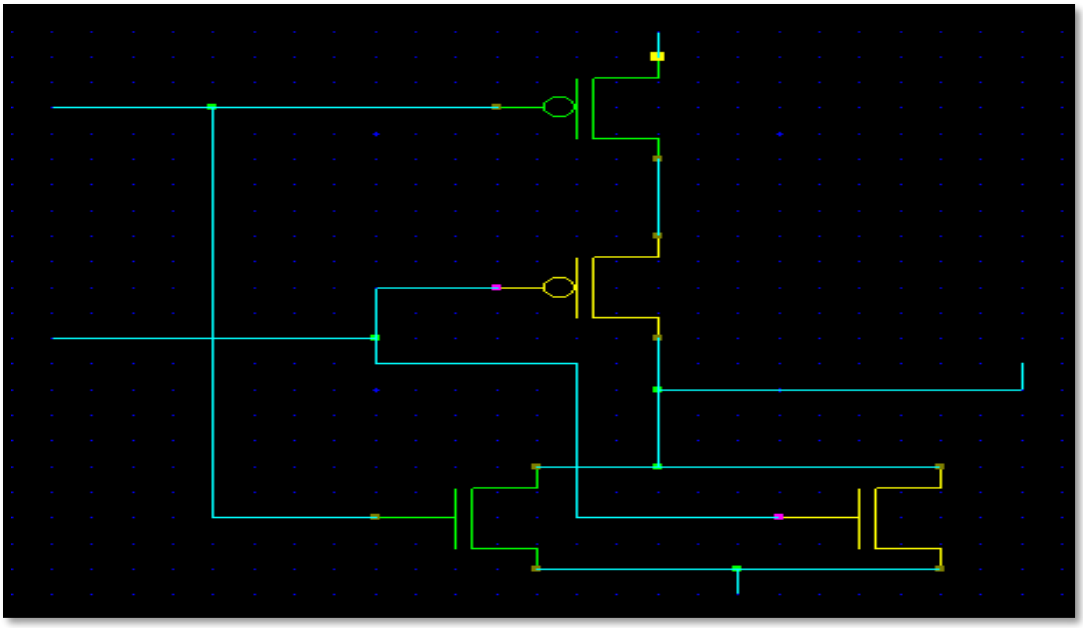


Figure 20: PMOS & NMOS connection

- Connect Vdd and GND to the schematic and Connect input button and output LED. See figure 19. (you can use clock input)

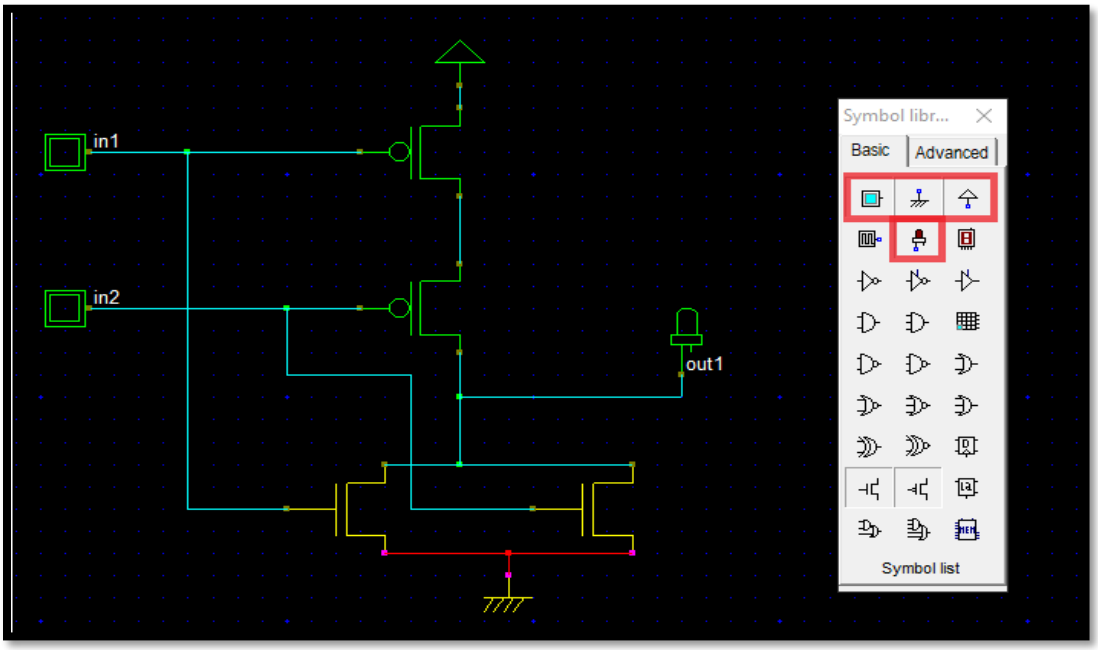


Figure 21: NOR schematic

- You now have NOR schematic ready.
- Use your logic simulator to verify the functionality of your schematic.
- The next step is to simulate the circuit and check for functionality.
- Click on Simulate -> Start simulation.
- This brings up a Simulation Control Window. Click on the input buttons to set them to 1 or 0. Red color in a switch indicates a '1'. See figures below:

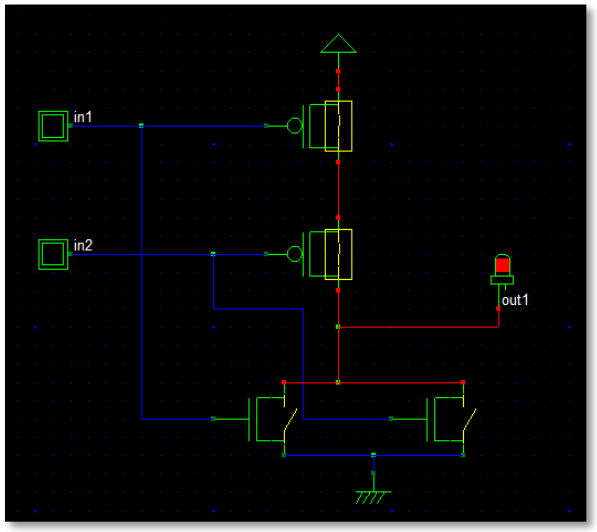


Figure 22: inputs 0,0

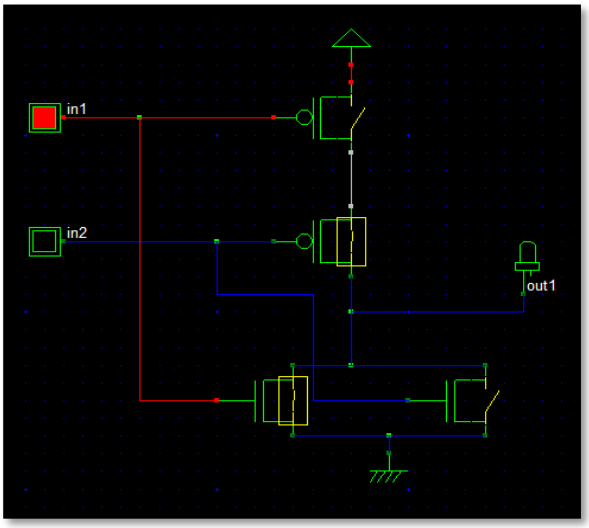


Figure 23: inputs 1,0

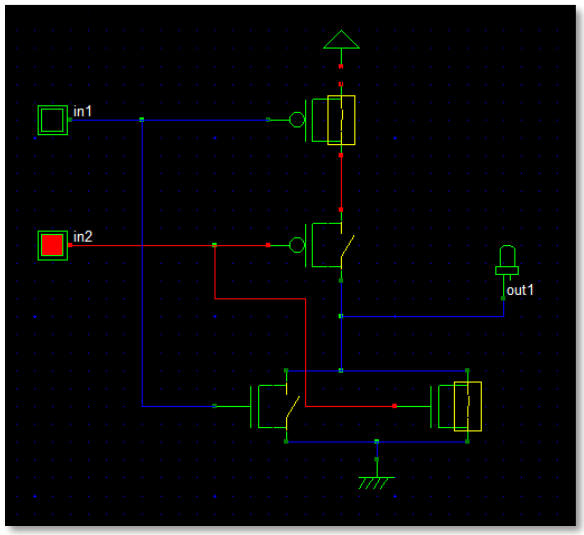


Figure 24: inputs 0,1

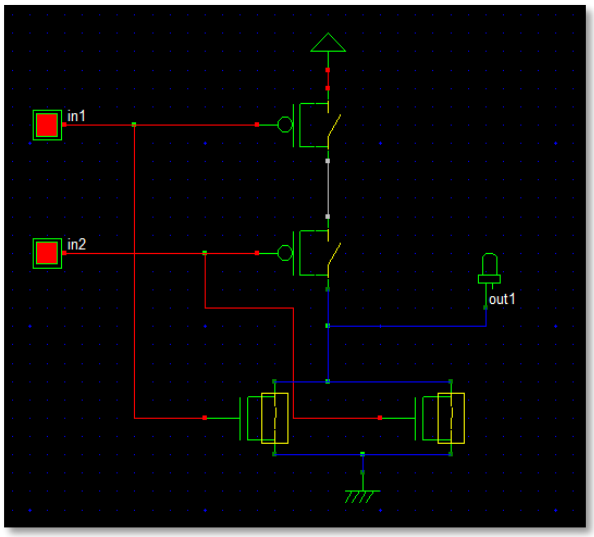


Figure 25: inputs 1,1

- The simulation output can be observed as a waveform after the application of the inputs as above. Click on the timing diagram icon in the icon menu to see the timing diagram of the input and output waveforms.

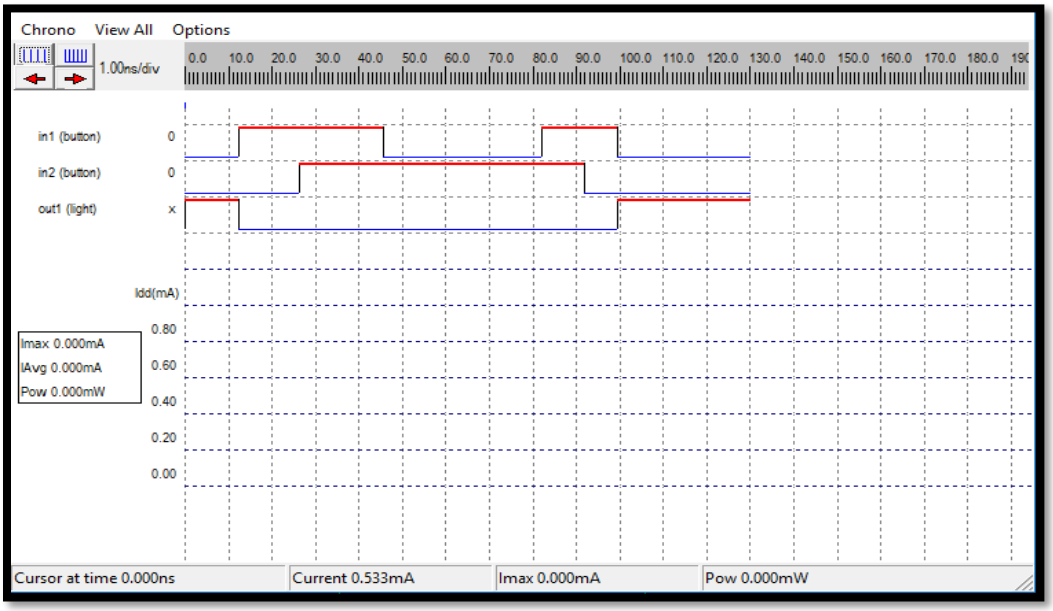


Figure 26: Timing diagram.

- Simulate your system with your hand calculated transistor sizes.
- Click File -> Make Verilog File. The Verilog, Hierarchy and Netlist window appears. This window shows the Verilog representation of NOR gate. Click OK to save the Verilog as a .txt file.
- Open the layout editor window in Microwind. Click File -> Select Foundry and select Y.rul. This sets your layout designs in Y technology. See figure 25:

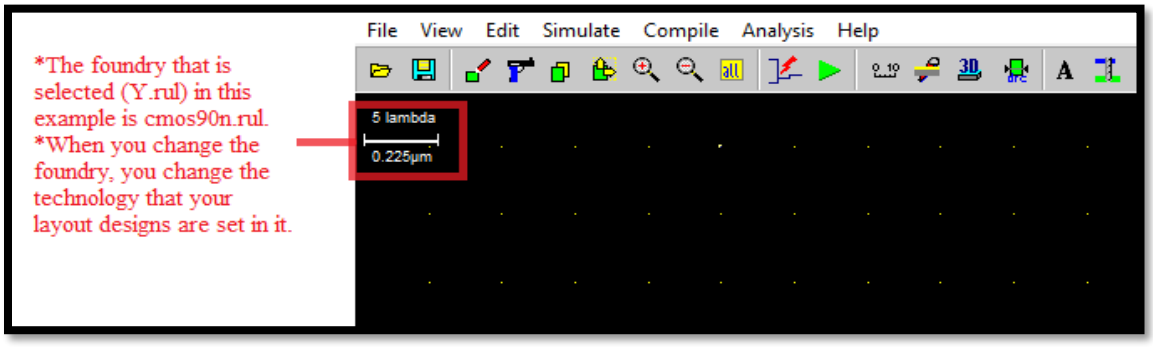


Figure 27: technology scaling

- Click on Compile -> Compile Verilog File. An Open Window appears. Select the .txt Verilog file saved before and open it.
- After selecting the .txt file, a new window appears called Verilog file. See Figure 26:

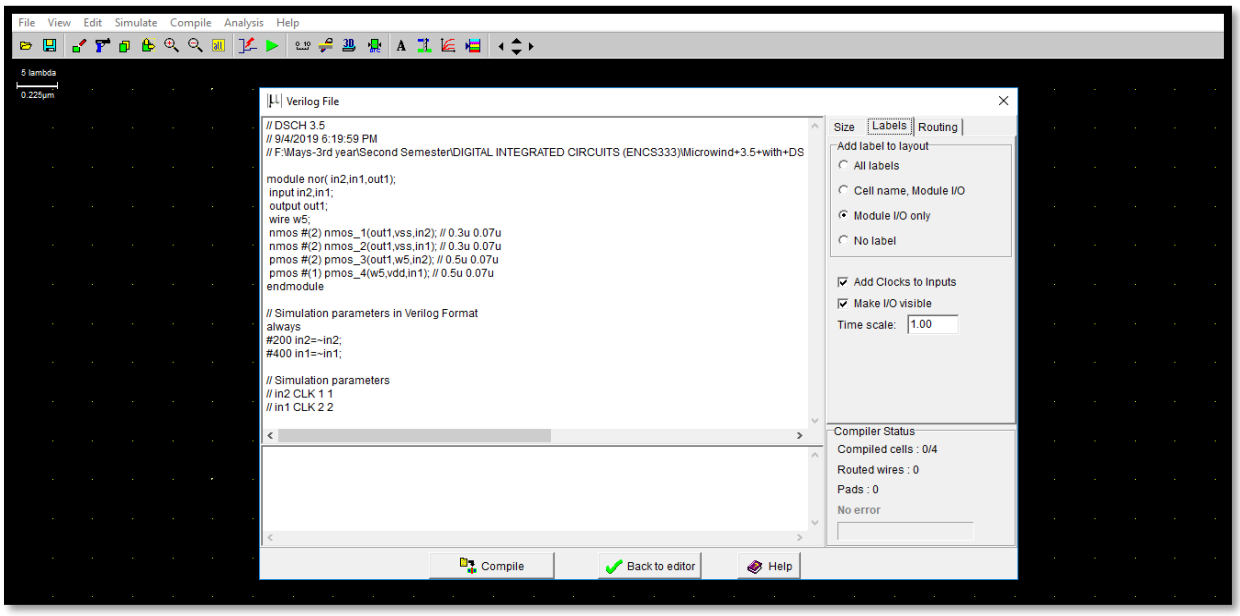


Figure 28: Verilog file window

- Click on Size on the right top menus. This shows up the NMOS and PMOS sizes. Set the sizes according to choice. See figure 27:

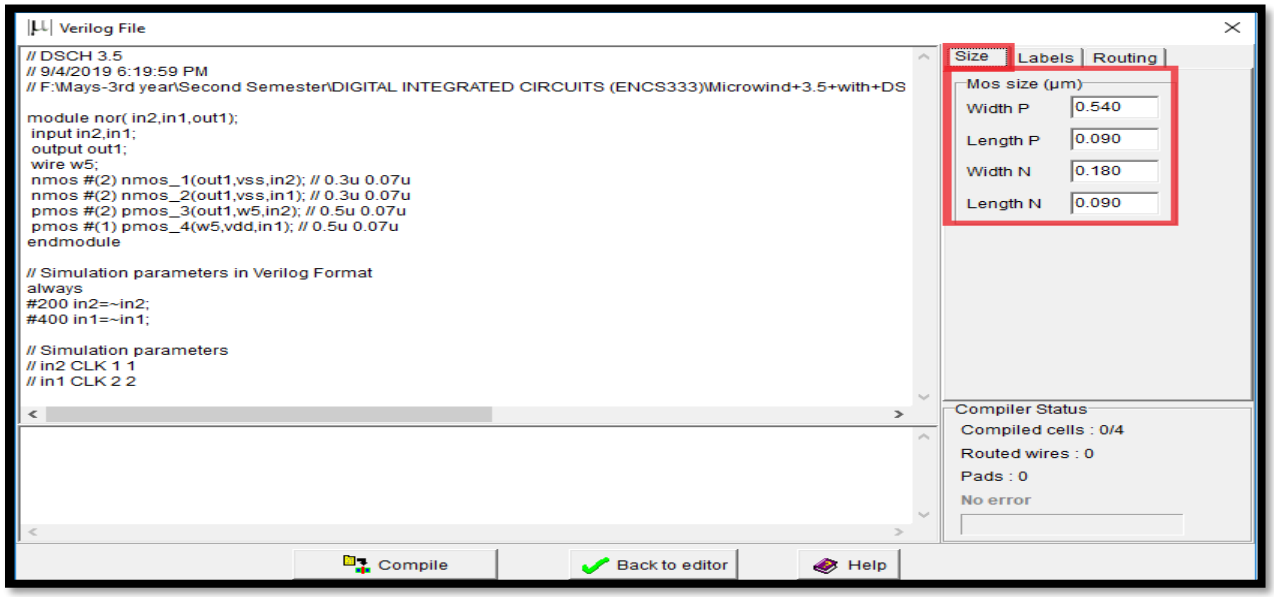


Figure 29: Verilog file window

- Click Compile and then Back to editor in the Verilog File Window. This creates a layout in layout editor window using automatic layout generation procedure.

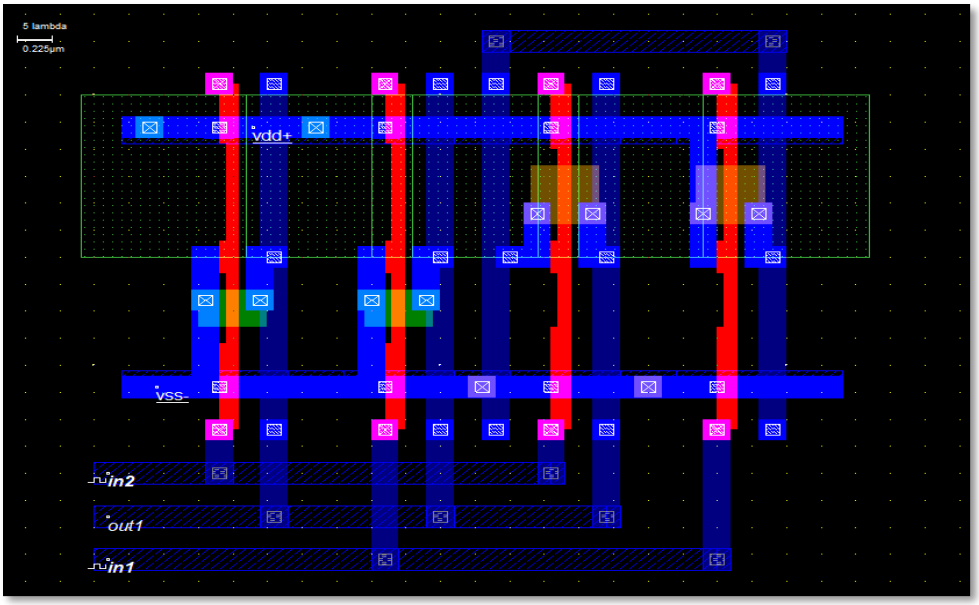


Figure 30: NOR layout using automatic layout generation procedure

- Add a capacitance to the output of the design. The value of the capacitance depends on your choice. See figure 29:

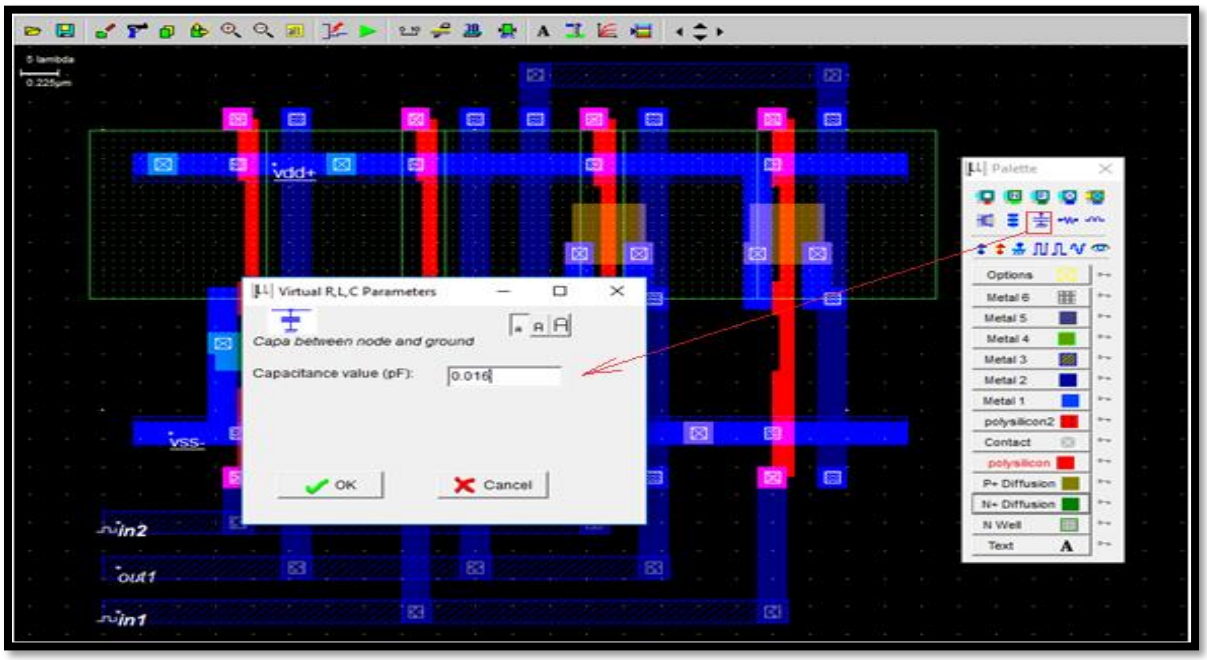


Figure 31:capacitor insertion

- Click on OK. The capacitance is shown on the left bottom corner with a value of 0.016 pF. See figure 30:

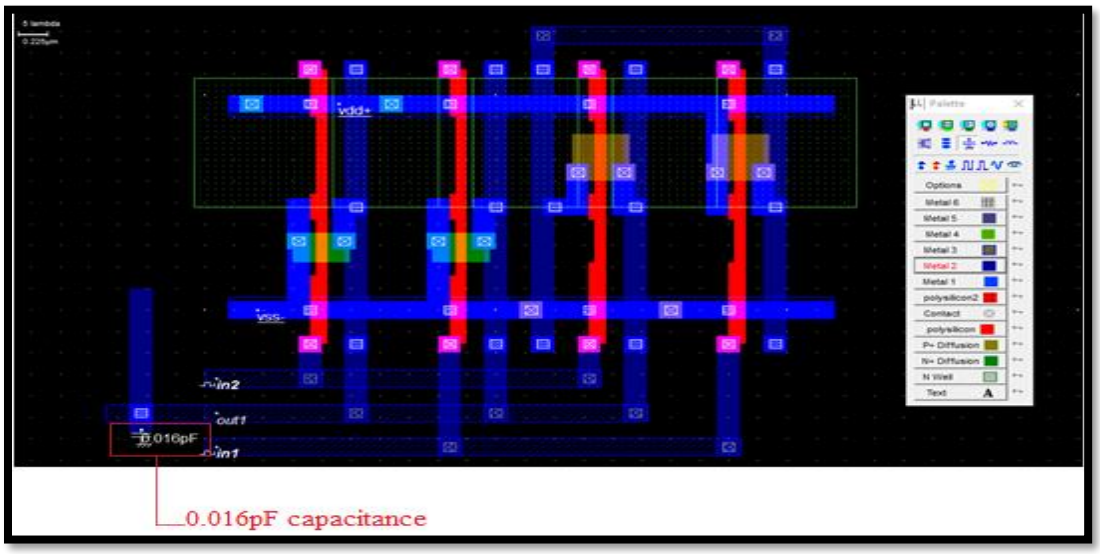


Figure 32: showing the capacitor on the layout

- Click on the label marked in1 (first input). A window appears. Click on the PWL option in the window. Insert a 01 sequence for that specific input and click on Insert. Then click on Assign. Perform this assignment on the other inputs. See figure 31:

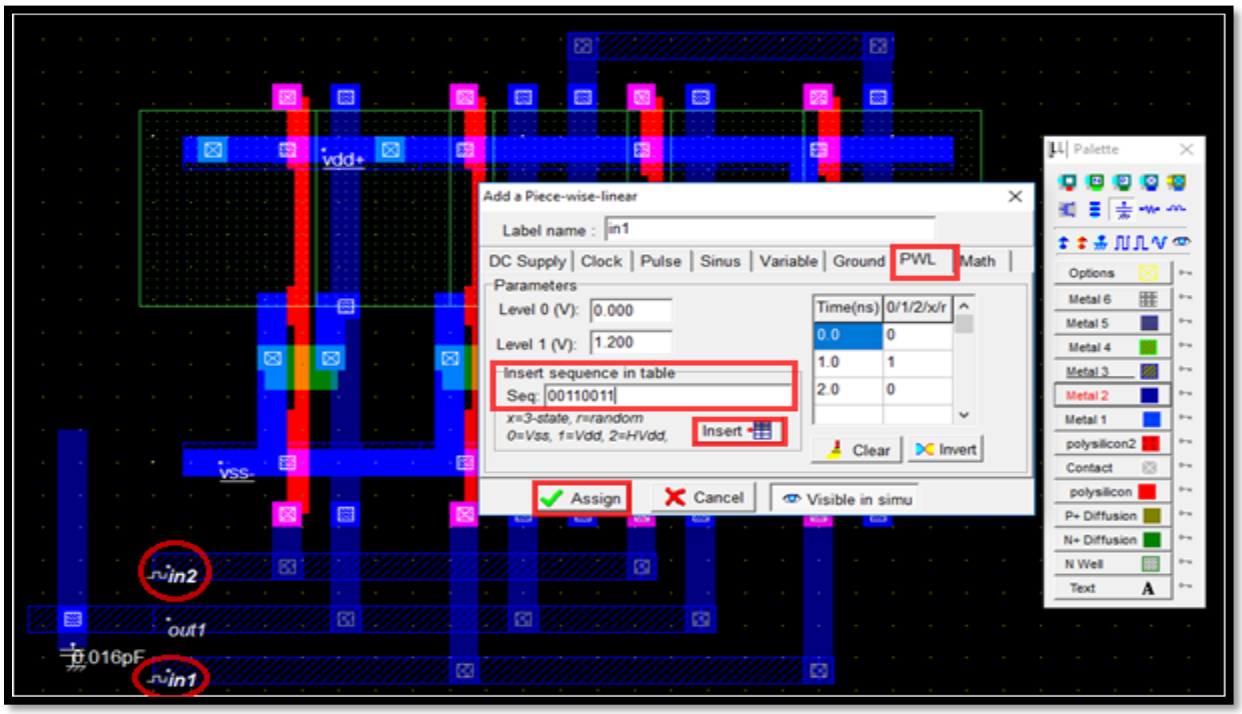


Figure 33:insert a 01 sequence

- Click Simulate -> Run simulation. A simulation window appears with inputs and output, shows the propagation delay of the circuit. The power consumption is also shown on the right bottom portion of the window. See figure 32:

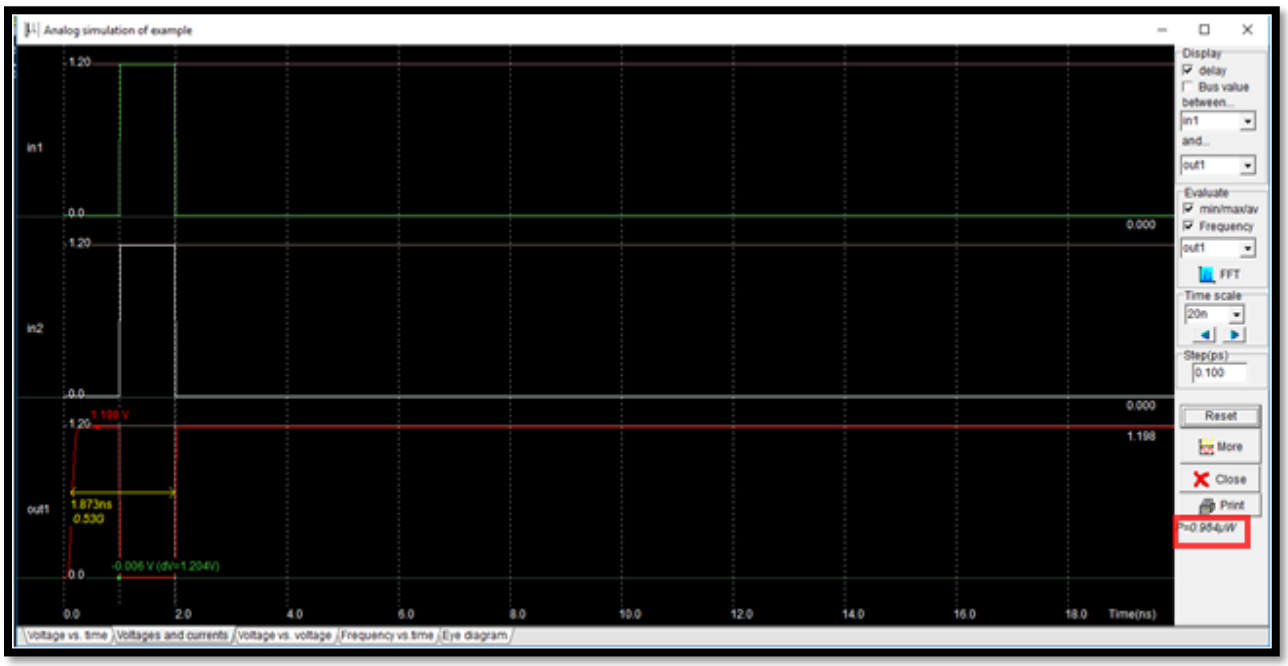


Figure 34: simulation window

- If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run the simulations till you achieve your target delays.

❖ **Design the layout manually:**

- Open the layout editor window in Microwind. Click File -> Select Foundry and select Y.rul.
- Vdd and GND rails are of Metal1. The top rail is used as Vdd and the bottom one as GND. Click on Metal 1 in the palette and then create the required rectangle in the layout window. See figure 33:

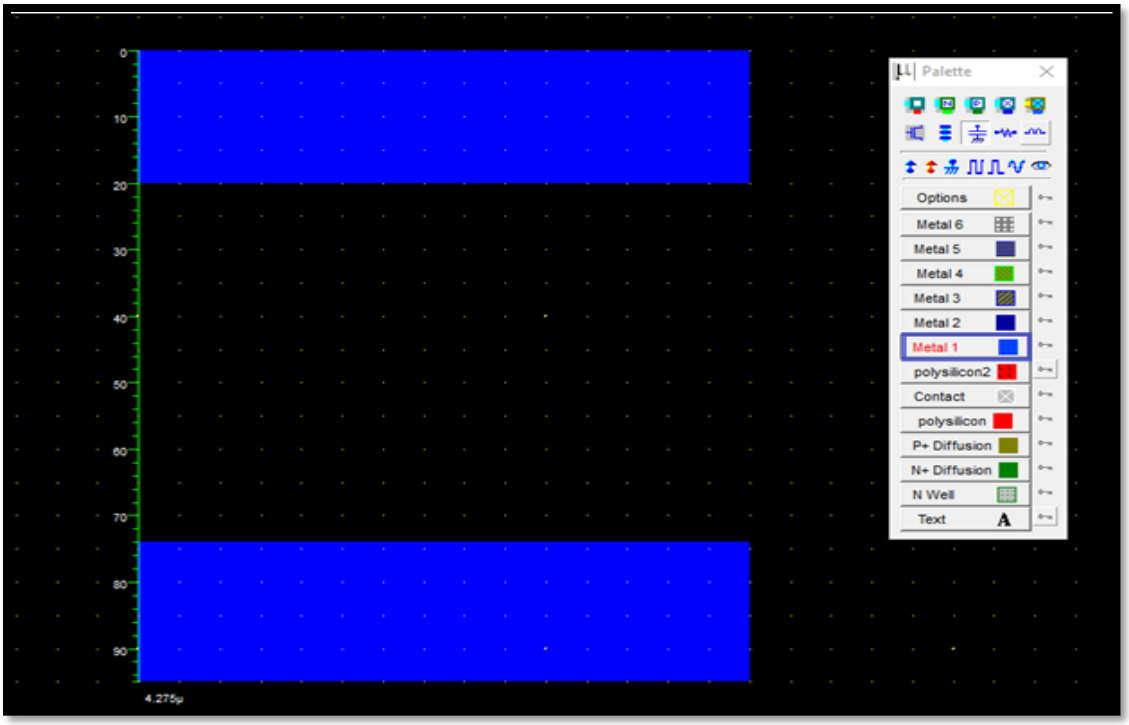


Figure 35: add metal1 for Vdd and GND

- The next step is to build the NMOS transistors. Click on the transistor symbol in the palette. Set the W, L of the transistor. See figure 34:

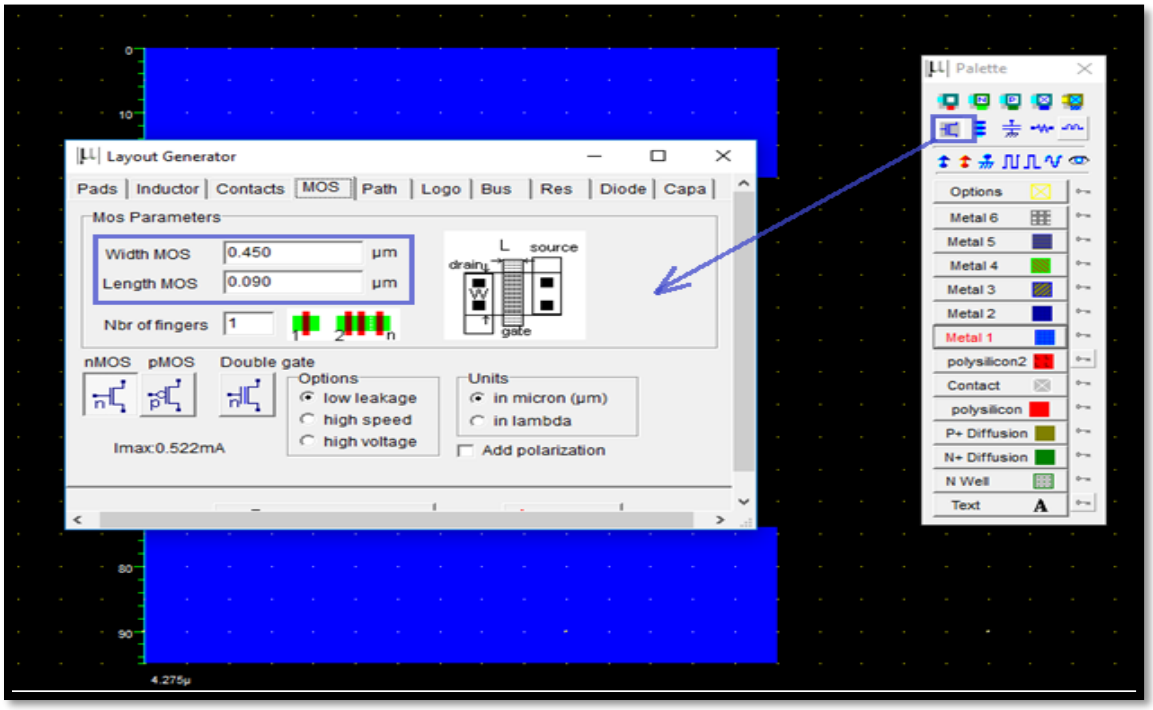


Figure 36: set W, L of the transistor

- Then click on Generate device. The source of the transistor is connected to the GND rail. See figures below:

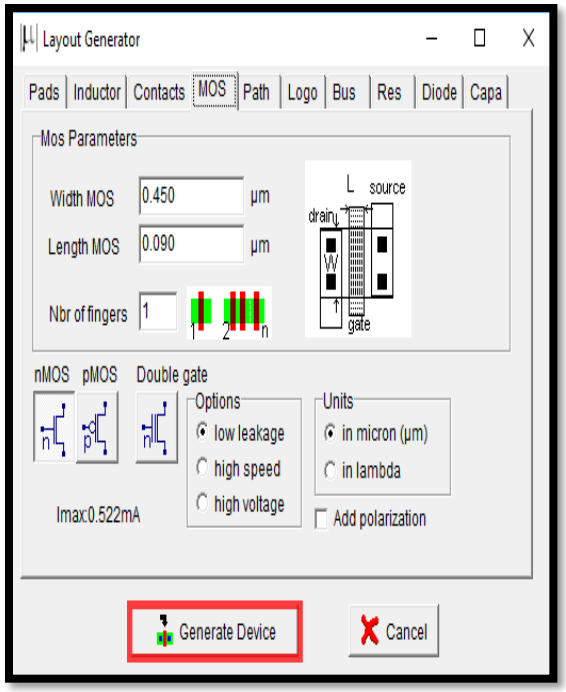


Figure 35: layout generator window

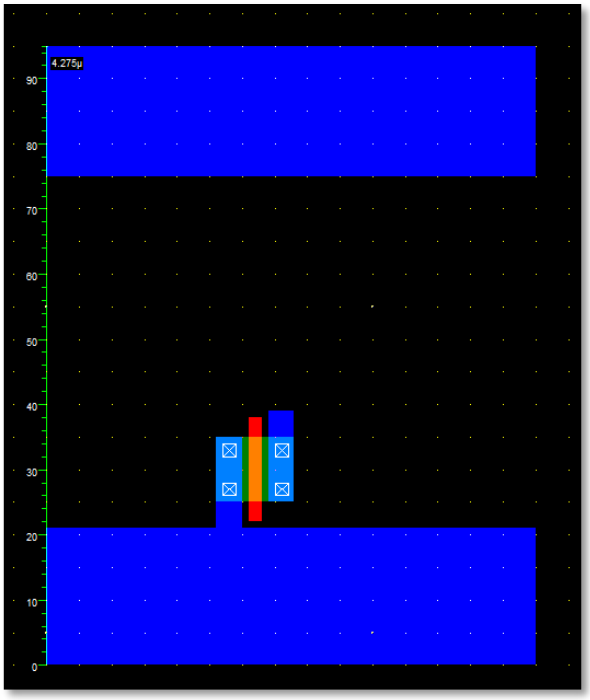


Figure 36: insert NMOS source transistor to the GND

- Create another NMOS and place it in parallel to the first NMOS device. We share the two devices' drain diffusions (by using flip horizontal from edit menu). A DRC check can be run by clicking on Analysis -> Design Rule Checker. See figure 35:

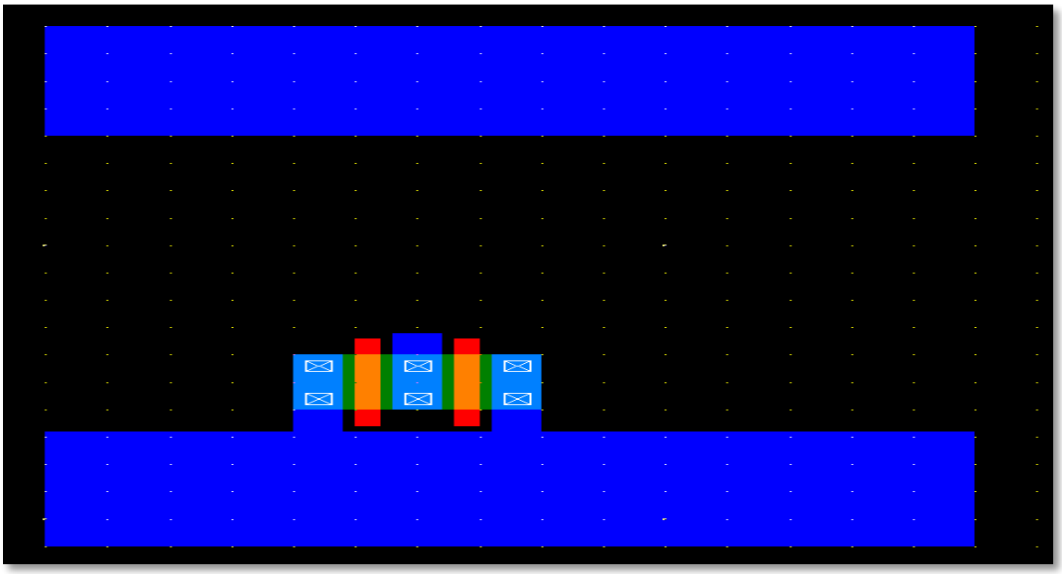


Figure 37: insert another NMOS device

- The next step is to place two PMOS transistors in series.
- Place the PMOs transistor on layout close to the Vdd rail on the top. To construct two PMOS transistors in series, diffusions are shifted to a side and another poly line is added as second transistor. The diffusion is shared to save area and reduce capacitance. See figure 36:

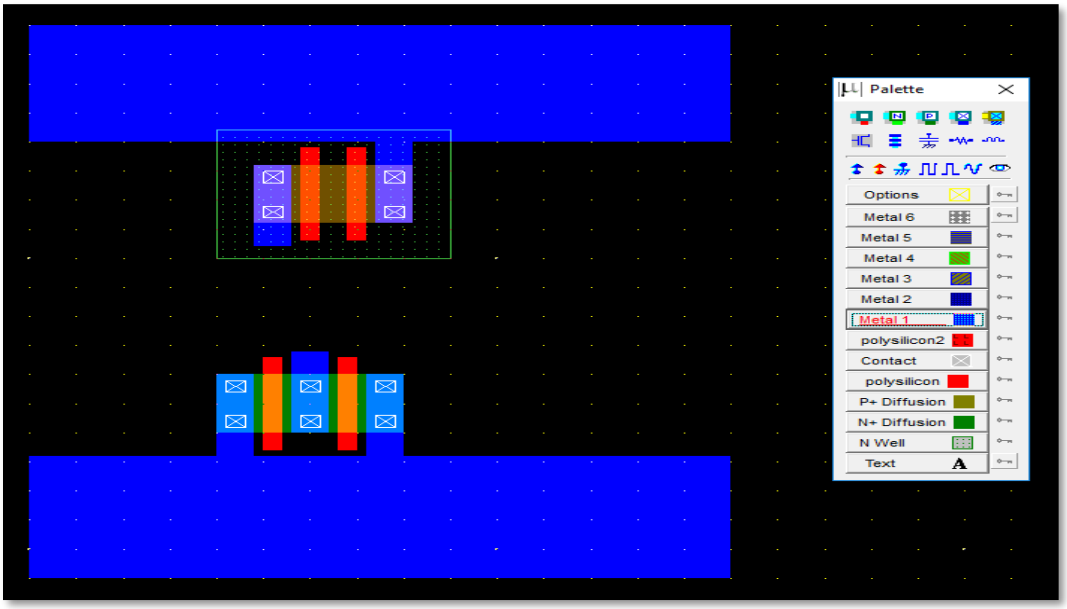


Figure 38: insert PMOS device to the Vdd

- The next step is to connect the inputs and the output of the two transistors. See figure 37:

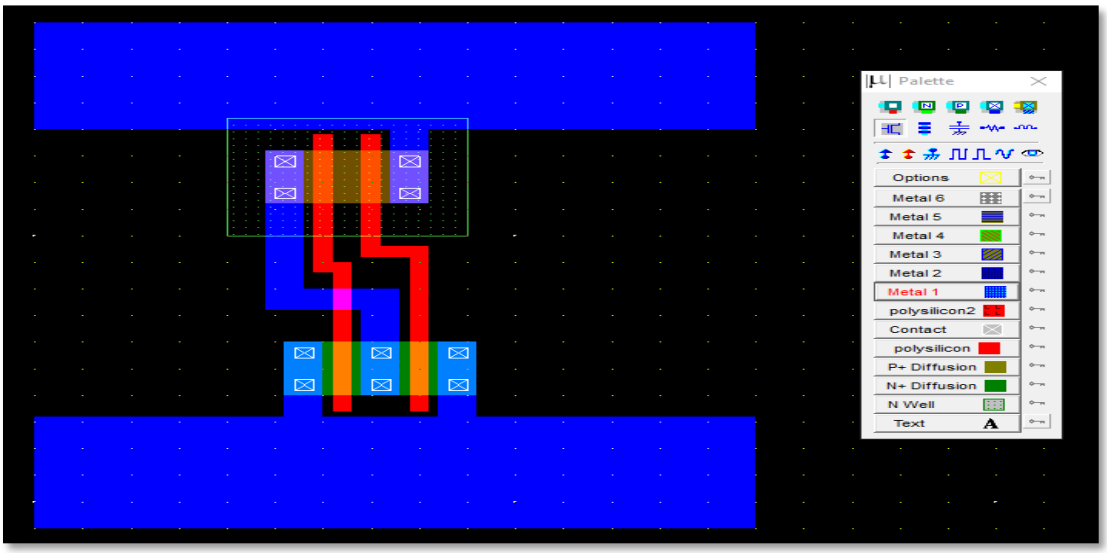


Figure 39: inputs and outputs connection

- Poly inputs are connected.
- Metal output is connected.
- The next step is to connect the poly to metal1 and then to metal2. The first symbol in the first row of the palette is the poly to metal1 contact. See figure38:

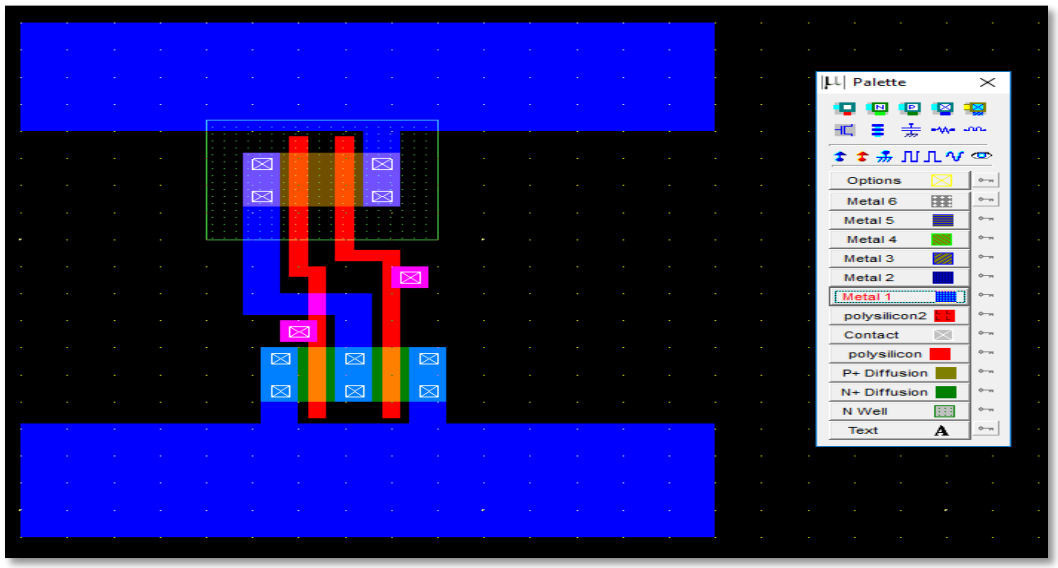


Figure 40: insert poly/metal1 contact

- Then we connect the metal1 to metal2 contact to the previous contact. This is the 4th contact on the first row.
- The next step is to connect the output Metal1 to Metal2. Once again use the 4th contact in the first row. See the figure39 below:

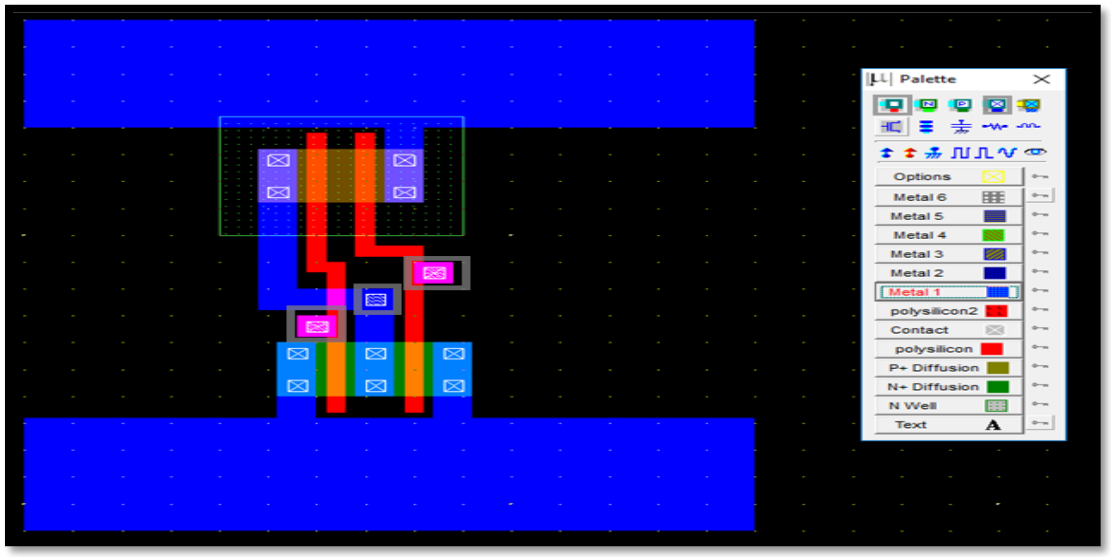


Figure 41:connect the contact (metal1/metal2)

- Now we connect metal2 to the two inputs and one output and bring them to the top to go out of the cell.
- Observe the two inputs (left & right) and an output (middle) above the Vdd rail in dark blue color. See figure 40:

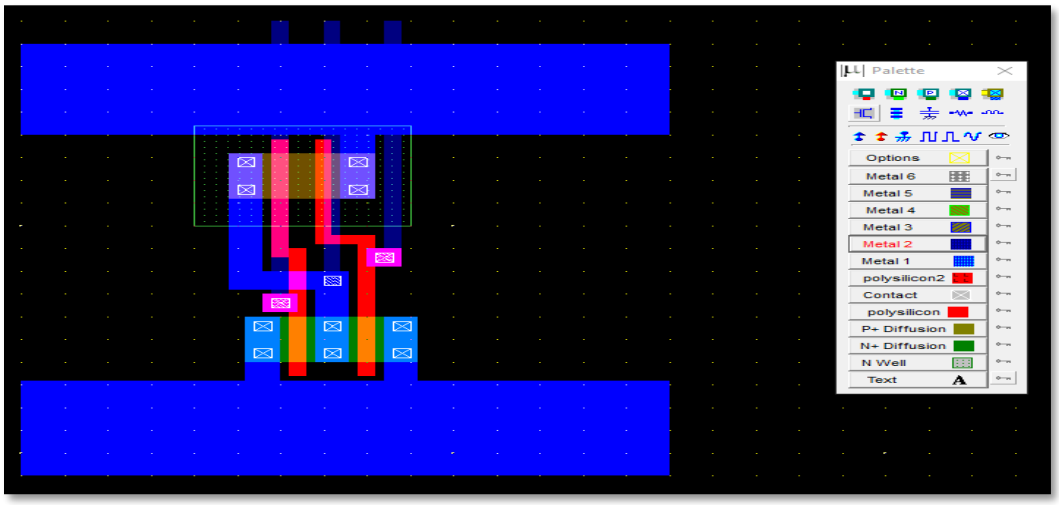


Figure 42: connect metal2 to inputs and output

- Now we label the inputs and output as in1, in2 and out1. Click on Add a Pulse Symbol in the palette (5th from the left in the 3rd row). Then click on the metal2 of one of the inputs. A window appears. Change the name of the input signal. Insert 01 sequences and click on Insert. The click on Assign. Similarly assign the 2nd input a pulse. See figure 41:

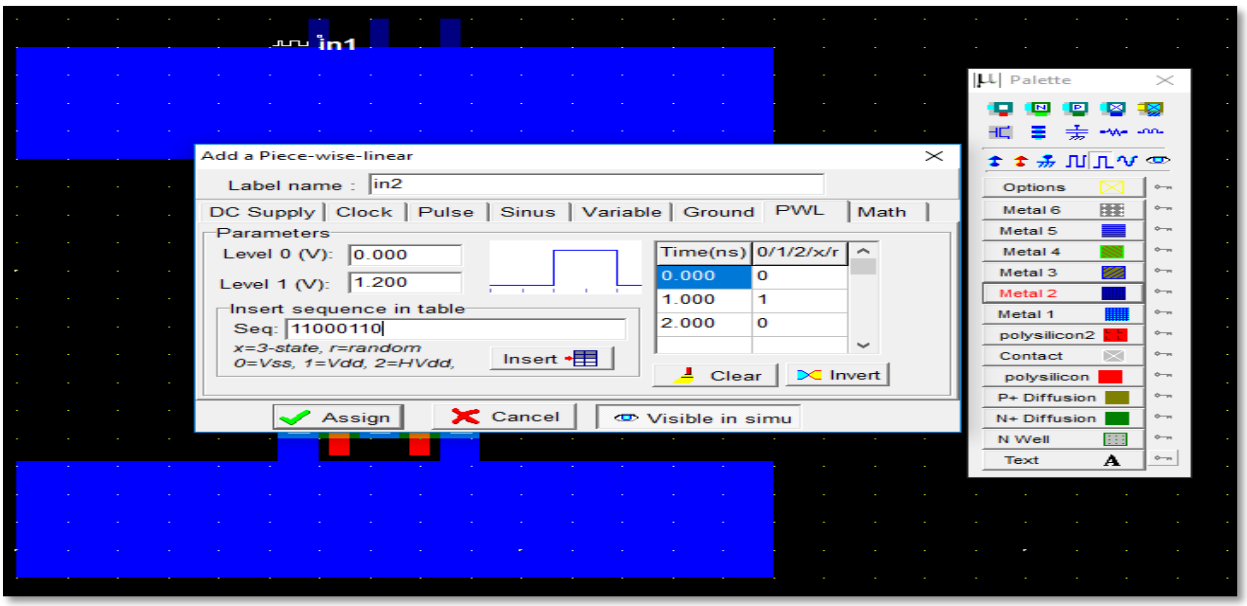


Figure 43: add pulses to the inputs

- Now select the Visible Node symbol from the palette (7th in the third row). Select it and click on the output. The 'Add a Visible Property' window appears. Change the label name to out1. Select Visible in Simulation. Click on Assign. Now the output is also labeled. See the two figures below:

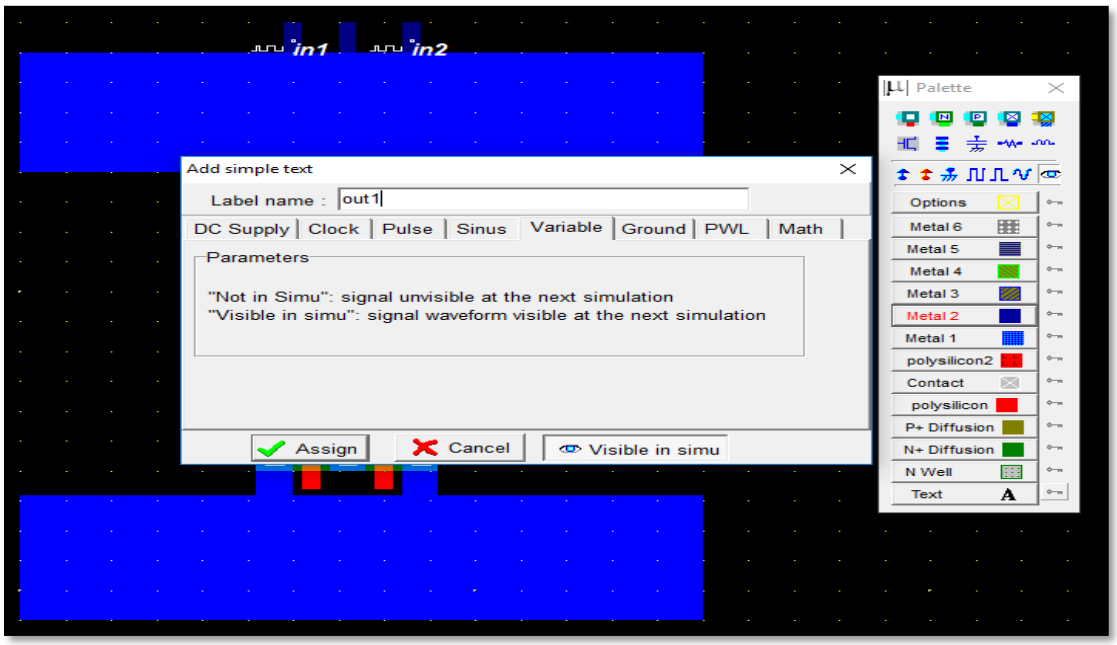


Figure 44: label the output

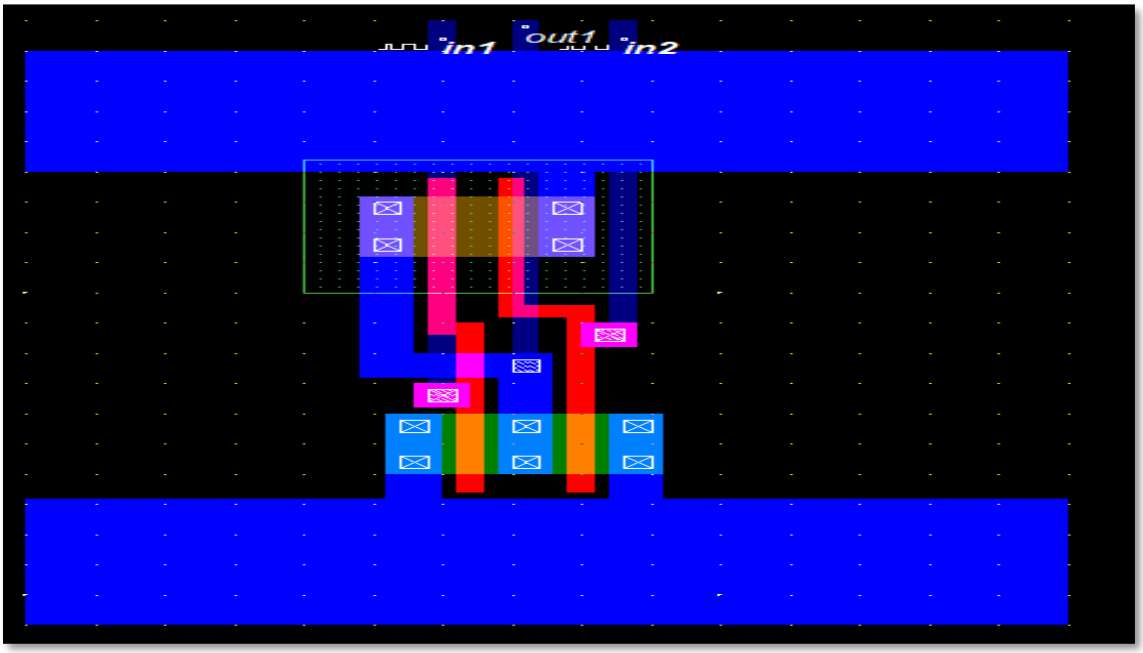


Figure 45: inputs & output are labeled

- Select Vdd Supply and GND from the palette (third row). Also click on the capacitor (3rd in 2nd row) symbol and add it to the output. Also, extend the pwell into the Vdd Rail. The click on Edit -> Generate -> Contacts. Select PATH and then in Metal choose Metal1 and N+ polarization. See figure44:

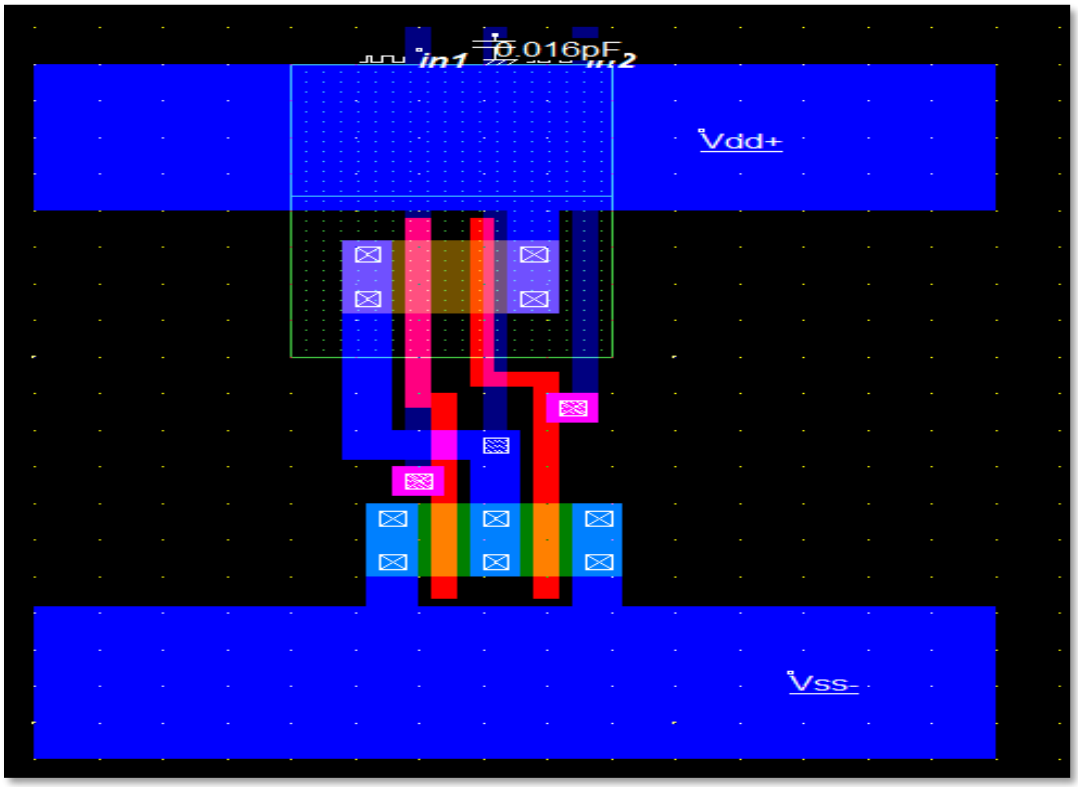


Figure 46: full layout

- To run the Simulation of your circuit, click on Simulate -> Start Simulation. Depending on the input sequences assigned at the input the output is observed in the simulation. The power value is also given.
- **You should know that I didn't depends the rules in the example. I just see you how to deal with the program through an example.**
- **About the design rule checker, you can take the dimensions of the design in details from help menu. Also, if you want to check the rules click on the design rule checker icon from the icon bar.**

➢ Notes:

- You can build the MOS transistors then use it in your layout. So, there is many different ways to build your layout manually not only the way that is explained before.

- **I want to give you an advice, while the program do the simulation don't try to stop the simulation or close it to avoid the tool damage.**

- If you do this example, you can do any example if you know the circuit. I gave you a background about the tool and its use and I hope you take a good utility. Also, I am sorry if there are any mistakes that I don't notice it.
- I attached you below some circuits for different basic gates, see them and try to build them in DSCH & Microwind. Good Luck

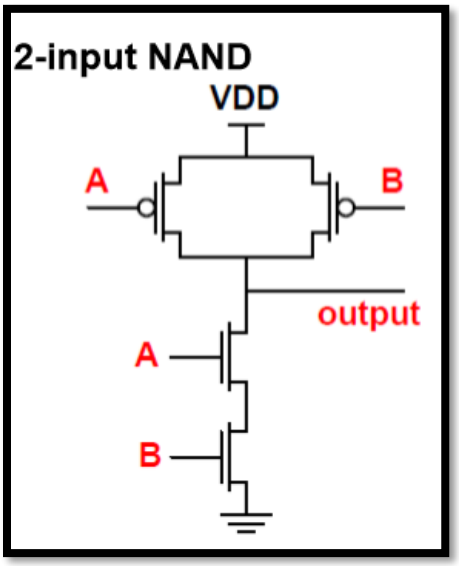


Figure 47: 2-input NAND

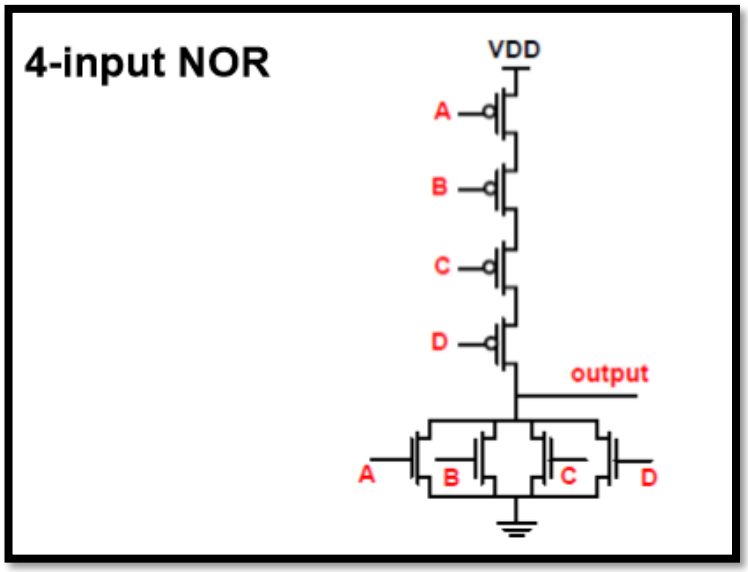


Figure 48: 4-input NOR

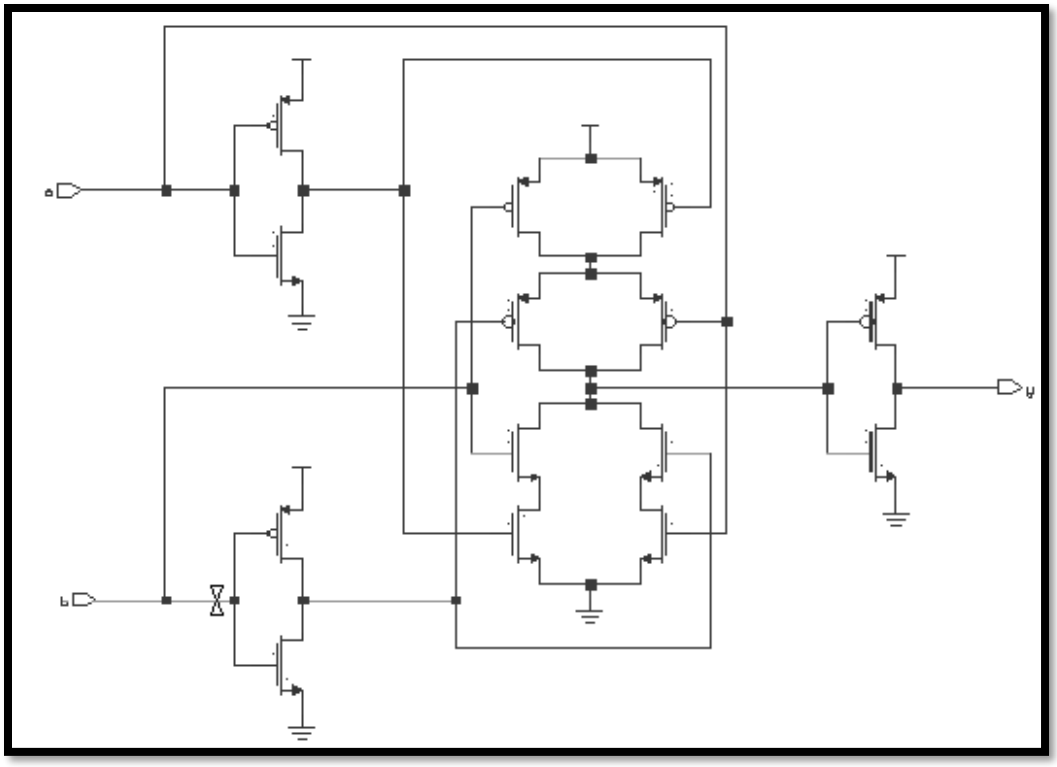


Figure 49: 2-input XOR