



Faculty of Engineering
Electrical and Computer Engineering Department
Integrated Circuits

IC Homework #1

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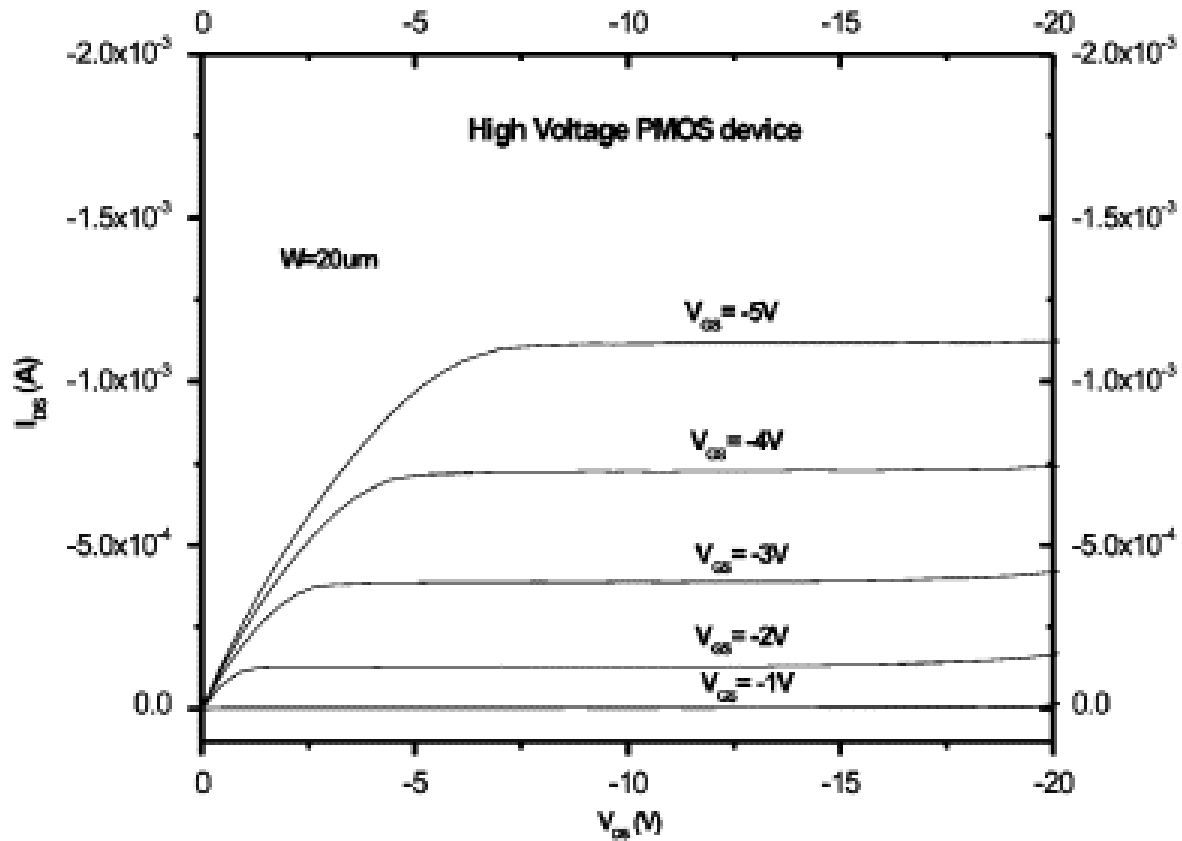
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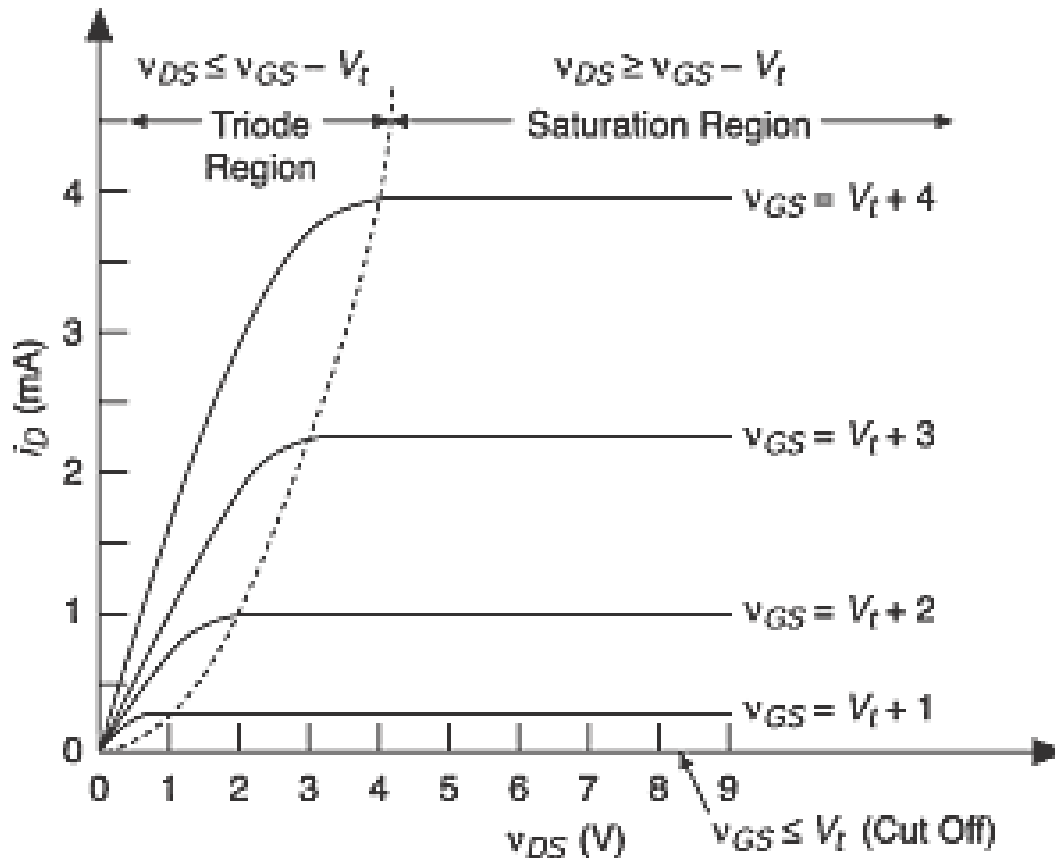
Q1: Cmos: known as Complementary metal–oxide–semiconductor, is a technology of constructing integrated circuits.

CMOS transistors work usually as switches that goes on and off which gives us the ability to construct many logic gates.

PMOS:



NMOS:



Q2: In high frequencies, Capacitance parasitic appears clearly, and we need to deal with it once it causes problems.
Inductance appears as Capacitance in high frequencies.

Q3: IC technology is getting smaller (Length in CMOS transistors is getting smaller) which leads to faster devices. However, it consumes more power (The power actually becomes 3 times more every 10 years).

Q4: IC fabrication steps:

- a. Wafer production
- b. Masking
- c. Etching
- d. Doping
- e. Metallization
- f. Assembly and packaging

Q5: Power is discussed in question 2. Area is getting smaller and smaller over time. ICs are getting faster because of shrinking the the process. Timing.

Q6: Inductance, capacitance and resistance parasitic

Q7: To define the process node, a process must be defined. A process is: set of steps to make an integrated circuit with transistors that meet a certain range of performance and size characteristics.

The process node is: is a standardized process used across a wide range of products. Standardizing the process for multiple products makes yield and process improvement much easier, since the same resources can solve complex problems