

 **Faculty of Engineering**

**Electrical and Computer Engineering Department**

 **Integrated Circuits desgin**

IC homework#2

 Student name:

 Mohammad Mouadi

 Student ID:

 1162246

 Instructor name:

D. Khader mohammad

1. Wn / Wp = µp/ µn
2. a **hole** is an electric charge carrier with a positive charge, equal in magnitude but opposite in polarity to the charge on the electron
3. A.
4. reduce the complexity of the circuit

b. low static power consumption

c. high noise immunity

B. The main **advantage** of **CMOS** technology **over** **NMOS** technology is the power dissipation.

1. In the second scenario, the two transistors in the bottom will work together in parallel which means less resistance. Thus, the second scenario has less delay.
2. Attached.
3. By observation and logical thinking

F(A,B,C,D,E,F,G)=AC+ADG+BC+CDFE+FEG+BDG

1. D terminal is at the top and S terminal is at the bottom.
2. VGS<VDS + VT 🡪 1.9 < 2.5 + 0.4 🡪 saturation
3. VGS>VDS + VT 🡪 4.5 < 2.9 + 0.4 🡪 non-saturated
4. VGS=VDS + VT 🡪 3.4 = 3 + 0.4 🡪 in between saturation and non-saturated.
5. Once VGS>VDS+VT, transistor is in saturation region



Id=100\*3(1.8-0.6)^2 = 432 µA = 0.432 mA

VDS=3-Id\*R=3-2.16=0.84 Volts

1. It is the same as the previous question.
2. Answer:
3. VG > VD + Vt 🡪 0 > 0 -0.4 🡪 saturation
4. Once VGS > Vt the transistor is off.
5. VG < VD + VT 🡪 -2.5 < -1.1 – 0.4 🡪 linear
6. pMOS transistor is in saturation region



Id=100\*4\*(-3.5 + 1)^2 = 2.5 mA

V0 = Id \* R = 2.5 mA (on the resistor)

VDS = V0 – VS = -4.5 Volts