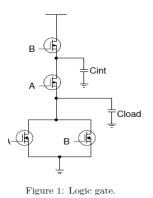


## Electrical and Computer Systems Engineering Department ENCS333 Homework 2

Due October 11<sup>th</sup>

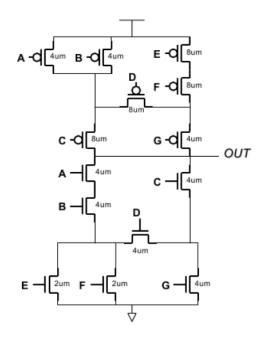
- 1- If a designer wants a perfectly balanced rise time and fall time for a CMOS inverter driving a capacitive load, what should the ratio of NMOSFET to PMOSFET transistor widths be?
- 2- In the context of digital integrated circuits, what are holes? Use three or fewer sentences.
- 3- List three advantages of CMOS over NMOS, and one advantage of NMOS over CMOS.
- 4- Delay depends on the input patterns. Consider Figure 1.
- In input pattern P, inputs A and B are each low for a long time, then input B transitions instantly to VDD.
- In input pattern Q, inputs A and B are each low for a long time, then both transition to VDD simultaneously and instantly. Which input pattern results in more delay? Explain why



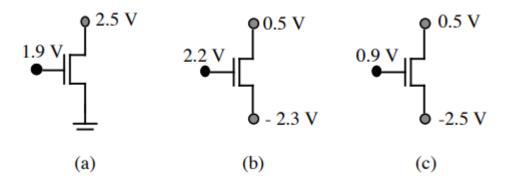
5- Show the circuit diagram for the function below using pass gate with output buffer or inverter.

$$f(a, b, c) = ab + \overline{a}\,\overline{b}\,\overline{c}$$

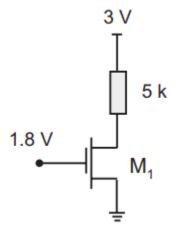
6- Use default parameters unless alternate values are given. Write a logic equation for this complex gate.



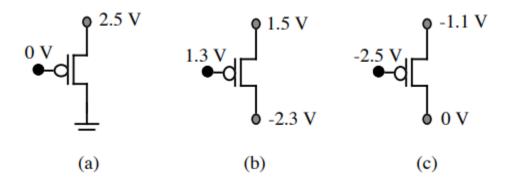
7- Determine the bias state (Region of operation) for the three circuit conditions if Vtn = 0.4
V. The source voltage is always lower than the drain voltage in an nMOS transistor. First identify the correct terminals.



8- Calculate ID and VDS if Kn = 100  $\mu$ A/V2 , Vtn = 0.6 V, and W/L = 3 for transistor M1.



- 9- Repeat Q8 above finding ID and VDS if VG = 1.8 V
- 10- Determine the bias state for the pMOS transistors where Vtp = -0.4 V. It is helpful with pMOS transistors to first identify and label the source and drain terminals. The source terminal in a pMOS transistor has a higher voltage than the drain terminal.



11-Calculate ID and VDS for Vtp = -1.0 V, Kp =  $100 \ \mu$ A/V2 , and W/L = 45 V

