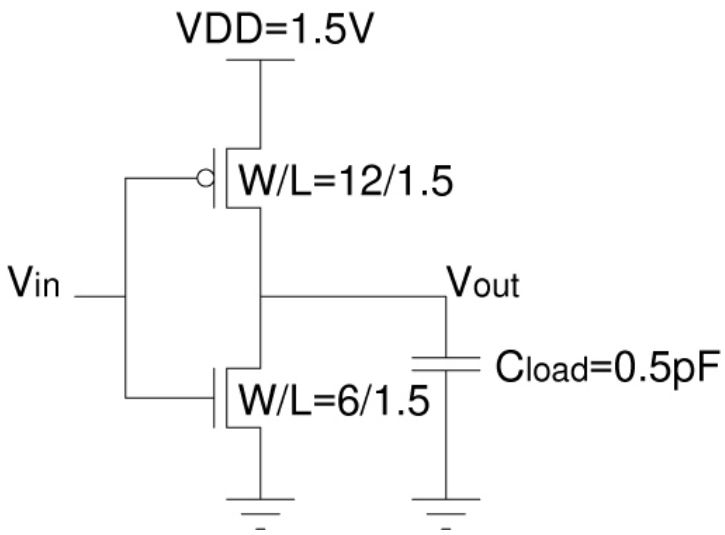
Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.012
Microelectronic Devices and Circuits
Spring 2007
March 16, 2007 - Homework #4
Due - March 23, 2007

Problem 1

Consider the CMOS inverter pictured below. Take channel length modulation into account.



Parameter	NMOS	PMOS
V_{TO}	0.5 V	-0.5 V
μ	220 cm^2/Vs	110 cm^2/Vs
λ	0.1 V^{-1}	0.1 V^{-1}
T_{ox}	15 nm	15 nm

• Dimensions of W and L are in µm

a) Calculate V_M, the voltage midpoint.
b) Calculate A_V, the voltage gain at $V_{in}=V_M$.
c) Calculate N_{ML} and N_{MH}, the noise margin low and noise margin high.
d) Calculate t_{PHL} and t_{PLH}, the propagation delay from high-to-low and propagation delay from low-to-high.

a) We set the drain current of the PMOS equal to the drain current of the NMOS, and plug in $V_{in}=V_{out}=V_M$.

V_M=0.75V

b) Voltage gain, Av= -(g_{mn}+g_{mp})*(r_{on}||r_{op})
g_{mn}=g_{mp}=50µS
r_{on}=r_{op}=1.47MΩ
A_v=-74

c)NM_L=V_M + (V_{DD}-V_M)/A_V=0.74V
NM_H= V_{DD}-V_M + V_M/A_V=0.74V

d) propagation delay = ΔV*C/ I
ΔV = 0.75V = 50% of the total value
C= 500fF
$I_{D,pmos}$=$I_{D,nmos}$= 202µA

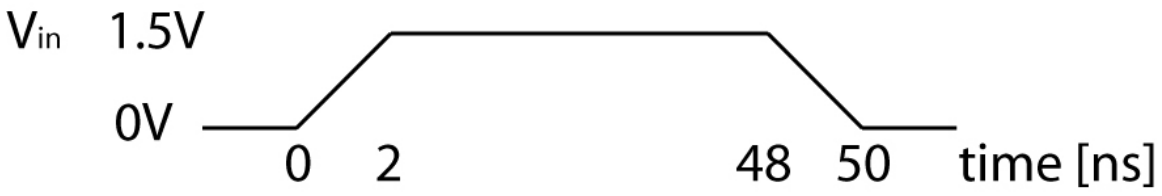
$T_{PH=}T_{PL}$ =1.856ns

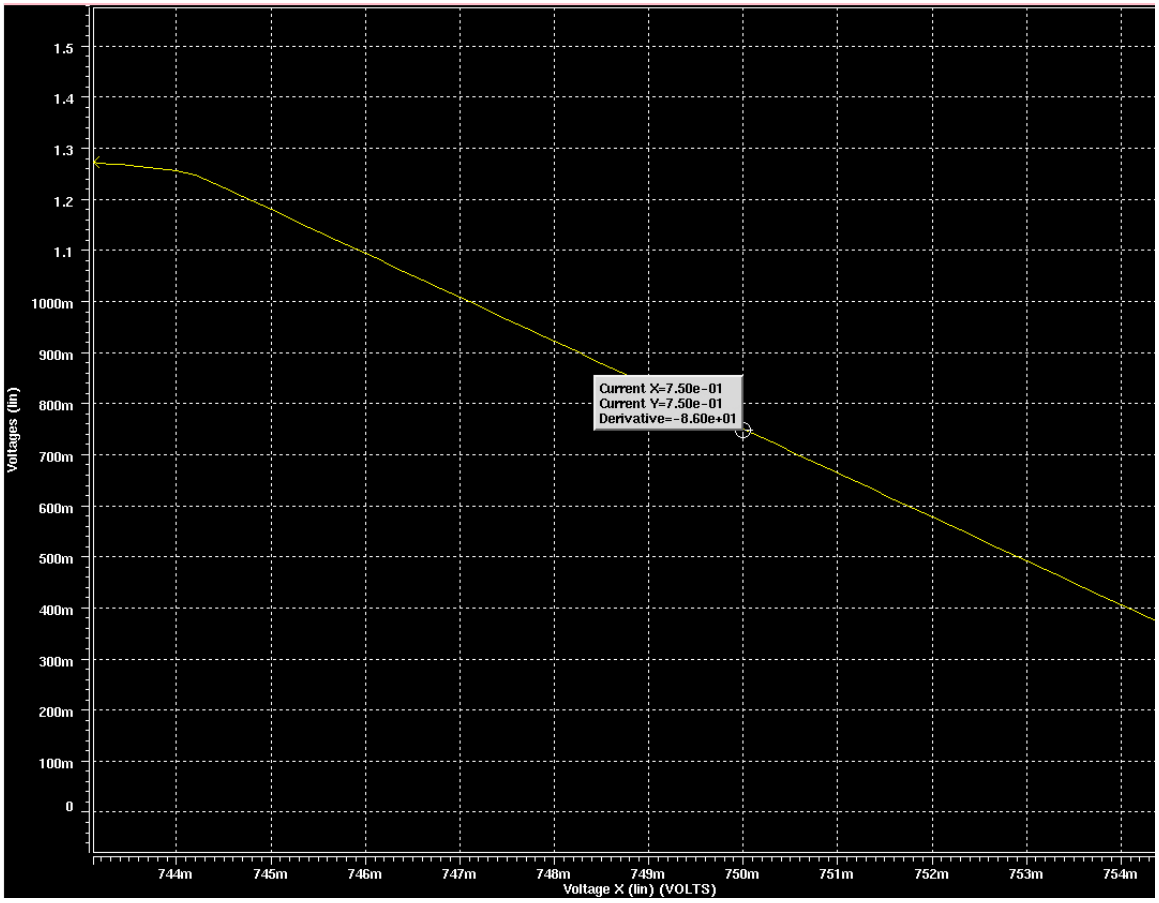
Problem 2

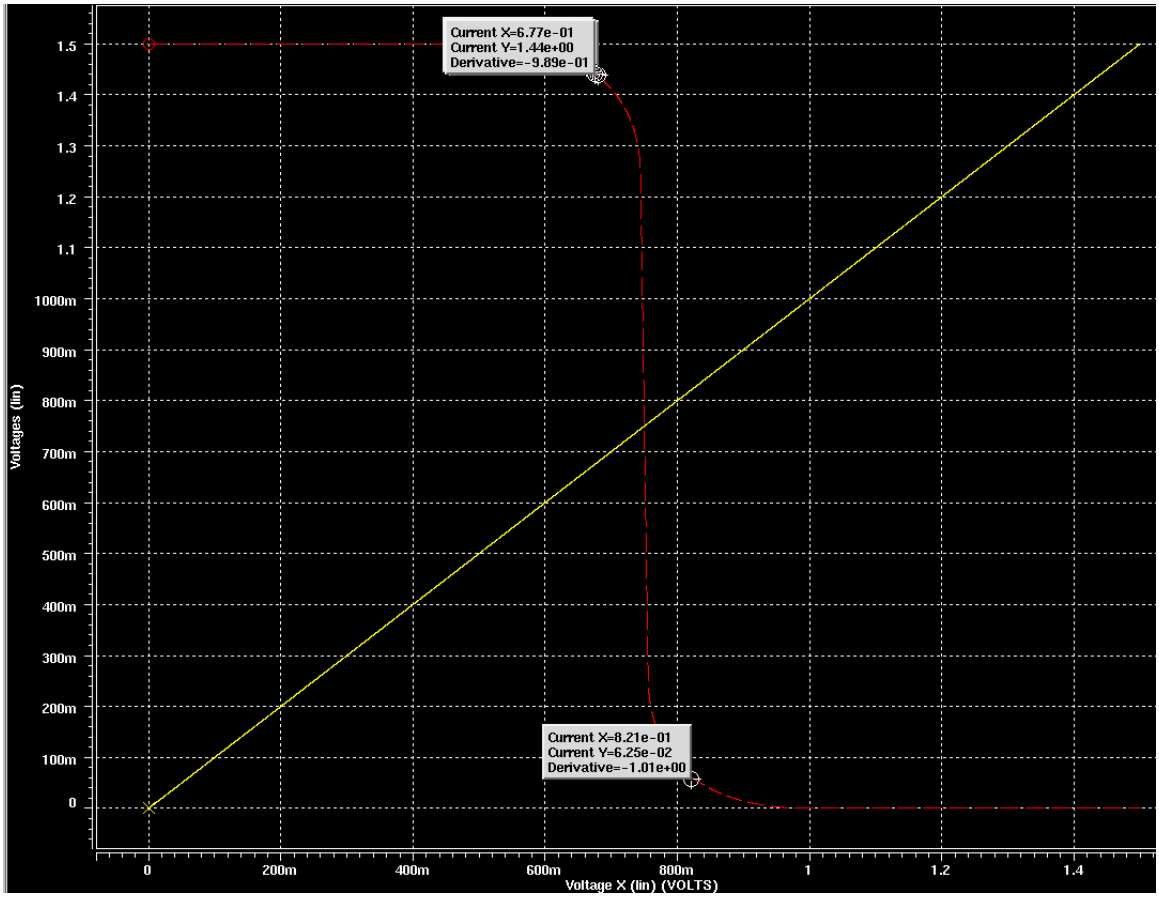
We will now use the following SPICE model and compare our hand calculations from Problem 1 with simulated results.

```
.MODEL N15 NMOS LEVEL=1 VT0=0.5 TOX=1.5e-8 U0=220 LAMBDA=1.0e-1
+GAMMA=0.6 CJ=1e-4 CJSW=5e-10 PB=0.95
.MODEL P15 PMOS LEVEL=1 VT0=-0.5 TOX=1.5e-8 U0=110 LAMBDA=1.0e-1
+GAMMA=0.6 CJ=3e-4 CJSW=3.5e-10 PB=0.9
```

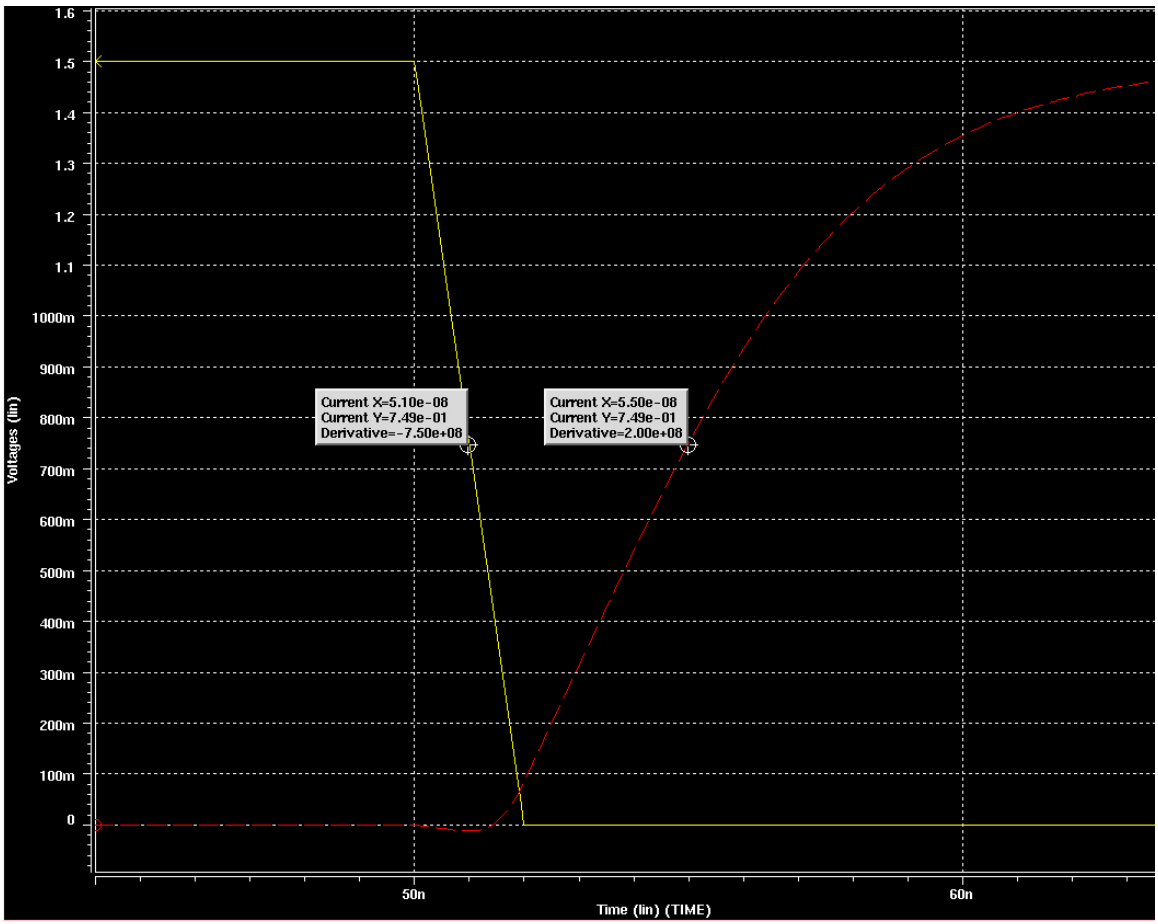
a) Use the DC sweep on the input voltage to simulate transfer characteristics using SPICE. Compare V_M, A_V, N_{ML}, N_{MH}, with the calculated results.
b) Use the Pulse input to simulate an input waveform shown below using SPICE. Compare t_{PHL} and t_{PLH} with your hand calculations.

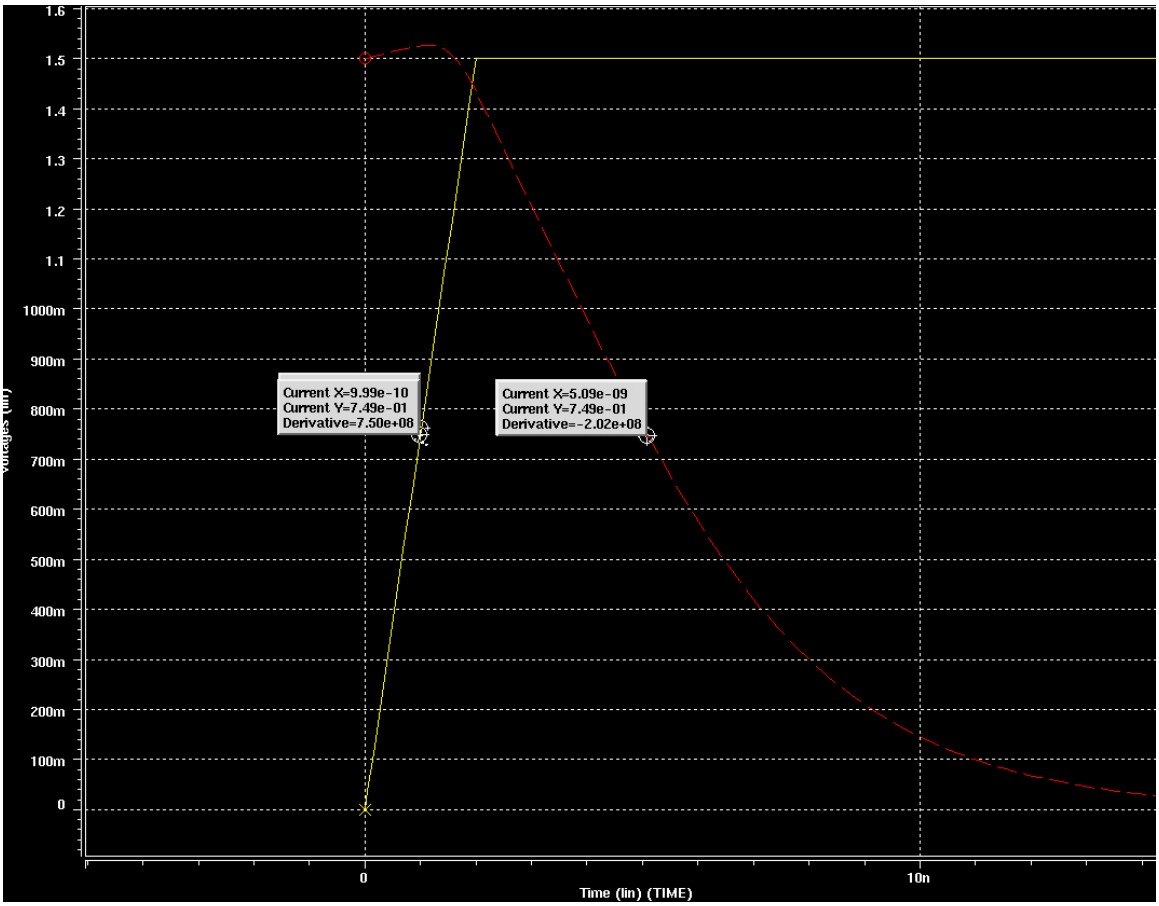



1.5
1.4
1.3
1.2
1.1
1000m
900m
800m
700m
600m
500m
400m
300m
200m
100m
0
Voltages (lin)
Current X=7.50e-01
Current Y=7.50e-01
Derivative=-8.60e+01
744m
745m
746m
747m
748m
749m
750m
751m
752m
753m
754m
Voltage X (lin) (VOLTS)



We see V_M=0.75V.
$N_{ML} = V_{IL}-V_{OL} \sim 0.677V-0.0625V=0.615V$
$N_{MH} = V_{OH}-V_{IH} \sim 1.44V-0.821V=0.619V$


1.6
1.5
1.4
1.3
1.2
1.1
1000m
900m
800m
700m
600m
500m
400m
300m
200m
100m
0
Voltages (lin)
Current X=5.10e-08
Current Y=7.49e-01
Derivative=-7.50e+08
Current X=5.50e-08
Current Y=7.49e-01
Derivative=2.00e+08
50n
60n
Time (lin) (TIME)



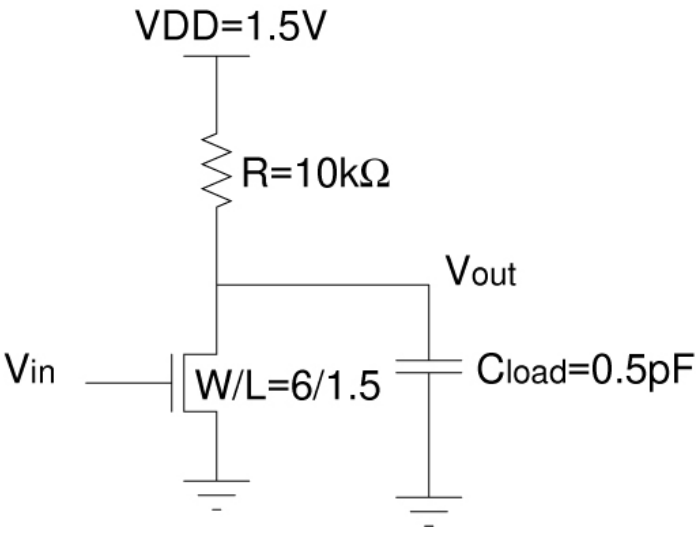
t_{PLH}~4ns

t_{PHL}~4.1ns

Problem 3

Consider the circuit below, which consists of an NMOS device and resistor load. Disregard channel length modulation for this problem.

a) Calculate V_M, V_{OH}, V_{OL}. Remember, for hand calculations we assume $V_{OH}=V_{MAX}$, and $V_{OL}=V_{MIN}$.
b) Calculate the voltage gain of this circuit, when $V_{in}=V_M$.



a) Set the current through the resistor equal to the current through the NMOS, with $V_{in}=V_{out}=V_M$.

$$\frac{V_{DD}-V_M}{R}=\frac{1}{2}\frac{W}{L}\mu C_{ox}\left(V_M-V_{Tn}\right)^2$$

V_M= 1.16V

When the input is 0V (low), the NMOS is in cutoff, so no current flows. Therefore, $V_{OH}=V_{MAX}$=1.5V

When the input is 1.5V (high), the NMOS is in triode. We must solve as we did earlier, setting the current through the resistor equal to the NMOS in triode. V_{in} is set to 1.5V.

$$\frac{V_{DD}-V_{\min}}{R}=\frac{W}{L}\mu C_{ox}\left(V_{DD}-\frac{V_{\min}}{2}-V_{Tn}\right)V_{\min}$$

$V_{OL}=V_{MIN}$=0.63V

b) The small signal gain of this circuit is $-g_m*R$.

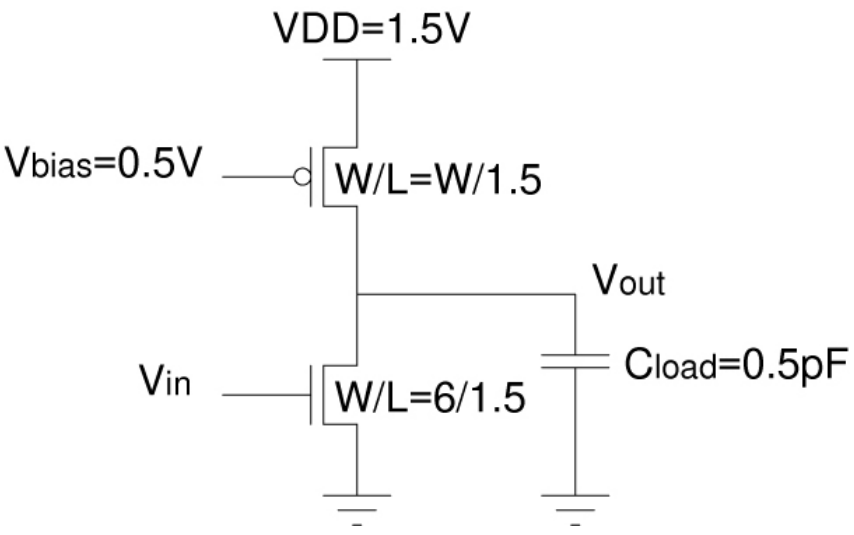
$$g_m=\sqrt{2\frac{W}{L}\mu C_{ox}I_{DSat}}=1.34\text{mA/V}$$

A_V=-1.34

Problem 4

Consider the circuit below, which consists of an NMOS device and PMOS current source load. *Do not* neglect channel length modulation.

a) Calculate the width of the PMOS device so its saturation current is 50μA.
b) Calculate V_M, V_{OH}, V_{OL}. Remember, for hand calculations we assume $V_{OH}=V_{MAX}$, and $V_{OL}=V_{MIN}$.
c) Calculate the voltage gain of this circuit, when $V_{in}=V_M$.



a) $50\mu A = \frac{1}{2}\frac{W}{1.5}\mu_p C_{ox}(1-0.5)^2$

Width of device, W =23.7 microns

b) Setting the saturation drain current of the NMOS equal to that of the PMOS, we find

V_M=1.175V

When the input is low, the NMOS is in cutoff, therefore
$V_{OH}=V_{DD}$

When the input is high, the NMOS is in triode. Setting the current through the NMOS equal to the PMOS,

$$\frac{1}{2}\frac{23.7}{1.5}\mu_p C_{ox}(1-0.5)^2(1+.1(V_{DD}-V_{\min})) = \frac{6}{1.5}\mu C_{ox}\left(V_{DD}-\frac{V_{\min}}{2}-0.5\right)V_{\min}$$

$V_{MIN}=V_{OL}= 0.33V$

c) For this circuit, the voltage gain is $-g_{mn} * (r_{on}||r_{op})$

$$g_m = \sqrt{2\frac{W}{L}\mu C_{ox} I_{DSat}} = 0.144 \text{ mA/V}$$

$$r_{on} = r_{op} = \frac{1}{\lambda I_D} \rightarrow I_D = 50\mu A \ , \ r_o = 200k\Omega$$

$A_v=-14$