1. **Please read the attached paper , using Microwind tool Design and simulate :**

* Inverter
* Design of CMOS OR gate
* CMOS AND gate
* NMOS 2:1 multiplexer

**Show the waveforms for input and output**

**Report total area for each design**

**Report delay for each gate**

**In your report, need to turn in:**

* **Show the waveforms for input and output**
* **Report delay/Area for each gate as shown in table below**
* **Layout**

|  |  |  |  |
| --- | --- | --- | --- |
| **Spice** | **Delay** | **Output slope (Fall)** | **Output slope (rise)** |
| **Inverter** |  |  |  |
| OR gate |  |  |  |
| AND gate |  |  |  |
| 2:1 multiplexer |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Layout** | **Area** | **Delay** | **Output slope (Fall)** | **Output slope (rise)** |
| **Inverter** |  |  |  |  |
| OR gate |  |  |  |  |
| AND gate |  |  |  |  |
| 2:1 multiplexer |  |  |  |  |

* Extra point for those who do that for more than one process and compare the results:
  + 65nm
  + 45nm
  + 22nm
  + 10nm
* Resources :
* Watch these videos : https://www.youtube.com/watch?v=T1oT6MLW9ZI