



Electrical and Computer Systems Engineering Department

ENCS333

Due October 23rd

HW 3: Layout design of a CMOS Inverter

Objectives: manually design the mask layout of a CMOS inverter. check the design for design rule errors. check the functionality of the inverter using simulation with the built-in simulator. extract netlist from the inverter layout for SPICE.

This assignment has 3 parts:

Part 1:

You need to build inverter using 35nm process and do spice simulations. You need to size the p an n device to have equal rise and fall time.

Simulate the inverter in spice and turn on snapshot of schematic, size (show how you do calculation ...etc and spice based simulation wave form showing delay, rise and fall time

Part 2:

Need to build the layout manually in Microwind, generate the netlist and simulate the design .

You need to turn in snapshot of layout showing:

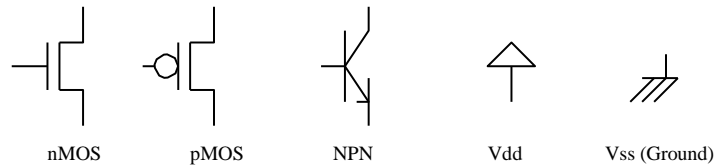
- IT is design rule clean
- Show dimensions and net names for PMOS AND nmos
- Simulation waveforms based on layout
- Compare layout results and spice simulation results

Part 3 :

Create symbol view of the inverter using the layout created and create a buffer
Turn in layout view of the buffer and simulation result of input and output

The CMOS Inverter

The CMOS inverter includes 2 transistors. One is a n-channel transistor, the other a p-channel transistor. The device symbols are reported below. In order to build the inverter, the nMOS and pMOS gates are interconnected as well as the outputs as shown in Figure 1.



Device symbols

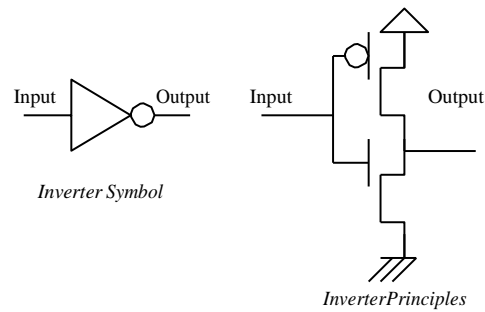


Fig. 1. The schematic diagram of the CMOS inverter with one nMOS at the bottom and one pMOS at the top.

Manual Design



In MicroWind, the default icon is the drawing icon shown above. It allows box editing. The palette is located in the lower right corner of the screen. A red color indicates the current layer. Initially the selected layer in the palette is polysilicon. The two first steps are illustrated in Figure 2.

n Fix the first corner of the box with the mouse.

o While keeping the mouse button pressed, move the mouse to the opposite corner of the box.

p Release the button. This creates a box in polysilicon layer as shown in Figure 2. The box width should not be lower than 2λ , which is the minimum width of the polysilicon box.



Fig. 2. Creating a polysilicon box.

Now, draw two more boxes as in Figure 3. Try to keep close to the shape and size shown in Figure.

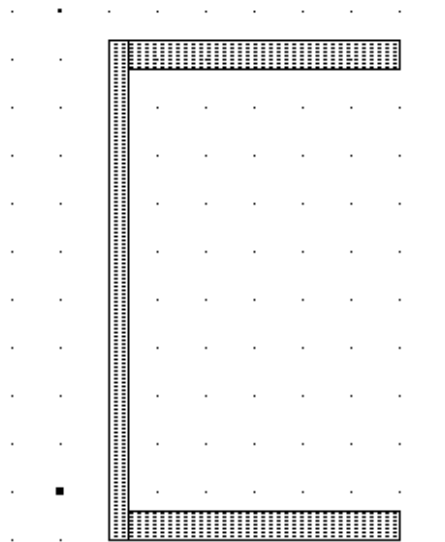


Fig. 3. Creating three polysilicon boxes.

Change the current layer into N+ diffusion by a click in the palette on the **Diffusion N+** button. Be sure that the red layer is now the N+ Diffusion. Draw a n-diffusion box at the bottom of the drawing as in Figure 4. N-diffusion boxes are represented in green. The intersection between the N+ diffusion and the polysilicon creates the channel of the MOS device.

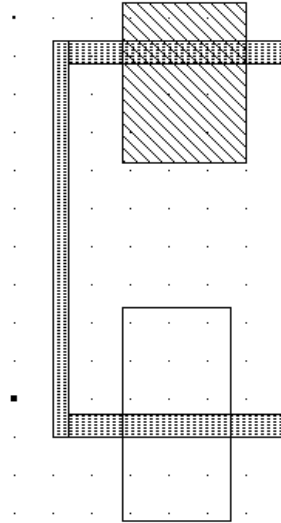


Fig. 4. Creating the N-channel and P-Channel devices.

Change the current layer into P+ diffusion by a click in the palette on the button **P+ Diffusion**. Draw a p-diffusion box at the top of the drawing as in Figure 4. P-diffusion boxes are represented in yellow. The intersection between the P+ diffusion and the polysilicon creates the channel of the pMOS device. Change the current layer into N Well by a click on the corresponding button in the palette. Draw a well all around the p+ diffusion, as in Figure 5. Use keyboard arrows (up key) to view the upper part of the layout.

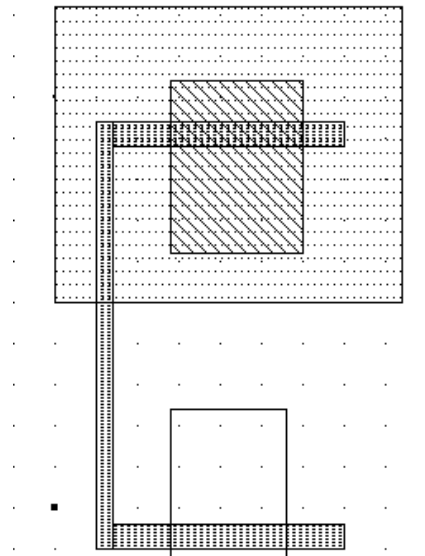


Fig. 5. Creating the well for the P-Channel Device.

Process Simulation



Click on this icon to access « **process simulation** ». The cross-section is given by a click on the mouse at the first point and the release of the mouse at the second point. In the example below (Figure 6), the cross-section of the n-channel MOS device appears on the left, and the cross-section of the p-channel MOS device on the right.

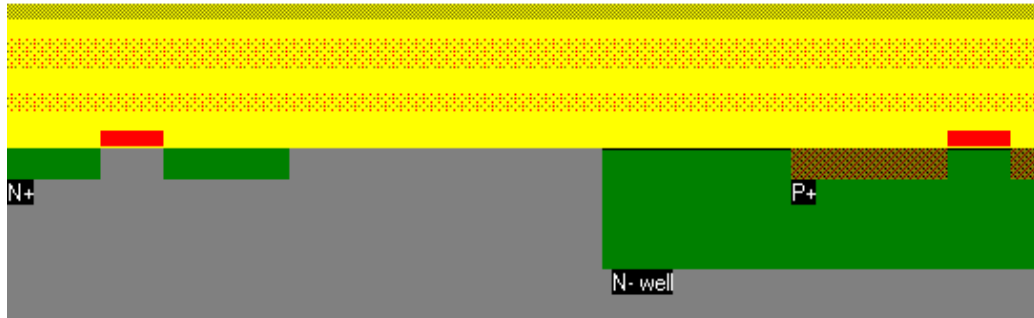


Fig. 6. The cross-section of the nMOS and pMOS devices.

Contacts and Metal Interconnects

The diffusion areas must be joined using a metal layer. The metal layer is isolated from the diffusions by a thick silicon dioxide SiO₂ layer. The contact layer is used to drill a hole in the oxide in order to join the metal and the diffusions. You could draw the contact box manually by selecting the layer « Contact » and drawing a 2 x 2 λ box. A fast solution is to use the predefined macros at the top of the palette. Various contacts built according to design rules are proposed.

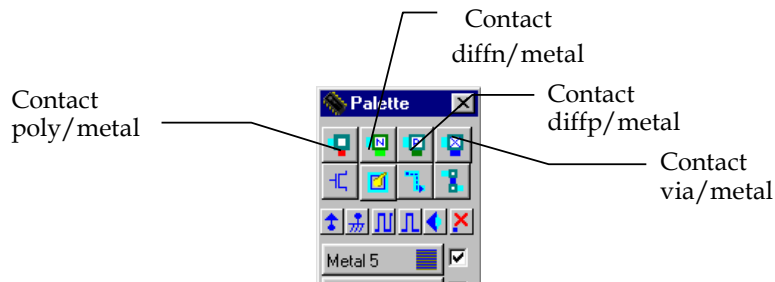


Fig. 7. The contact macros.

Choose the diffn/metal contact icon in the palette. The contact outline will appear. Fix the contact inside the n+ diffusion area. Click again on the diffn/metal contact and place it at the upper corner of the n-well box. This contact is used to polarize the well at VDD. The diffusion N+ in the nwell makes an ohmic contact and prepares for the VDD polarization using metal layers. Finally, click on the diffp/metal icon and fix the contact inside the p+ diffusion area.

Select the « metal » layer in the palette. Draw a metal bridge between the n+ and p+ contacts. The CMOS inverter layout is almost completed (Figure 8). The remaining task is to define where the supply, the ground, the input and the output are.

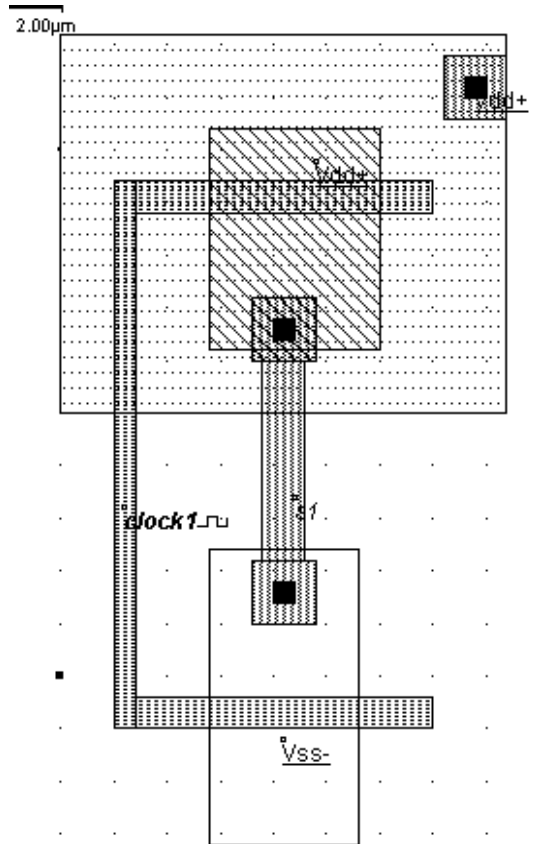
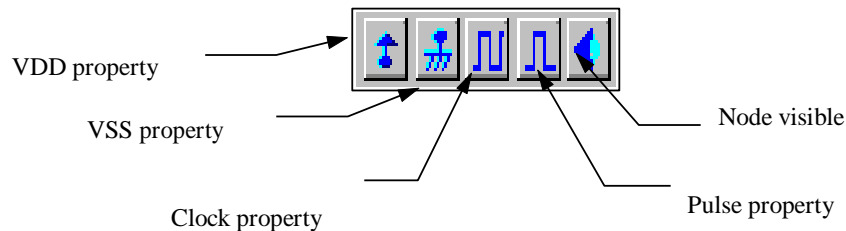


Fig. 8. The metal bridge and the inverter are completed.

Add Properties for Simulation

Properties must be added to the layout to fix the ground, the supply, the input and the outputs. The summary of available properties is reported below.



For the inverter example, we must assign the upper p-diffusion to a VDD power supply, and the lower n-diffusion box to a VSS ground voltage. We also need to specify a clock as the input for the IN node and have a look at the output OUT.

- Stuck at Vdd: Click on the Vdd icon and click on the upper p-diffusion box.
The Vdd property is sent to the node.

- Also click in the N-Well region inside which the pMOS is located. The NWell must always be at VDD voltage to keep the pMOS junctions inverted.
- Ⓟ Hold at Vss: Click on the Vss icon, click on the lower n-diffusion box. The Vss property is sent to the node.
- Ⓠ Apply a clock to node IN: Click on the Clock icon and on the polysilicon gate. The Clock menu appears (See below). Click on OK. A default clock with 3 ns period is generated. The Clock property is sent to the node and appears at the right hand side of the desired location with the name « clock1 ».

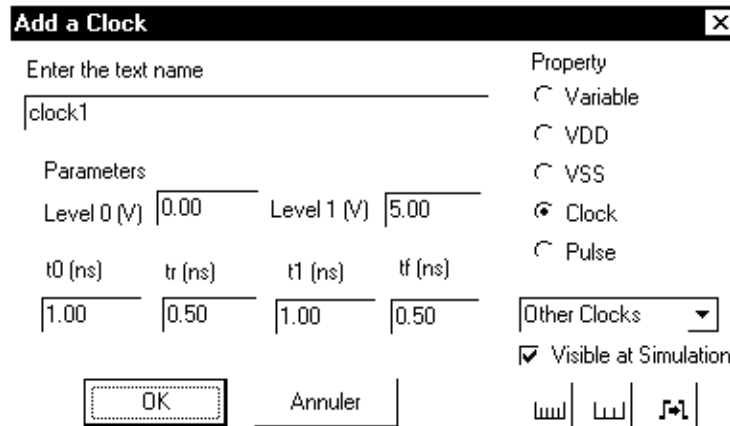
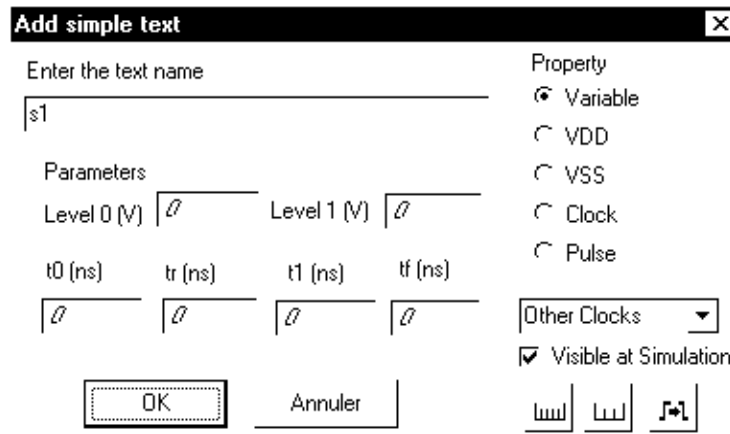


Fig. 9. The clock menu.

- Ⓡ Watch the output: Click on the Visible icon and then, on the metal bridge. The window below appears. Click OK. The Visible property is sent to the node. The associated text « s1 » is in italic. The chronogram of this node will appear in the next simulation.



Analog Simulation

IMPORTANT : Always save BEFORE simulation ! Click on **File** in the main menu. Move the cursor to **Save as ...** and click on it. A new window appears, into which you are to enter the design

name. Type, for example, MYINV. Use the keyboard for this and press \leftarrow . Then click on OK. After a confirmation question, the design is saved under that filename.

Click on **Simulate** in the main menu. The timing diagrams of the inverter appear, as shown in Figure 10. Click on **More** in order to perform more simulations. Click on **Stop** to return to the editor. The gate delay is computed at $V_{DD}/2$, that is 2.5 V, between the signal selected in the Start Node list and the signal selected with the Stop Node list.

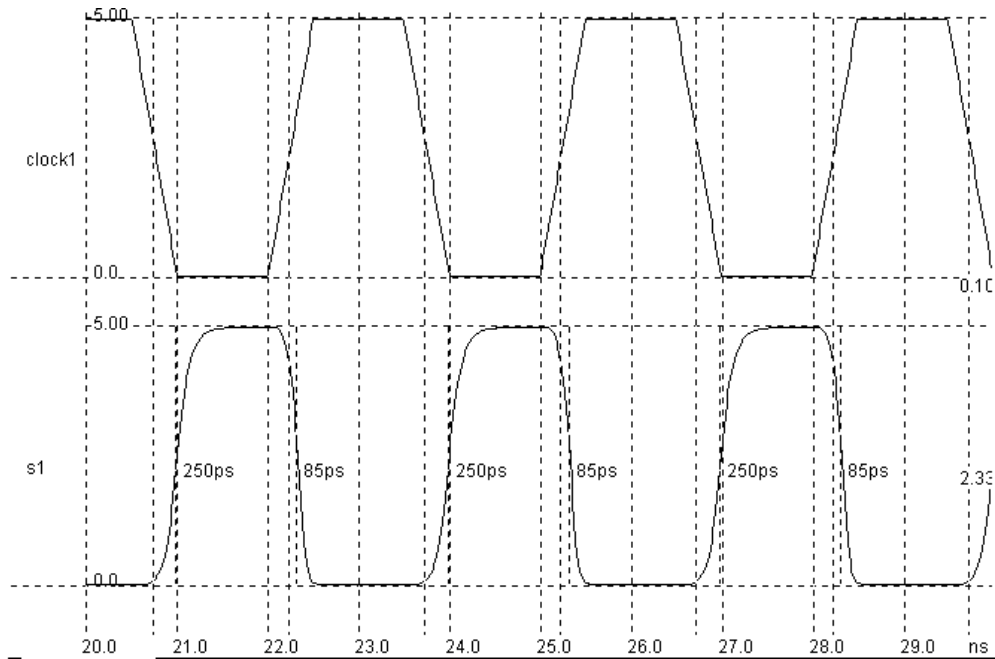
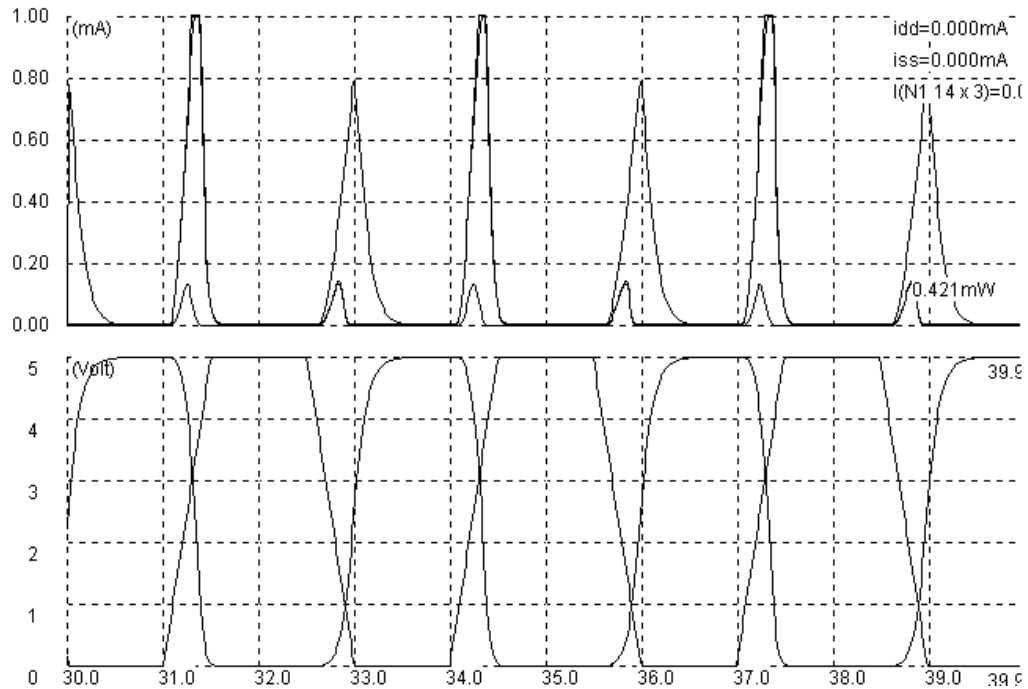


Fig. 10. Analog simulation of the CMOS inverter. The output has the opposite value of the clock input.



- ◆ Click on **Voltage & Currents** to see both currents and voltages (Figure 10). The current peaks can be seen in the upper window. All voltages are reported in the lower window. The current scale can be adjusted using a predefined list of values. Some current is consumed at VDD supply, mainly when the output of the inverter rises to VDD. Some current is consumed at VSS, mainly when the output goes down to zero.
- ◆ Click on **Voltage vs. Voltage** to see the DC transfer characteristics of the inverter (Figure 11-bottom). The commutation point of the inverter V_c is the input voltage for which the output is close to $V_{DD}/2$. In the case of Figure 24, V_c is around 1.8 V. Click on **Back to Editor** to return to the editor.

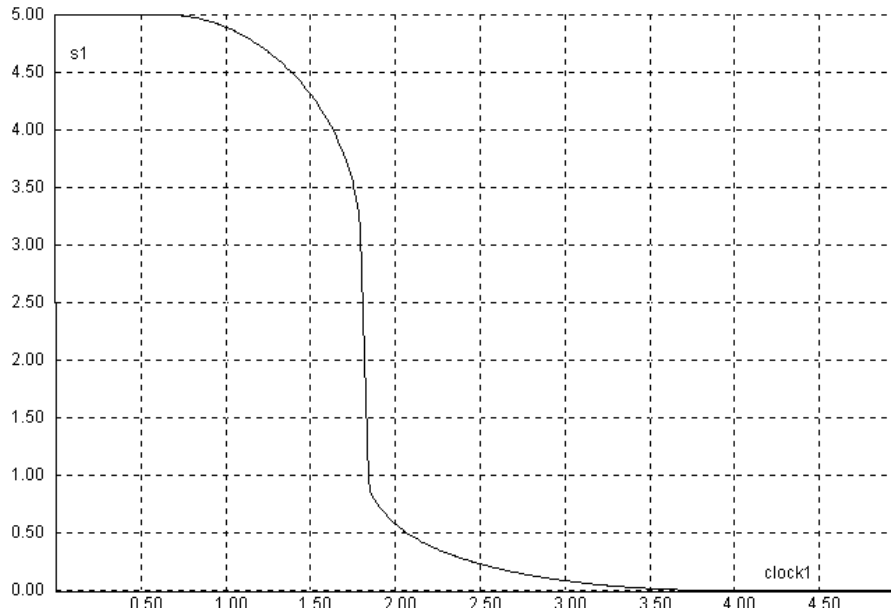


Fig. 11. Current consumption of the CMOS inverter (top) and DC characteristics of the CMOS inverter(bottom).

Is your layout correct ?



Click on the above icon to answer the question. The *Design Rule Checker (DRC)* scans the design and verifies a set of design rules. The errors are highlighted in the display window, with an appropriate message giving the nature of the error. Details about the position and type of error(s) appear on the screen. Only an error-free layout can be sent to fabrication.

Parametric Analysis of the Inverter

Click on **Analysis -> Parametric Analysis**. Click on the output node of the inverter in the layout. The window below appears. The parametric analyzer allows you to investigate easily the influence of various parameters on the inverter delay.

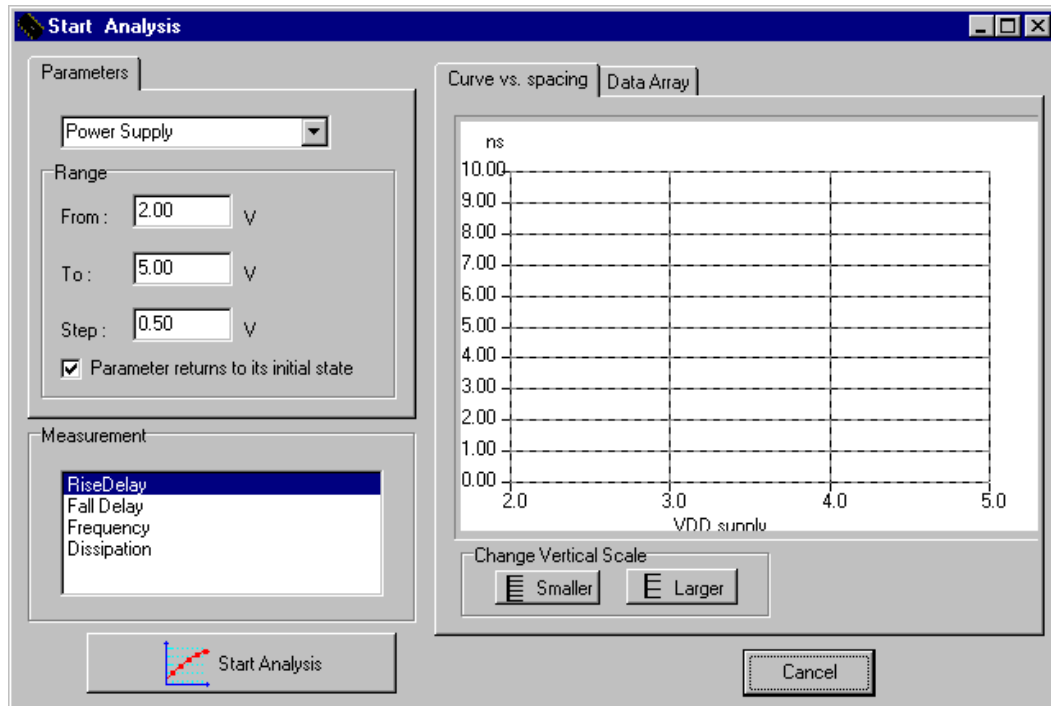


Fig. 12. The parametric analyzer

- n** Select the « Delay » in the « Measurement » menu.
- o** Select « power-supply » in the « Parameter » choice.
- p** Click on « Start Analysis ». An iterative procedure conducts simulations and extracts the delay from the simulation for each value of VDD power supply as defined in the « Range » menu. The result in Fig. 12 shows that the gate delay decreases rapidly with the power supply.

Other possible investigations concern the frequency and dissipation. The temperature, the node capacitance and the voltage supply are parameters worth of interest are. Fig 13 gives an account of the increase of the power consumption with the VDD supply. Fig 13 also points out (bottom) the delay increase with the output capacitance load.

In order to obtain this curve, you should select the « Node Capacitance » in the parameter list first, and then modify the items « From », « To » and « Step » according to Fig. 13. Once those modifications have been made, you can start the analysis. As expected, the gate delay increases rapidly along with the output capacitance.

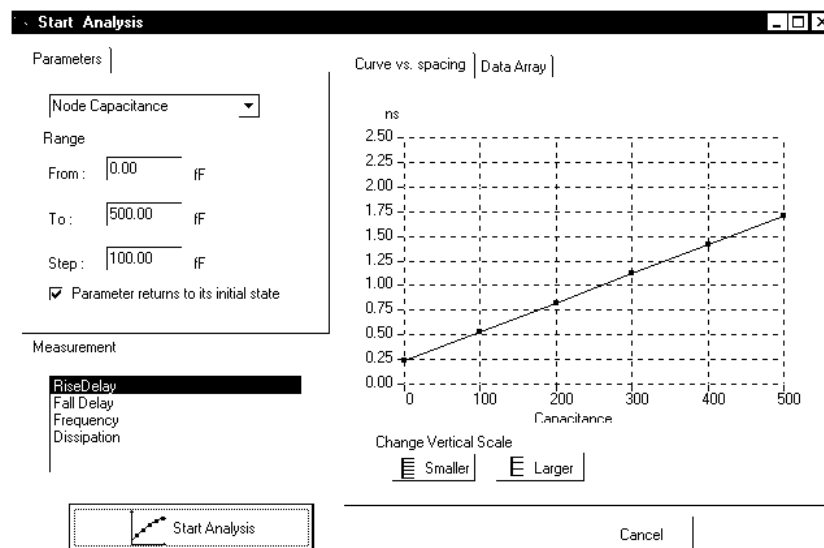
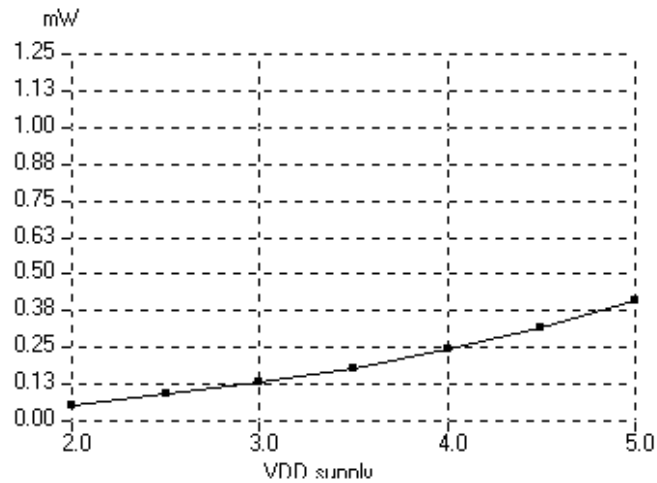


Fig. 13. Investigation of the VDD supply effect on the power consumption (top), and the effect of the output capacitance load on the delay (bottom).

Extract SPICE netlist

The SPICE netlist for the inverter layout can be extracted using the relevant menu command. The extracted netlist can then be simulated using SPICE for performance.

Save & Quit



Click on F2 or **File -> Save**. The design is saved under the current name. The MSK appendix is automatically added to the user's filename. To leave MICROWIND, click on **File->Leave Microwind** in the main menu.