Electrical and Computer Systems Engineering Department
ENCS333
Homework 4

Due November 5th

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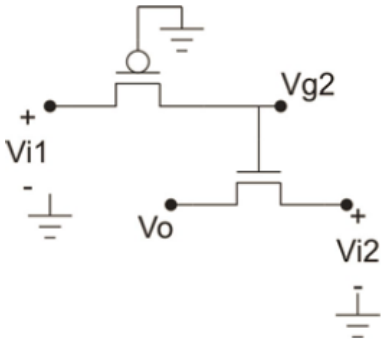
1. Using the rules given in lecture notes, find **Vg2** and **Vo** required for both transistors to be ON in the two-transistor circuit shown below for each of the listed input voltage combinations. Assume **VDD = 2.5V**, **Vtn = 0.5V**, and **|Vtp| = 0.5V**.

(a) Vi1 = 0V, Vi2 = 0V
(b) Vi1 = 2V, Vi2 = 2V
(c) Vi1 = 2.5V, Vi2 = 2.5V
(d) Vi1 = 0V, Vi2 = 1V



2. Design a transistor-level CMOS logic circuit to implement the function $F = \overline{(x + yz) \cdot (w + x)}$ using the least number of transistors.

HINT: Consider that you may need to expand the equation in order to reduce it using the logic properties shown in the Chapter 2 lecture notes.

3. Construct the CMOS logic circuit that implements $Y = a + \overline{\bar{a} + b} + c\bar{b}$ using the fewest possible transistors. You are allowed to use inverted inputs (e.g., *a'*) rather than adding inverters to create these signals.

4. Mux design

a) Construct a schematic for a 2:1 MUX using two CMOS transmission gates and an inverter.

b) Using the 2:1 MUX symbol below, construct a gate-level schematic for a 4:1 multiplexer using only 2:1 multiplexers. The inputs should be s0, s1, and P3:0 (P0 – P3) and the output is F.
c) How many transistors are needed to form the transmission gate based 4:1 MUX in (b)?
d) Are there any redundant transistors that could be eliminated if you constructed the 4:1 MUX at the transistor level? If so, how many and which ones?

5. A CMOS metal layer with resistivity, ρ, 3x10-6 Ω-cm is 0.6μm thick. It is used to draw a signal trace that is 100μm long and 0.75μm wide.

a) Calculate the sheet resistance, Rs, of this metal layer.
b) How many "squares", n, are in the signal trace?
c) Use the results in (a) and (b) to determine the resistance of the trace.

6. Draw the schematic for the CMOS circuit that implements the function ***F*** described by the truth table below. Use the least possible number of transistors. Explain your procedure and show the reduced function equation used to design the schematic.

Inputs			***Output***
X	**Y**	**Z**	**F**
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

7. Sketch a color-coded stick diagram for the circuit that implements the function $f=a+\overline{(b.c)+d}$ Organize the layout so that the transistors can be implemented on a continuous strip of active (i.e., do not break the active).