BIRZEIT UNIVERSITY

Electrical and Computer Systems Engineering Department
ENCS333
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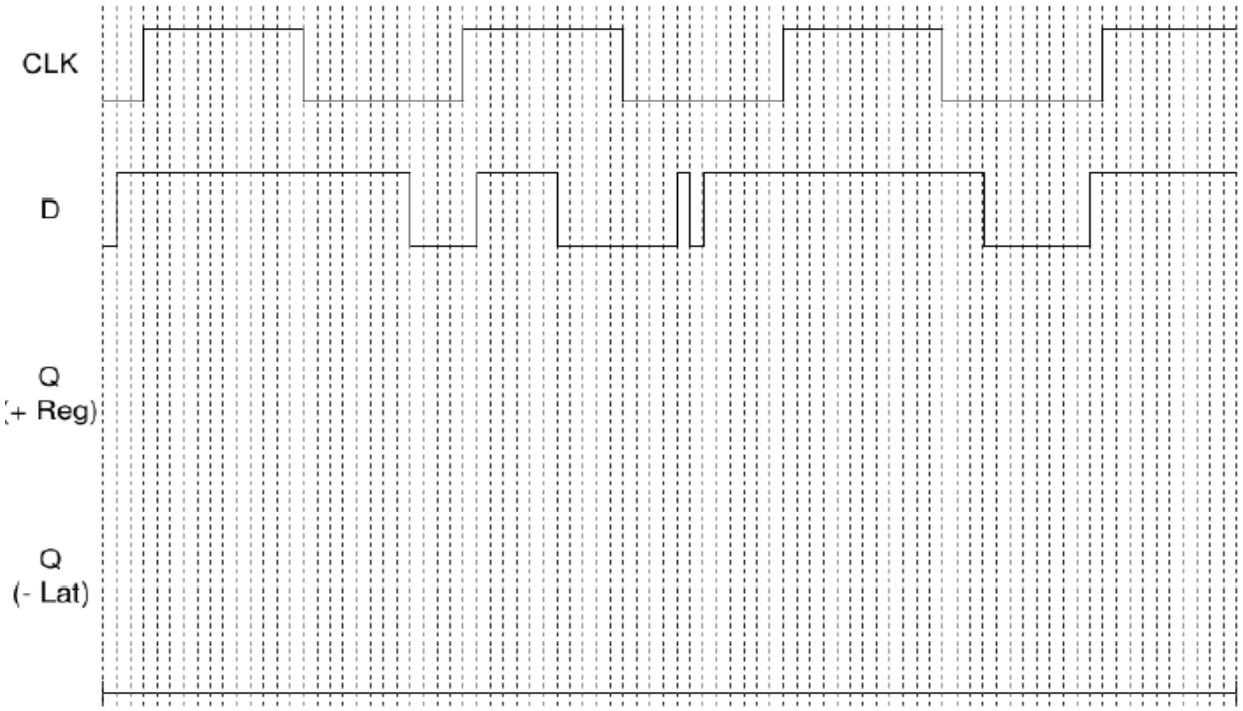
Homework 6

Due December 20th

Problem 1

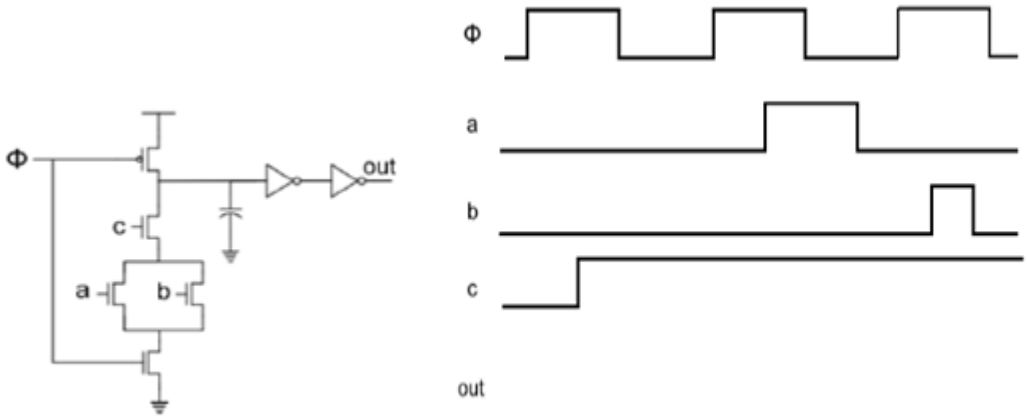
Given the following clock and data waveforms, draw the output waveforms for a
(a) positive edge-triggered register and

(b) a negative (or transparent-low) latch.
The timing characteristics of these sequential elements follow: $tc \rightarrow Q$ = 4 units, $tD \rightarrow Q$ = 3 units, *tsetup* = *thold* = 2 units. Vertical dashed lines have a separation of one unit. The clock period is equal to 24 units. Clearly mark on the figure where setup and hold time violations occur for each sequential element.



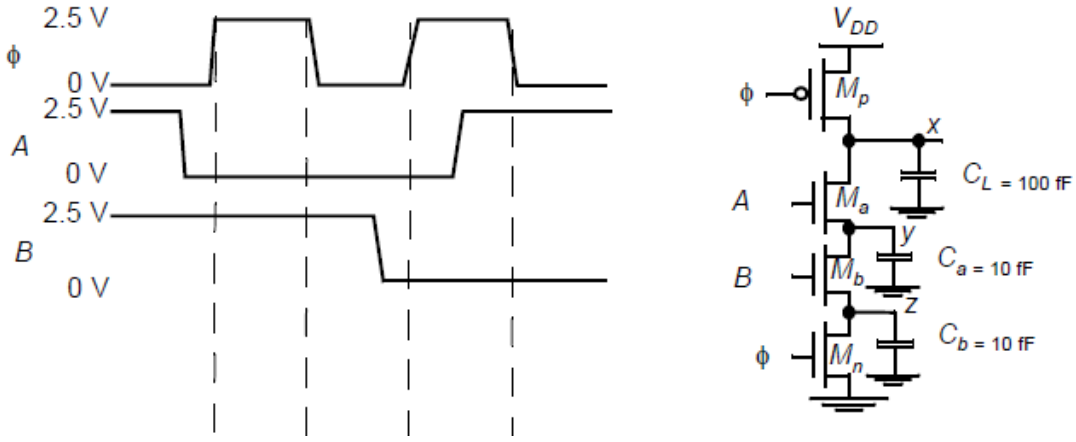
Problem 2 :

Consider the dynamic gate shown in the following figure. Based on the input signal, draw the output signal.



Problem 3

Sketch the waveforms **at *x*, *y*, and *z* for the given inputs**. You may approximate the time scale, but be sure to compute the voltage levels. Assume that V_T= 0.5 V



Problem 4

The simplified layout of a pMOS transistor in a 0.5µm process is shown here with the "actual" fabricated dimensions. Determine the device parasitics below using the following process model values:

k'p =90µA/V^2, |Vtp| = 0.5V, Cox = 1.8fF/µm^2, Cj = 0.75fF/µm^2
and Cjsw = 0.25 fF/µm

a) What is the gate capacitance, C_G?

b) What is the gate-to-drain capacitance, C_{GD}?

c) What is the drain-to-bulk capacitance, C_{DB}?

d) What is the total capacitance at the drain node?

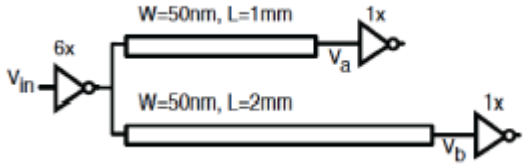
e) If the drain node RC time constant is 4psec, what is channel resistance?

Problem 5:

Elmore Delay

For the following problem, $C_G = C_D$ = 2fF=um, the minimum sized (labeled as 1x in the picture) inverter has L = 0:1um, W_p = 2um, W_n = 1um and for this technology $R_{n,\,on}$ = 10kOhm/sq: (i.e. the resistance of an NMOS with width W and length L is equal to 10k Ohm $_{L/W}$) and $R_{p,\,on}$ = 20k=sq: (i.e. the resistance of a PMOS with width W and length L is equal to 20k $_{L/W}$). Note that a 6x inverter has 6 times the width of a 1x inverter

For the wire, R_{wire} = 0:1=Ohm/sq:, the parallel plate capacitance is C_{pp} = 20aFfum$_2$ and the fringing capacitance per each side of wire is C_{fr} = 14aF/um. The wire widths and lengths are shown in the picture..



a) Using the _ wire model, draw the equivalent RC switch model. What is the propagation delay from a step at Vin to Va and Vb?

b) What is the skew (difference in arrival time between Va and Vb)?

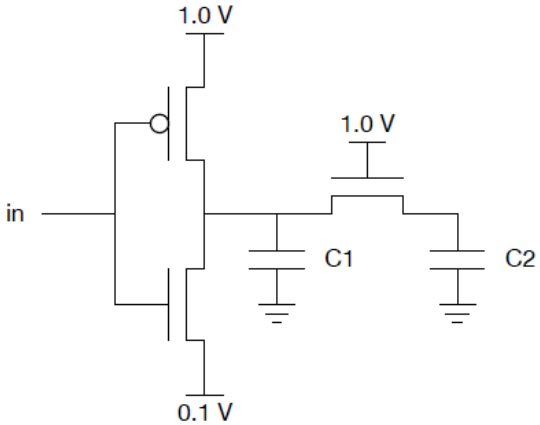
Problem 6

Energy

Given the circuit below, answer the following questions. Assume that the capacitances associated with the FETs are negligible.

$C_1 = C_2$ = 90fF

$V_{th,n} = jV_{th,p}j$ = 0:4V



Part a

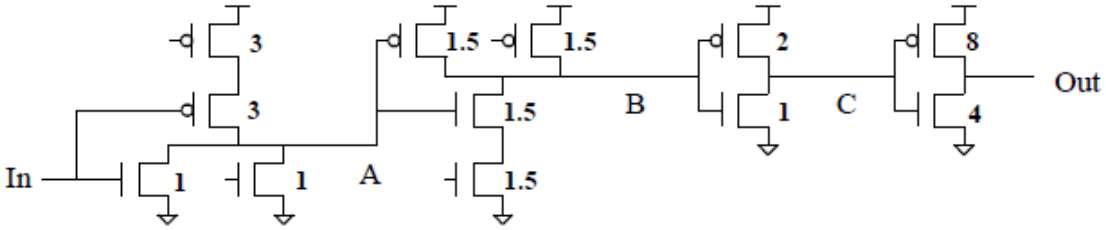
How much energy is stored in each capacitor after a 1V to 0V transition on `in`? Please show your work.

Part b

How much energy was drawn by the supply in part a? Is this what you expected? Please show your work.

Proplem 7

1. Given the cstatic logic as shown in figure below, Converted to dynamic logic and size the device accordingly



Proplem 8:

What is difference between clk skew and jitter

Proplem 9:

Clock distribution is one of the most critical areas in the design of high performance VLSI chips. Poor clock distribution can result in excessive clock skews between clusters on the chip, reducing the maximum operating frequency. In general we need to reduce the effect of clock skew on the chip. What are the list of things that is required to do that ?

Proplem 10

Write the equation for dynamic power consumption and the equation for static power consumption. Explain the circuit characteristics (e.g., Vt, temperature, or gate size) that each depends on. Point
out recent trends for these characteristics.

Proplem 11

The simplified layout of a pMOS transistor in a 0.5µm process is shown here with the "actual" fabricated dimensions. Determine the device parasitics below using the following process model values:
$k'p = 90\mu A/V^2$, $|Vtp| = 0.5V$, $Cox = 1.8fF/\mu m^2$, $Cj = 0.75fF/\mu m^2$
and $Cjsw = 0.25\ fF/\mu m$

a) What is the gate capacitance, C_G?

b) What is the gate-to-drain capacitance, C_{GD}?

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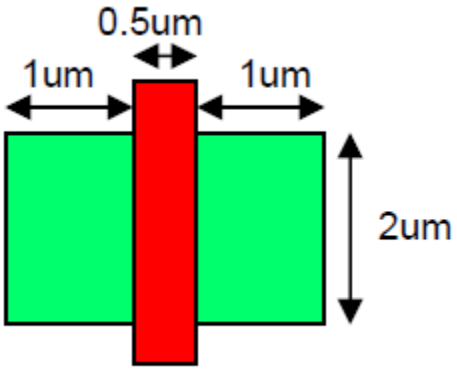


Problem 12

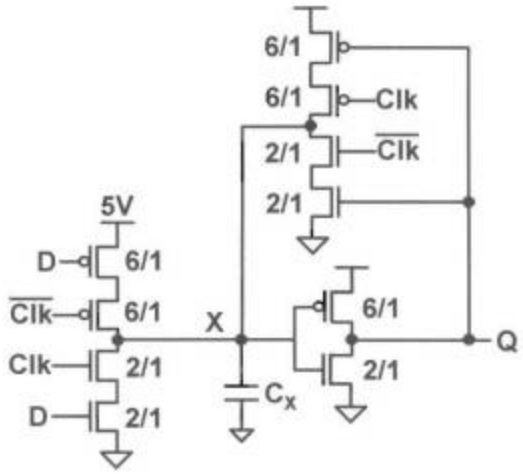
Suppose the inverter you designed in Problem drives a total capacitance of 45fF at 4.1GHz. How much power does it consume assuming VDD = 5V?

Problem 13

Implement the logic function F = AB + CD using a 4-input dynamic CMOS logic gate with a minimum number of transistors and a single minimum-sized inverter ration (1/3). Size the 4-input gate such that the worst case rise and fall times at its output are equal to the minimum-sized inverter.

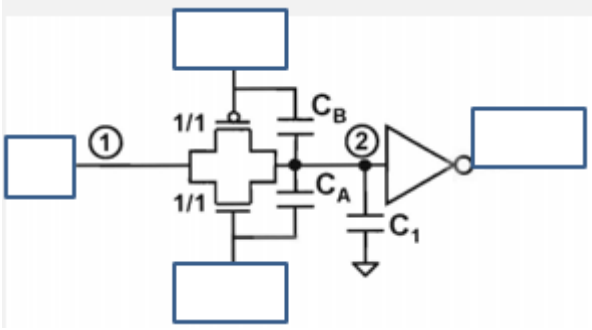
Problem 14

What kind of circuit is the circuit below ? is it dynamic or static circuit ? is it aa latch or ff ?



Proplem 15

A. For the latch circuit shown in Figure below, label the boxes D, C LK, CLK, Q such that the circuit works as a positive transparent inverting latch.



B. Is the circuit in a static or dynamic latch (circle one)? Justify your answer.

C. Suppose the latch is used as the slave stage of an edge-triggered flip-flop and that node 1 and node 2 in Figure above are initially at 1.8V and OV, respectively. Assuming Rp = 300ohm for a PMOS device with W/ L = 1/1 and Rn = lOOohm for an NMOS device with W/L = 1/1 , CA = 19fF, CB = 23fF, C1 = 150fF, and tpHL for the inverter is 8.9ps, estimate the clock-to-Q delay for the latch using the switch RC model for the transistors.