جامعة بيرزيت
BIRZEIT UNIVERSITY

ENCS 333

(HOMEWORK #1)

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Section: 1

Question No.1:

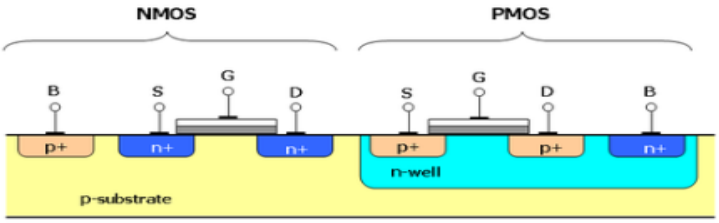
Define CMOS? What are the two types of transistor? How do they work, show operation region of each device? Draw the ID vs. VDs curve?

Answer:

CMOS stands for "Complementary Metal-Oxide Semiconductor", is the technology that used for constructing the integrated circuits. CMOS technology is used in many digital logic and analog circuits.

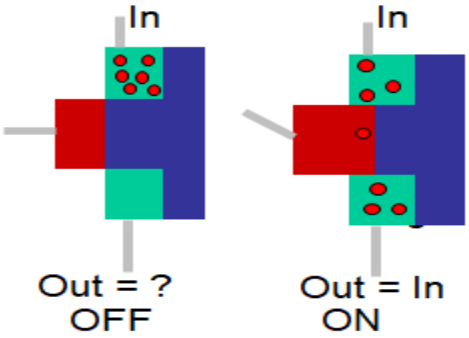
CMOS contains two types of semiconductors: p-type and N-type.

CMOS semiconductor use both NMOS and PMOS circuits, so it contains two different types of semiconductors. These two semiconductors work together and may form logic gates based on how the circuit is designed.



CMOS semiconductor [1]

CMOS transistor is a switch:



[2]

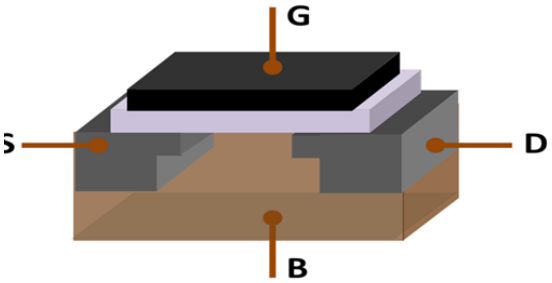
Very useful used for CMOS in computers to store data, time, and BIOS (Basic Input Output System) settings.

It is also used to perform logical functions.

CMOS ICs are fabricated on circular slices of silicon called wafers.

MOSFET transistor stands for "Metal Oxide Semiconductor Field Effect Transistor", which is used for switching and amplifying electronic signals in the electronic devices.

MOSFET is a four terminal device (Source, Gate, Drain, and Body), where the body of the MOSFET is frequently connected to the source terminal so making it a three terminal device like field effect transistor.



MOSFET [3]

The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain. It is insulated from the channel near an extremely thin layer of metal oxide.

The working of MOSFET depends upon the MOS capacitor.

Semiconductor surface at the below oxide layer which is located between source and drain terminal. It can be inverted from p-type to n-type by applying a positive or negative gate voltage respectively.

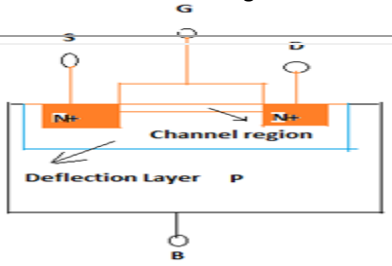
How the two types of MOS work:

If $V_{ds}=0$ → Accumulation $V_{gs} << V_t$, Depletion $V_{gs}-V_t$, Inversion $V_{gs} > V_t$

If $V_{ds}>0$ → Unsaturated $V_{gs}-V_t > V_{ds}$, Saturation $V_{gs} - V_t < V_{ds}$,cut-off : current =0

There are two types of MOSFET:

1) **<u>NMOS:</u>**



This type of MOSFET the drain and source are heavily doped n+ region and the substrate or body is P- type.

The current flows due to the negatively charged electrons.

When we apply the positive gate voltage:

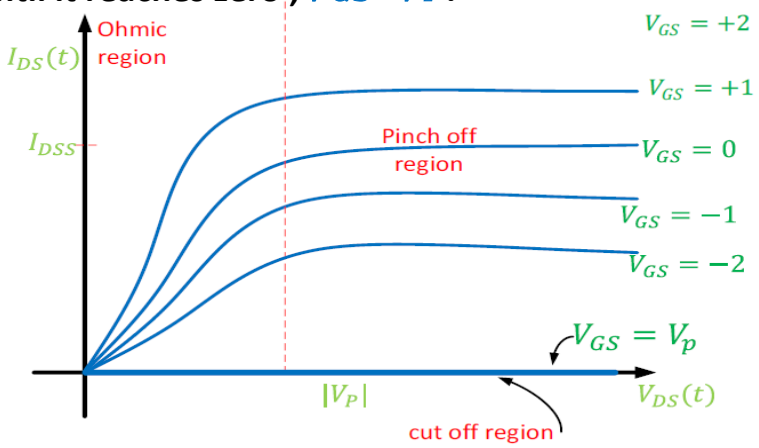
The holes present under the oxide layer pushed downward into the substrate with a repulsive force. The depletion region is populated by the bound negative charges which are associated with the acceptor atoms. The electrons reach channel is formed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Instead of positive voltage if we apply negative voltage a hole channel will be formed under the oxide layer.

On the application of VDS and keeping VGS=0 electrons from the n-channel are attracted towards positive potential of the drain terminal.

This establishes current through the channel to be denotes as $IDSS$ at VGS=0.

If we apply negative gate voltage (VGS<0) the negative charge on the gate repel electrons from the channel. The number of repelled electrons depends on the magnitude of the negative voltage VGS.

The grater the negative voltage applied at the gate , the level of drain current will reduces until it reaches zero ; VGS= VP.



Drain characteristics for an n-channel DMOSFET

As shown in the above curve, there are three regions:

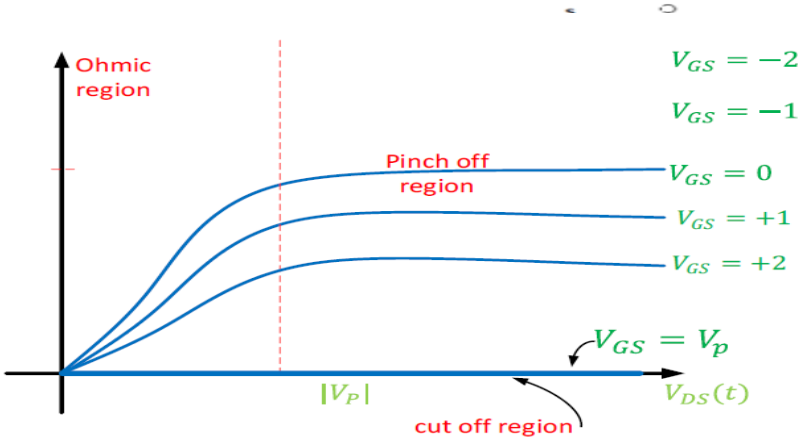
1) **Ohmic region.** 2) **Pinch off region.** 3) **Cut-off region.**

2) **<u>PMOS:</u>**

The drain and source are heavily doped p+ region and the body or substrate is n-type.

When we apply the negative gate voltage:

The electrons present under the oxide layer with are pushed downward into the substrate with a repulsive force. The depletion region populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage also attracts holes from p+ source and drain region into the channel region. Instead of negative voltage if we apply positive voltage an electrons channel will be formed under the oxide layer.



◆ **For the n- channel**

$V_{GS} > V_P$ (negative)
$V_{DS} > V_{GS} - V_P$

◆ **For the p- channel**

$V_{GS} < V_P$ (positive)
$V_{DS} < V_{GS} - V_P$

Drain characteristics for an p-channel DMOSFET

As shown in the above curve, there are three regions:

1) **Ohmic region.** 2) **Pinch off region.** 3) **Cut-off region.**

Question No.2:

In parallel with the increase of IC operating frequencies, how do the roles of parasitic C and L change?

Answer:

The value of impedance X_L normally increased with increase of frequency according to the following X_L=jwL, but since at higher frequencies there is parasitic capacitance in series or in parallel with L, the impedance starts to decrease. While in C, the roles are inverted, so the value of impedance X_c normally decreased with increase of frequency according to the following X_c=1/jwc, but since at higher frequencies there is parasitic inductance in series or in parallel with C, the impedance starts to increase.

Also, when the frequency increase, the size of the transistors will decrease, and this leads that the effect of parasitic C and L on the transistors will increase, so this change threshold voltage, and of course this effect to the others different values.

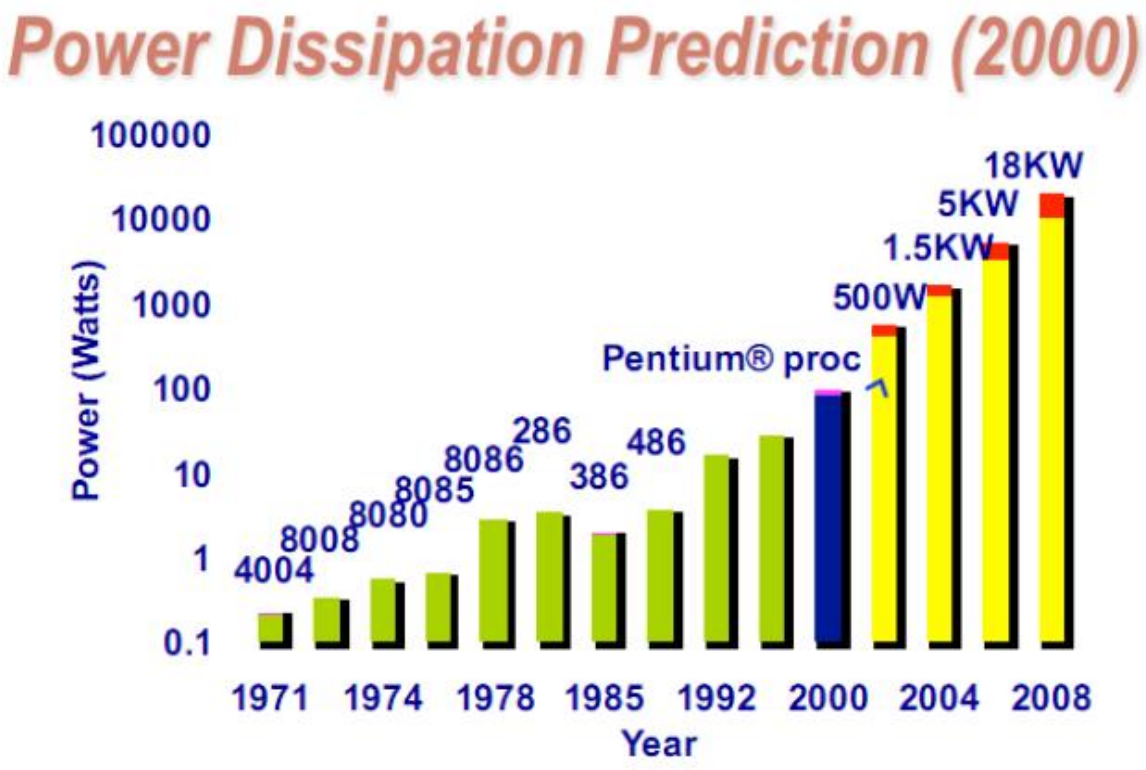
Question No.3:

What are the trends of power consumption related to IC evolution?

Answer:

In Fact, when the evaluation of the integrated circuit increased, the power consumption also will increase.

The graph below shows the power consumption due to the evolution of integrated circuits:



Question No.4:

What are the basic steps for CMOS IC fabrication?

Answer:

The CMOS can be fabricated using different processes such as:

N-well process for CMOS fabrication.

P-well process.

Twin tub-CMOS- fabrication process.

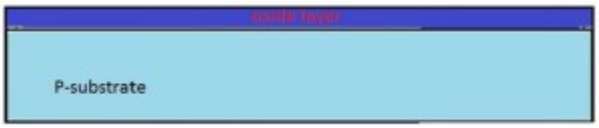
So, if we use P-substrate, the fabrication can be done with these steps:

Step 1: Substrate

Primary start process with a P-substrate

Step 2: Oxidation

The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.

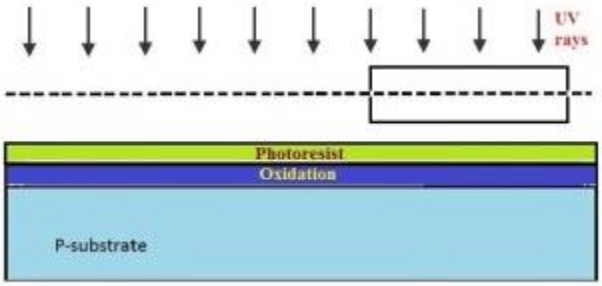


Step3: Photoresist

A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.

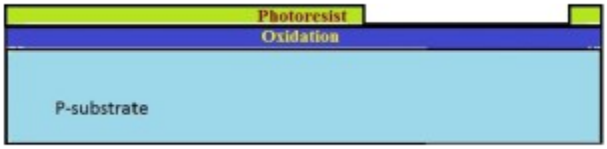
Step4: Masking

The photoresist is exposed to UV rays through the N-well mask



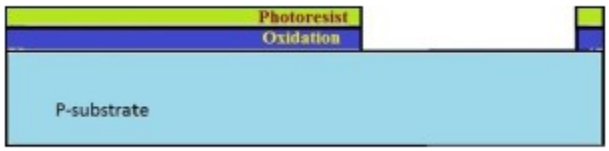
Step5: Photoresist removal

A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution.



Step6: Removal of SiO2 using acid etching

The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.

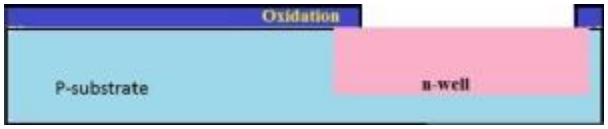


Step7: Removal of photoresist

The entire photoresist layer is stripped off, as shown in the below figure.

Step8: Formation of the N-well

By using ion implantation or diffusion process N-well is formed.

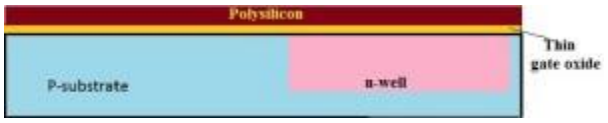


Step9: Removal of SiO2

Using the hydrofluoric acid, the remaining SiO2 is removed.

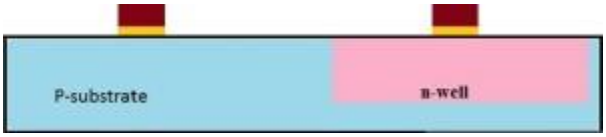
Step10: Deposition of polysilicon

Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.



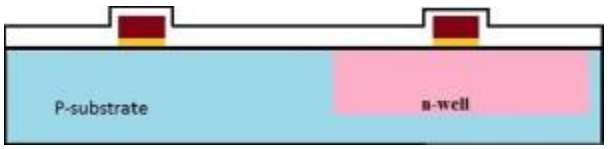
Step11: Removing the layer barring a small area for the Gates

Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.



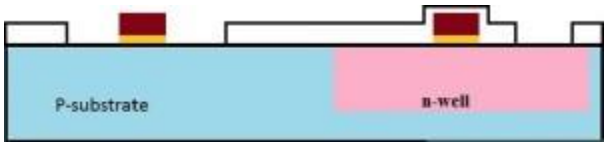
Step12: Oxidation process

Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.



Step13: Masking and N-diffusion

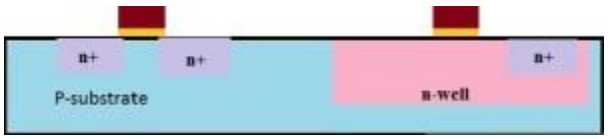
By using the masking process small gaps are made for the purpose of N-diffusion



The n-type (n+) dopants are diffused or ion implanted, and the three n+ are formed for the formation of the terminals of NMOS.

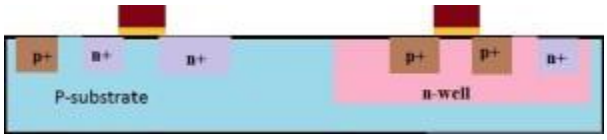
Step14: Oxide stripping

The remaining oxidation layer is stripped off.



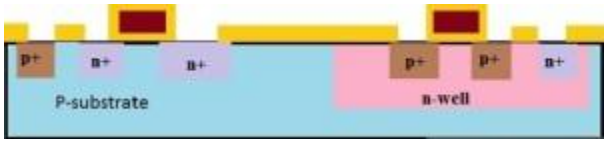
Step15: P-diffusion

Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.



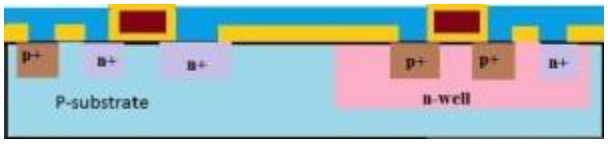
Step16: Thick field oxide

A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.



Step17: Metallization

Aluminum is sputtered on the whole wafer.

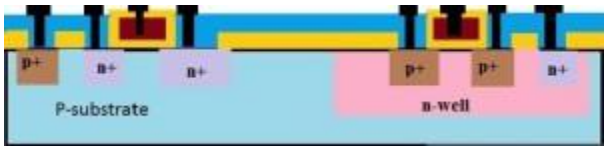


Step18: Removal of excess metal

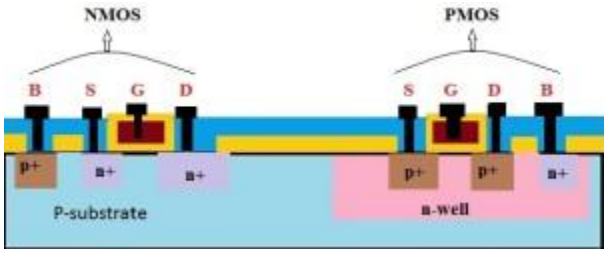
The excess metal is removed from the wafer layer.

Step19: Terminals

The terminals of the PMOS and NMOS are made from respective gaps



Step20: Assigning the names of the terminals of the NMOS and PMOS



Fabrication of CMOS using P-well process:

Among all the fabrication processes of the CMOS, N-well process is mostly used for the fabrication of the CMOS. P-well process is almost similar to the N-well. But the only difference in p-well process is that it consists of a main N-substrate and, thus, P-wells itself acts as substrate for the N-devices.

Different steps of the fabrication of the CMOS using the twintub process are as follows:

- **Lightly doped n+ or p+ substrate is taken and, to protect the latch up, epitaxial layer is used.**
- **The high-purity controlled thickness of the layers of silicon are grown with exact dopant concentrations.**
- **The dopant and its concentration in Silicon are used to determine electrical properties.**
- **Formation of the tub**
- **Thin oxide construction**
- **Implantation of the source and drain**
- **Cuts for making contacts**
- **Metallization**

Question No.5:

What are the main IC Characteristics?

Answer:

The main characteristics of integrated circuits are:

- **Power**
- **Area**
- **Speed**
- **Timing**
- **Cost**
- **Reliability**
- **Scalability**
- **Integration**

Question No.6:

What are the main IC parasitic?

Answer:

The main IC parasitic:

- **Resistors.**
- **Capacitors.**
- **Inductors.**
- **Transistors (Bipolar).**
- **Diodes.**

Question No.7:

Explain what do we mean by process node? And how does that affect IC characteristics?

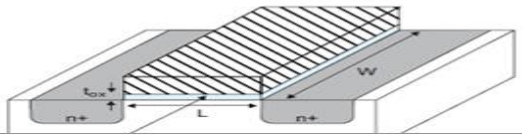
Answer:

Process node is standardized process used across wide range of products, it is determining the technology that used in this device (for example it is the length of gate in MOSFET transistor). The process for multiple products makes yield and process improvement much easier, since the same resources can solve complex problems involving multiple steps for many products simultaneously instead of having to have a separate team for each small product group.

Process technology

Intel Technology Roadmap

Process Name	P1266	P1268	P1270	P1272	P1274
Lithography	45 nm	32 nm	22 nm	14 nm	10 nm
1st Production	2007	2009	2011	2013	2015



So, the process node affect to IC characteristics, for examples, when L is increase we need more electrons or holes to connect the channel between drain and source, so according to process node, Vt will change so the other values will changed.

Also it effect to the cost of IC, it is depends to the technology that used in IC. Also speed, when the technology make the channel connected quickly it makes IC faster. In the same way it effects to the power and timing.

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