

ENCS 333

(HOMEWORK #3)

Student name: Fadi Armoush

Student number: 1160302

Instructor: Dr. Khader Mohammad

Section: 1



Aim of this assignment:

Is to be familiar with Microwind software which able us to design a layout of circuits (here we build inverter and buffer) with equal fall and rise time. Also we will do PSPICE to do our simulation.

First: inverter by using Microwind

Layout:

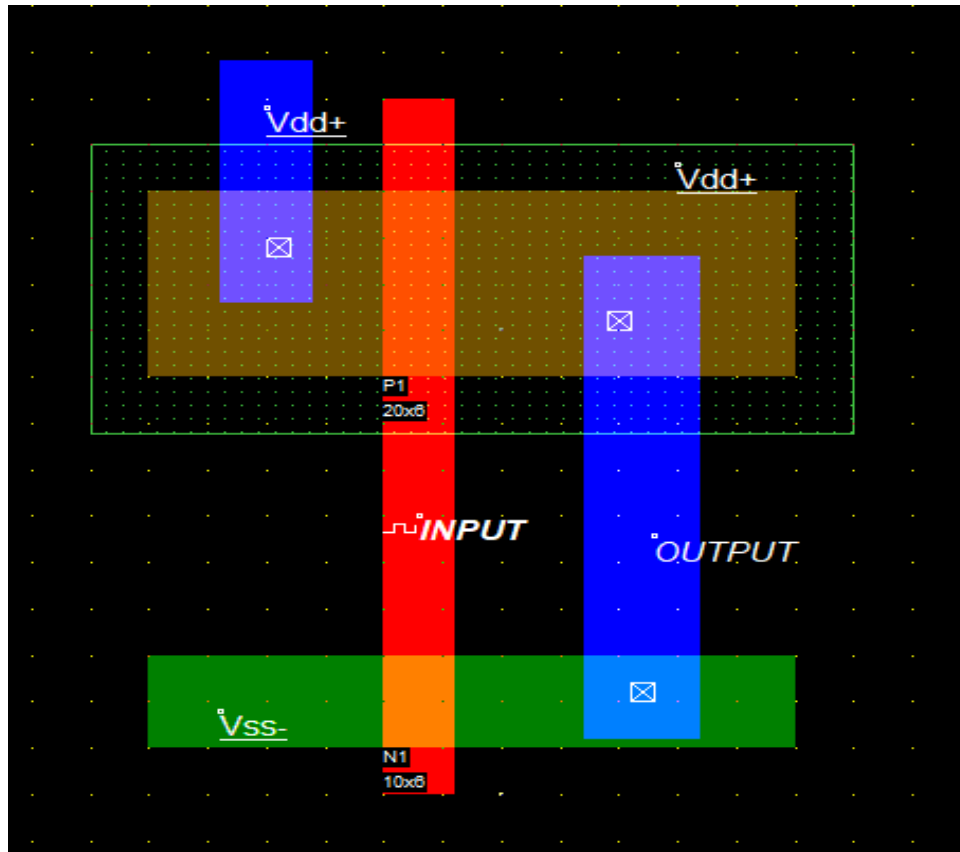


Fig.1

Dimensions:

| MOS | W(μm) | L(μm) | W(lamb) | L(lamb) | Type |
|-----|--------------------|--------------------|---------|---------|---------|
| N1 | 0.350 | 0.035 | 10 | 6 | low lea |
| N2 | 0.350 | 0.035 | 10 | 6 | low lea |

Fig.2

So for make the rise and fall time are equals:

$$T_{a0d} = T_{a0n} \rightarrow I_{dn} = I_{dp} \rightarrow M_p(w/L)_p = M_n(w/L)_n$$

So to make rise and fall time equals \rightarrow should the width of PMOS is twice the width of NMOS.

We do $W_p=0.7\mu m$, $W_n=0.35\mu m$, and $L=35nm$ (see fig.2) .

Then we obtained the following output with equal fall and rise time =9ps

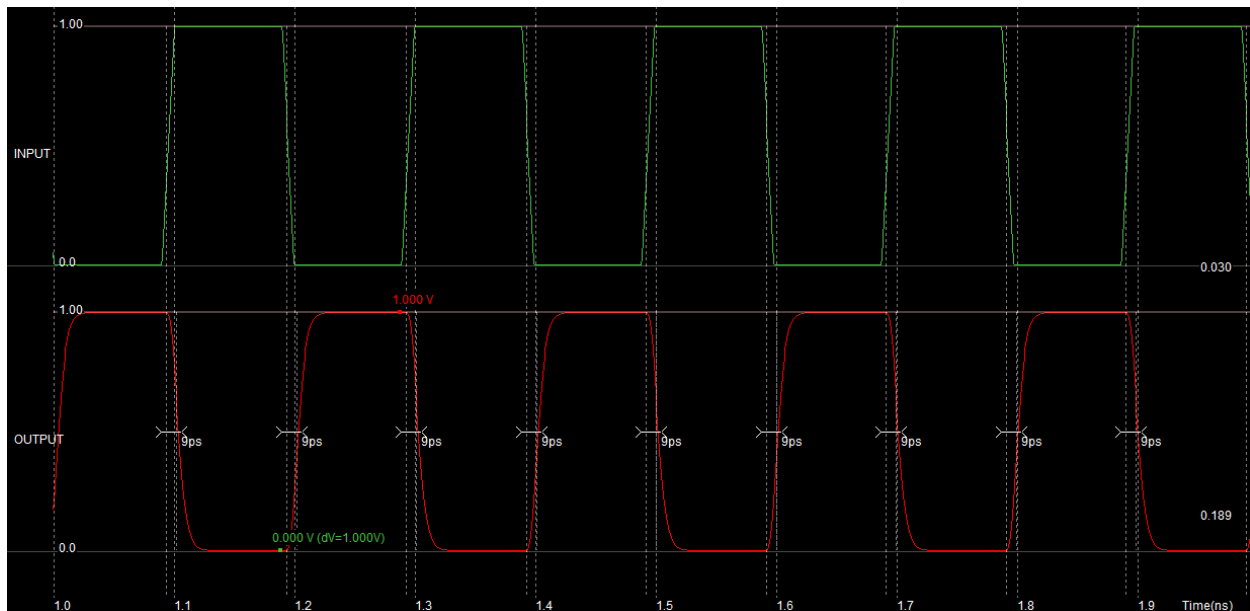


Fig.3

From fig.3 we see that there is a delay between input and output, this is based in our routing and how we build our layout.

Then we generate out netlist for PSPICE:

Netlist:

CIRCUIT example.MSK

*

* IC Technology: CMOS 65nm general purpose - 8 Metal copper - strain - SiON oxide

*

VDD 1 0 DC 1.00

VINPUT 6 0 DC 0 PULSE(0.00 1.00 0.09N 0.01N 0.01N 0.09N 0.20N)

*

* List of nodes

* "s4" corresponds to n°3

* "INPUT" corresponds to n°6

*

* MOS devices

MN1 0 6 3 0 N1 W= 0.35U L= 0.035U

MP1 1 6 3 1 P1 W= 0.70U L= 0.035U

*

C2 1 0 0.617fF

C3 3 0 0.962fF

C4 1 0 0.394fF

C6 6 0 0.047fF

*

*

* n-MOS BSIM4 :

* low leakage

.MODEL N1 NMOS LEVEL=14 VTHO=0.35 U0=0.055 TOXE= 1.1E-9 LINT=0.010U

+K1 =0.450 K2=0.100 DVT0=2.000

+DVT1=0.750 LPE0=0.200e-9 ETA0=0.080

+NFACTOR= 1.0 U0=0.055 UA=7.000e-15

+WINT=0.005U LPE0=0.200e-9

+KT1=-0.050 UTE=-1.800 VOFF=0.010

+XJ=0.150U NDEP=170.000e15 PCLM=1.100

+CGSO=100.0p CGDO=100.0p

+CGBO= 60.0p

*

* p-MOS BSIM4:

* low leakage

.MODEL P1 PMOS LEVEL=14 VTHO=-0.32 U0=0.027 TOXE= 1.1E-9 LINT=0.010U

+K1 =0.500 K2=0.100 DVT0=2.000

+DVT1=0.650 LPE0=0.200e-9 ETA0=0.080

+NFACTOR= 1.1 U0=0.027 UA=4.800e-15

+WINT=0.005U LPE0=0.200e-9

+KT1=-0.060 UTE=-1.800 VOFF=0.010

+XJ=0.150U NDEP=170.000e15 PCLM=0.700

+CGSO=100.0p CGDO=100.0p

+CGBO= 60.0p

*

* Transient analysis

*

* (Winspice)

.options temp=27.0

.control

tran 0.1N 1.00N

print V(6) V(3) > out.txt

plot V(6) V(3)

.endc

.END

Then we use our inverter to do buffer, simply we put to inverter in cascade:

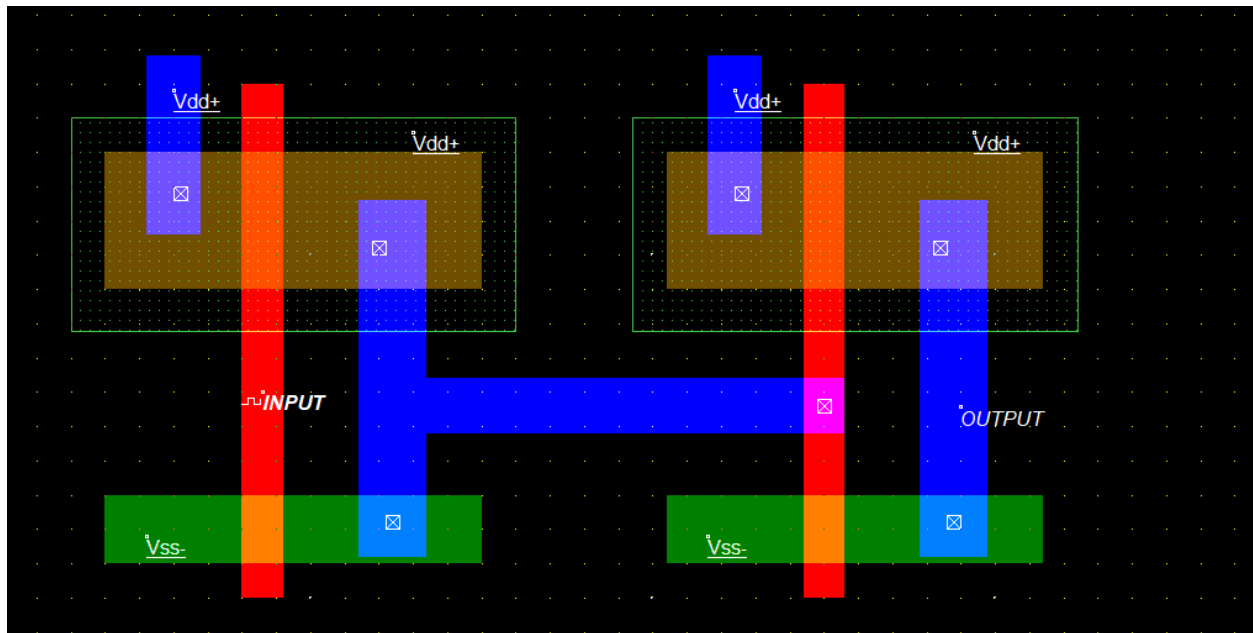


Fig.4

And we obtained the following output:

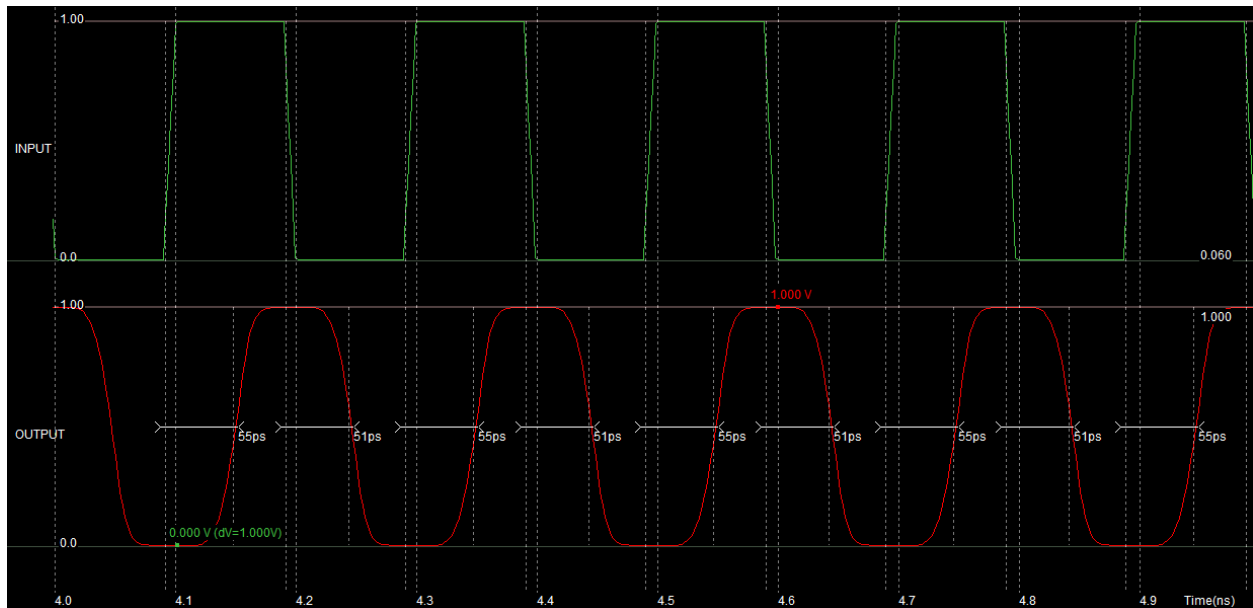


Fig.5

Then we do PSPICE simulation:

(note: in this section I helped with this link in youtube:
<https://www.youtube.com/watch?v=YUbrjbJ4y4>

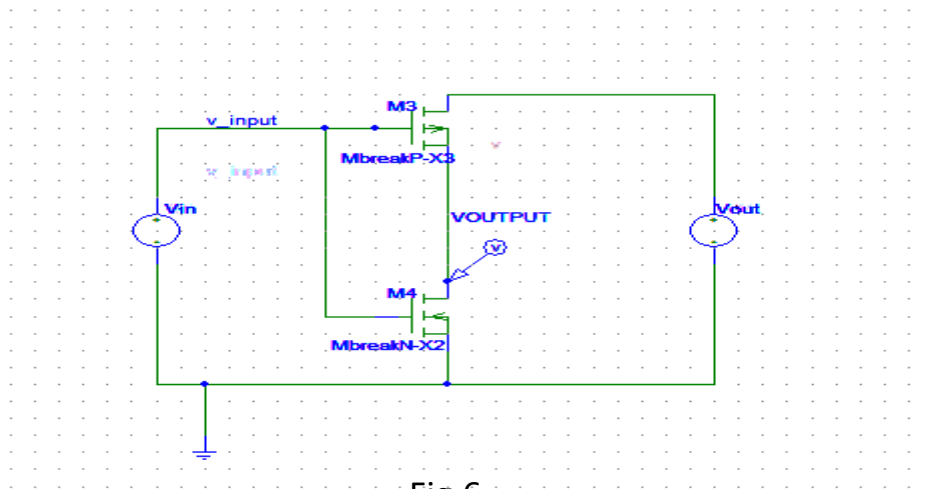


Fig.6

```
.model MbreakP-X3 PMOS (  
LEVEL=2  
VTO=-1.4  
Kp=0.2m  
)  
*$
```

```
.model MbreakN-X2 NMOS (  
LEVEL=2  
VTO=1.4  
Kp=0.6m  
)  
*$
```

Then we obtained the following output (note this graph in DC sweep with varying VIN from 0 to 5)

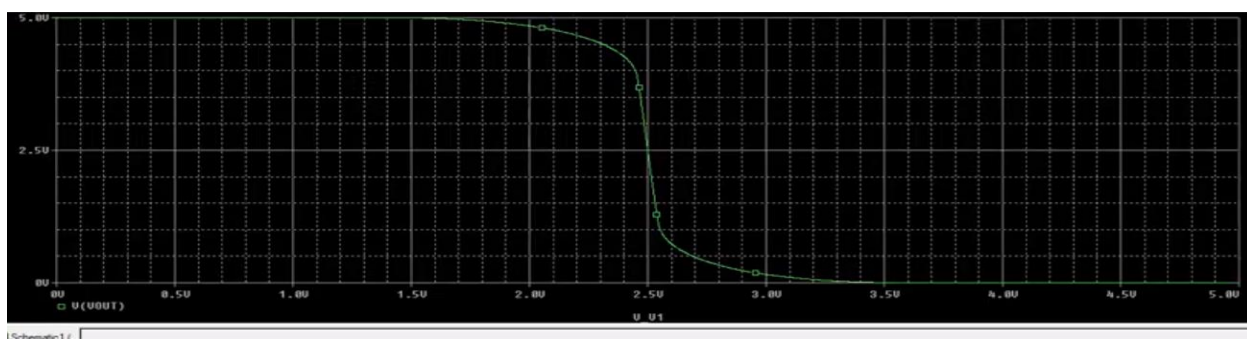


Fig.7

So, from fig.7 we see as V_{in} change from 0 to 5 volt, V_{out} change from 5 to 0 volt, so it is work as inverter. It seen from fig.7 that there is a delay between input and output this reasons refer to the type of transistors that we used.

To compare Microwind result with PSPICE result, in both cases we obtained an inverter but the delay different between them, the reasons is that here there is a drop in voltage in wires and component.

Prepared by
Fadi armoush
1160302