جامعة بيرزيت
BIRZEIT UNIVERSITY

ENCS 333

(HOMEWORK #5)

Student name: Fadi Armoush

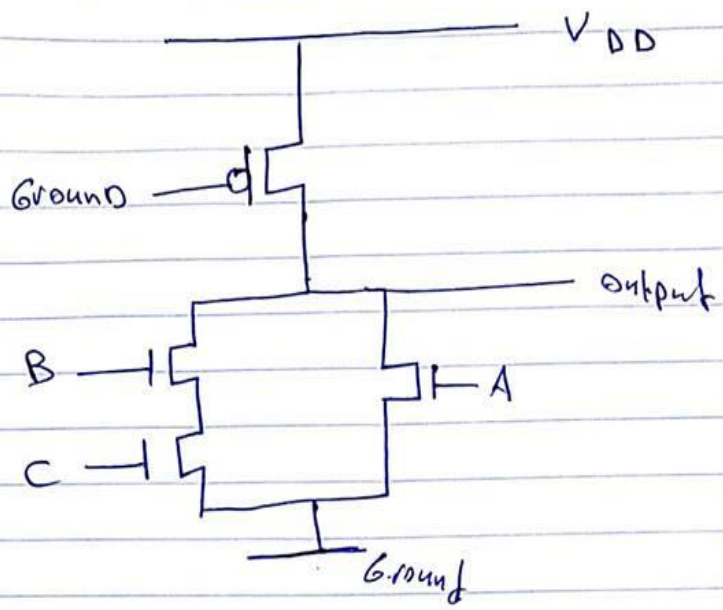
Student number: 1160302

Instructor: Dr. Khader Mohammad

Section: 1

Question one:

1.



2. $output = \overline{(A + BC)}$

Since the PMOS connected to the ground it is pseudo NMOS circuits.

3. yes of course, since it is used less numbers of transistors than fully complementary CMOS, In addition it is more faster than it.

Question two:

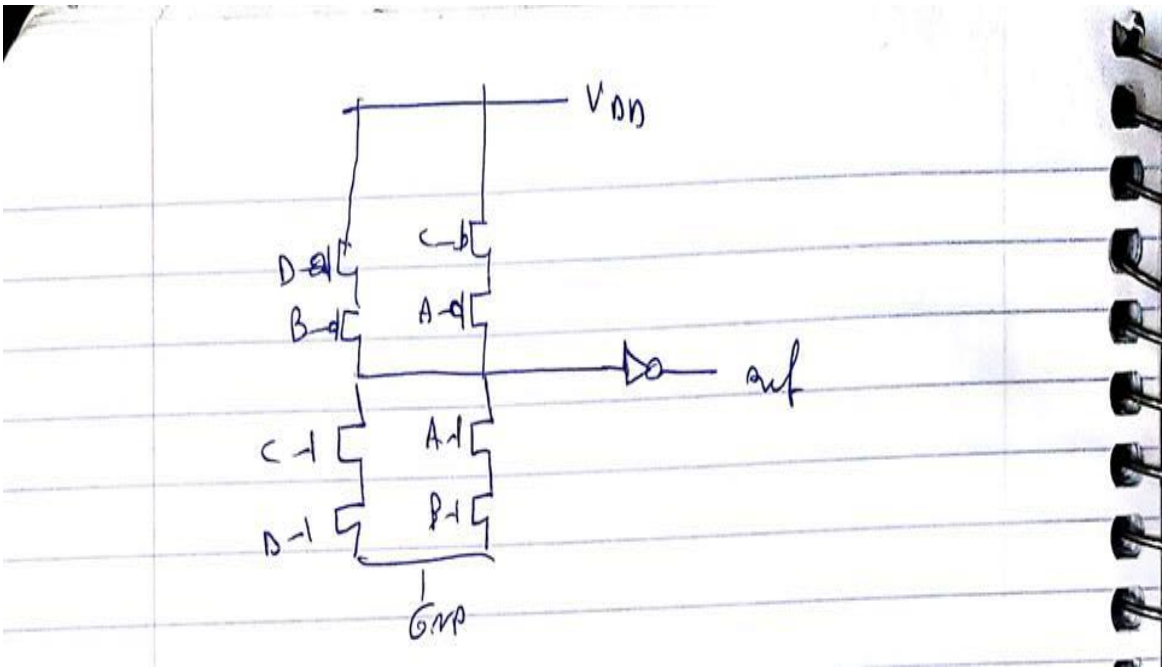
First we need to implement a four input XOR gate, we know that XOR gate is odd function (i.e. the function is one when the number of ones from inputs is odd).

Truth table for 4-input XOR gate:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1

1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

So, function is:



Then we will build the layout:

From the previous graph:

Delay=1.54ns-1.50ns=0.4ns < 0.5ns → our design is accepted.

Also It obvious from the layout that our design occupies less than 500 square microns.

From our result, we see that our design work correctly as four input XOR gate. → our work is accepted.

Prepared by

Fadi armoush

1160302