BIRZEIT UNIVERSITY

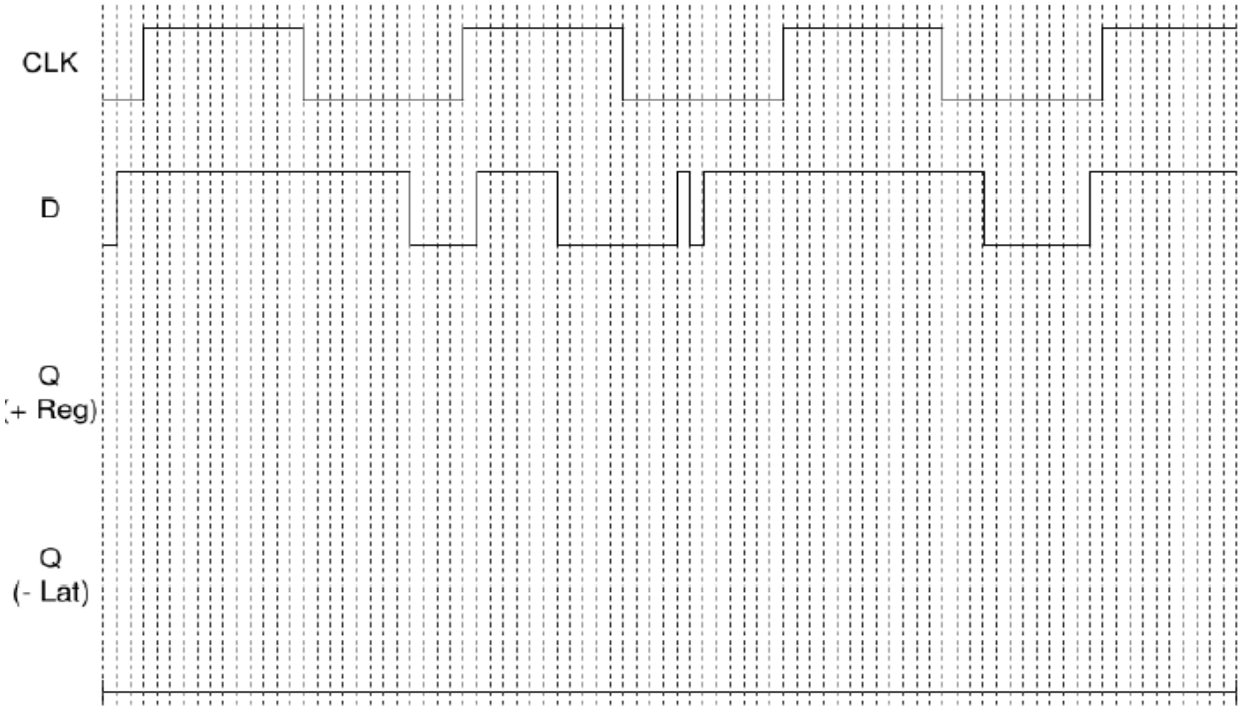
Electrical and Computer Systems Engineering Department
ENCS333
Homework 6

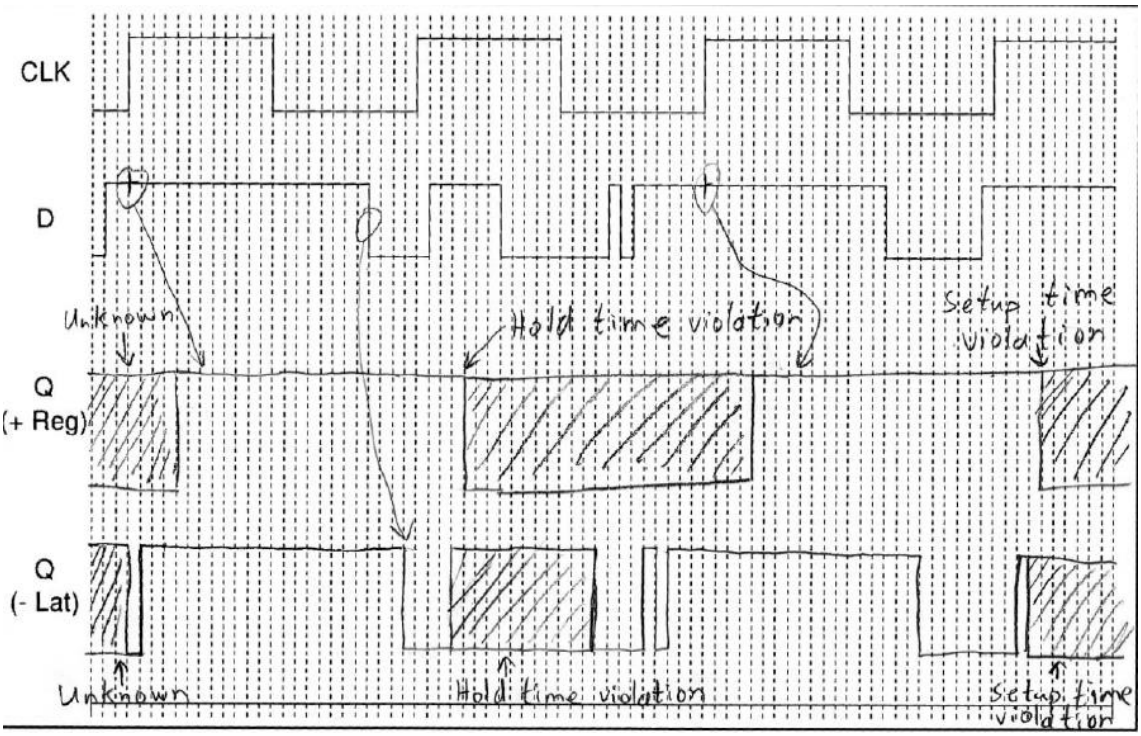
Due December 20th

Question 1

Given the following clock and data waveforms, draw the output waveforms for a
(a) positive edge-triggered register and

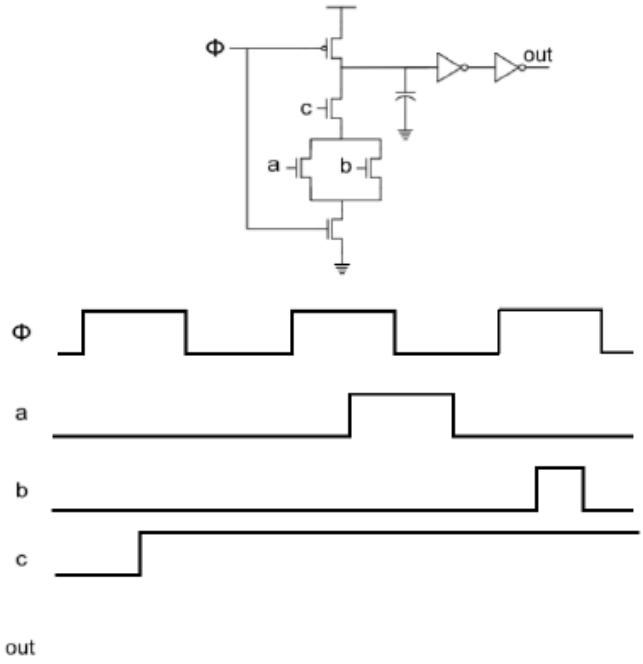
(b) a negative (or transparent-low) latch.
The timing characteristics of these sequential elements follow: $tc \rightarrow Q$ = 4 units, $tD \rightarrow Q$ = 3 units, *tsetup* = *thold* = 2 units. Vertical dashed lines have a separation of one unit. The clock period is equal to 24 units. Clearly mark on the figure where setup and hold time violations occur for each sequential element.

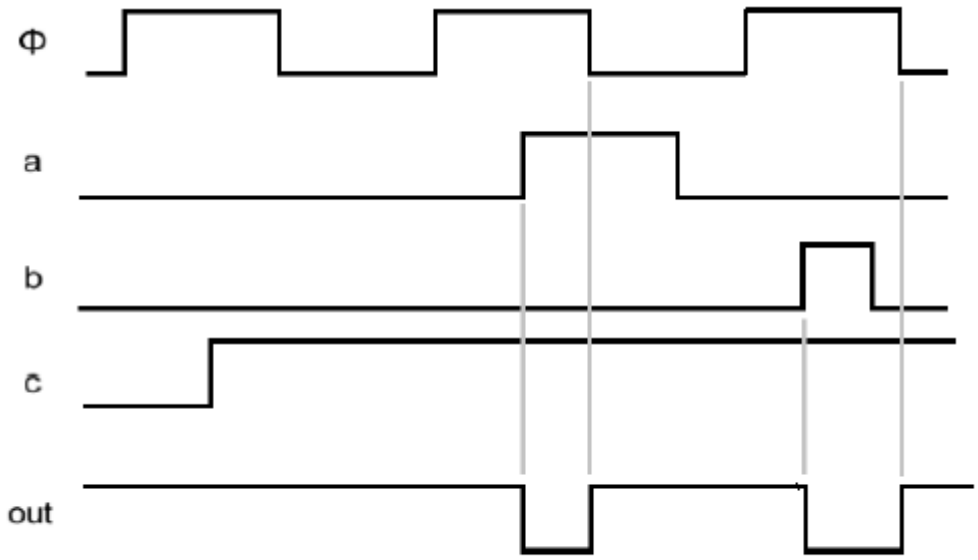




Question 2 :

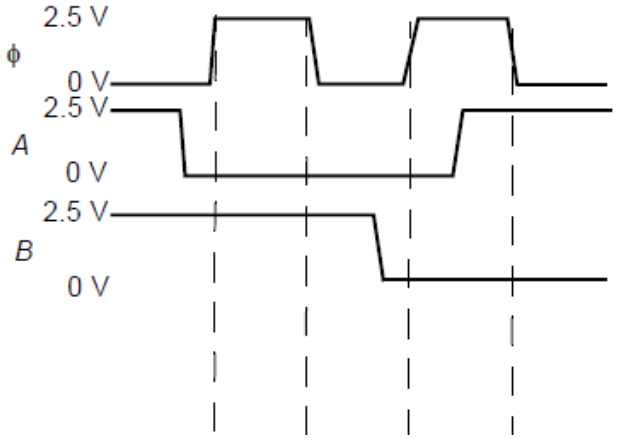
Consider the dynamic gate shown in the following figure. Based on the input signal, draw the output signal.

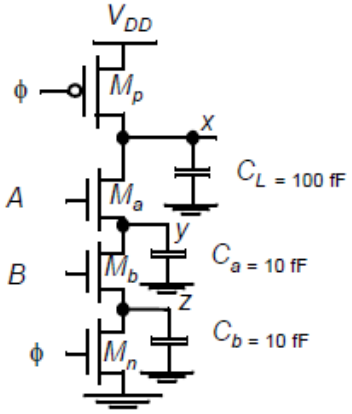


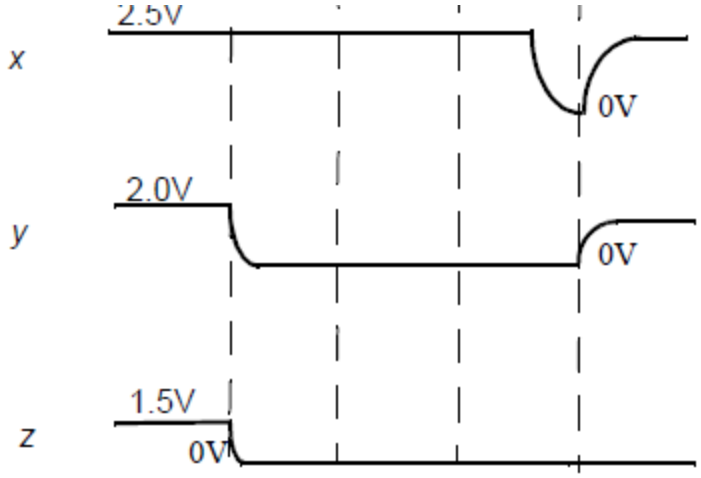


Problem 3

Sketch the waveforms at *x*, *y*, and *z* for the given inputs. You may approximate the time scale, but be sure to compute the voltage levels. Assume that $V_T = 0.5$ V







Problem 4

The simplified layout of a pMOS transistor in a 0.5µm process is shown here with the "actual" fabricated dimensions. Determine the device parasitics below using the following process model values:

k'p =90µA/V^2, |Vtp| = 0.5V, Cox = 1.8fF/µm^2, Cj = 0.75fF/µm^2
and Cjsw = 0.25 fF/µm

a) What is the gate capacitance, C_G?

b) What is the gate-to-drain capacitance, C_{GD}?

c) What is the drain-to-bulk capacitance, C_{DB}?

d) What is the total capacitance at the drain node?

e) If the drain node RC time constant is 4psec, what is channel resistance?

solution:

a) $C_G = Cox\ (W\ L) = (1.8fF/\mu m^2)\ (2\mu m)\ (0.5\mu m) =$ **1.8fF**

b) $C_{GD} = \frac{1}{2}\ C_G = \frac{1}{2}\ (2f) =$ **0.9fF**

c) $C_{DB} = C_j\ A_{Dbot} + C_{jSW}\ P_{DSW}$

$A_{Dbot} = 2\mu m \times 1\mu m = 2\mu m^2$

$P_{DSW} = 2\ (2\mu m + 1\mu m) = 6\mu m$

$C_{DB} = C_j\ A_{Dbot} + C_{jSW}\ P_{DSW} = 0.75f\ (2) + 0.25f\ (6) =$ **3fF**

d) Total capacitance at the drain node is

$C_D = C_{GD} + C_{DB} = 0.9 + 3 =$ **3.9fF**

e) $\tau = Rn\ C_D \rightarrow Rn = \tau/C_D = 4p/3.9f =$ **1,025 Ω**

a) N-channel MOSFET

Cut Off	$V_{GS} \le V_T$	$I_{DS} = 0$
Linear	$V_{GS} > V_T,\ V_{DS} \le V_{GS} - V_T$	$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right](1 + \lambda V_{DS})$
Saturation	$V_{GS} > V_T,\ V_{DS} > V_{GS} - V_T$	$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$

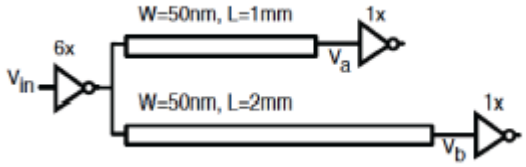
b) P-channel MOSFET

Cut Off	$V_{SG} \le \lvert V_T \rvert$	$I_{SD} = 0$
Linear	$V_{SG} > \lvert V_T \rvert,\ V_{SD} \le V_{SG} - \lvert V_T \rvert$	$I_{SD} = \mu_p C_{ox} \frac{W}{L}\left[(V_{SG} - \lvert V_T \rvert)V_{SD} - \frac{V_{SD}^2}{2}\right](1 + \lambda V_{SD})$
Saturation	$V_{SG} > \lvert V_T \rvert,\ V_{SD} > V_{SG} - \lvert V_T \rvert$	$I_{SD} = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}(V_{SG} - \lvert V_T \rvert)^2(1 + \lambda V_{SD})$

Problem 5: Elmore Delay

For the following problem, $C_G = C_D$ = 2fF=um, the minimum sized (labeled as 1x in the picture) inverter has L = 0:1um, W_p = 2um, W_n = 1um and for this technology $R_{n,\,on}$ = 10kOhm/sq: (i.e. the resistance of an NMOS with width W and length L is equal to 10k Ohm $_{L/W}$) and $R_{p,\,on}$ = 20k=sq: (i.e. the resistance of a PMOS with width W and length L is equal to 20k $_{L/W}$). Note that a 6x inverter has 6 times the width of a 1x inverter

For the wire, R_{wire} = 0:1=Ohm/sq:, the parallel plate capacitance is C_{pp} = 20aFfum$_2$ and the fringing capacitance per each side of wire is C_{fr} = 14aF/um. The wire widths and lengths are shown in the picture..



a) Using the _ wire model, draw the equivalent RC switch model. What is the propagation delay from a step at Vin to Va and Vb?

$$C_{o,6x} = 6 \cdot C_{o,1x} = 36fF$$

- For the top wire:

$$R_{w1} = 0.1\Omega \frac{1000\mu m}{0.05\mu m} = 2k\Omega$$

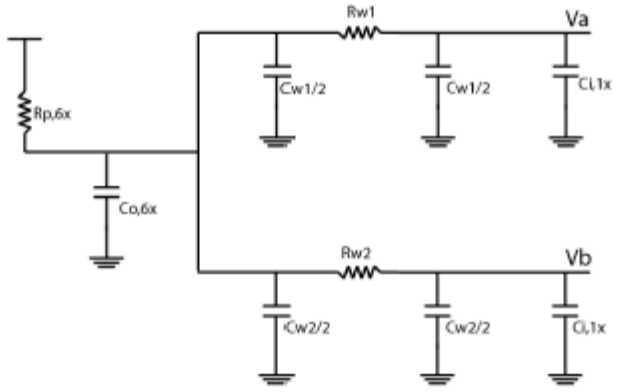
$$C_{w1} = 20aF/\mu m^2 \cdot 0.05\mu m \cdot 1000\mu m + 2 \cdot 14aF/\mu m \cdot 1000\mu m = 29fF$$

- For the bottom wire:

$$R_{w2} = 2 \cdot R_{w1} = 4k\Omega$$

$$C_{w2} = 20aF/\mu m^2 \cdot 0.05\mu m \cdot 2000\mu m + 2 \cdot 14aF/\mu m \cdot 2000\mu m = 58fF$$

The equivalent RC circuit is:



The delay from input to V_a is:

$$t_{p,a} = ln2 \cdot R_{w1} \cdot (C_{i,1x} + \frac{C_{w1}}{2}) + ln2 \cdot R_{p,6x} \cdot (C_{i,1x} + \frac{C_{w1}}{2} + C_{i,1x} + \frac{C_{w2}}{2} + \frac{C_{w1}}{2} + \frac{C_{w2}}{2} + C_{o,6x})$$

$$\Rightarrow t_{p,a} = ln2 \cdot 62.38ps = 43.24ps$$

The delay from input to V_b is:

$$t_{p,b} = ln2 \cdot R_{w2} \cdot (C_{i,1x} + \frac{C_{w2}}{2}) + ln2 \cdot R_{p,6x} \cdot (C_{i,1x} + \frac{C_{w2}}{2} + C_{i,1x} + \frac{C_{w1}}{2} + \frac{C_{w2}}{2} + \frac{C_{w1}}{2} + C_{o,6x})$$

$$\Rightarrow t_{p,b} = ln2 \cdot 162.55ps = 112.27ps$$

b) What is the skew (difference in arrival time between Va and Vb)?

$$t_{skew} = |t_{p,b} - t_{p,a}| = 69.03ps$$

- For the 1x inverter:

$$R_{N,1x} = R_{P,1x} = 10k\Omega \frac{0.1\mu m}{1\mu m} = 1k\Omega$$

$$C_{i,1x} = C_{o,1x} = (2\mu m + 1\mu m)2fF/\mu m = 6fF$$

- For the 6x inverter:

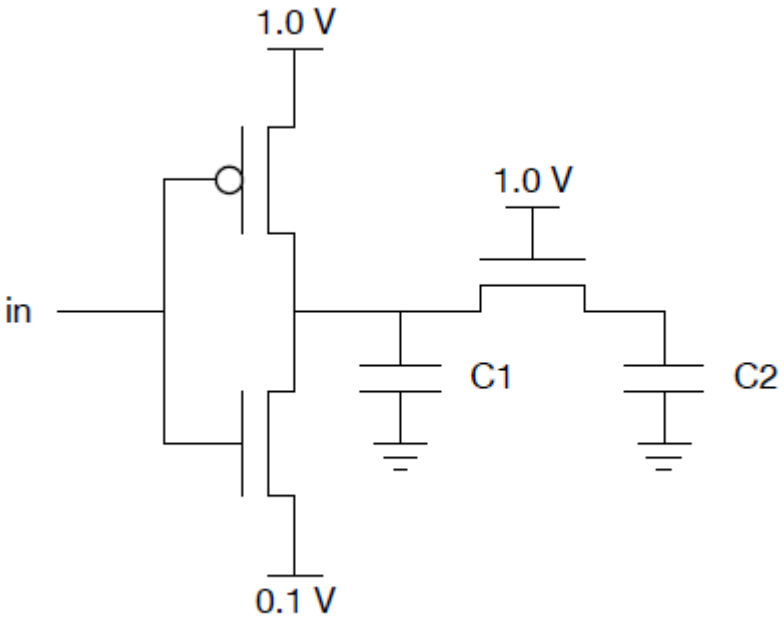
$$R_{N,6x} = R_{P6x} = R_N/6 \approx 167\Omega$$

Problem 6: Energy

Given the circuit below, answer the following questions. Assume that the capacitances associated with the FETs are negligible.

$C_1 = C_2 = 90fF$

$V_{th,n} = jV_{th,p}j = 0{:}4V$



Part a

How much energy is stored in each capacitor after a 1V to 0V transition on `in`? Please show your work.

$E_1 = \frac{1}{2} \cdot C_1 \cdot V_1^2 = \frac{1}{2} \cdot 90fF \cdot (V_{DD})^2 = \frac{1}{2} \cdot 90fF \cdot (1.0V)^2 = 45.0fJ$

$E_2 = \frac{1}{2} \cdot C_2 \cdot V_2^2 = \frac{1}{2} \cdot 90fF \cdot (V_{DD} - V_{th,n})^2 = \frac{1}{2} \cdot 90fF \cdot (0.6V)^2 = 16.2fJ$

Part b

How much energy was drawn by the supply in part a? Is this what you expected? Please show your work.

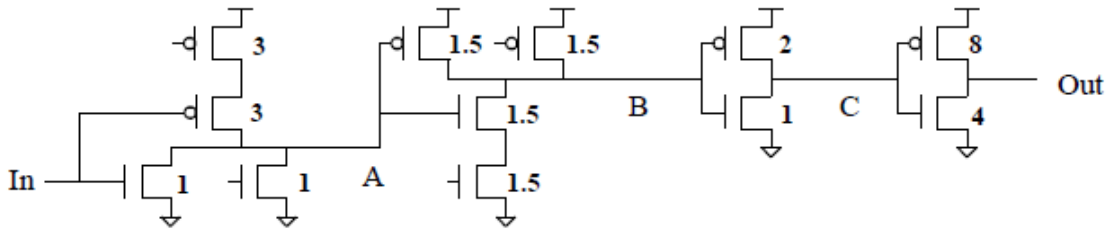
$$E_{supply,1->0} = \int_0^\infty i_{DD}(t) \cdot V_{DD}\, dt = V_{DD} \int_0^\infty C_1 \frac{dV_1}{dt} + C_2 \frac{dV_2}{dt}\, dt = V_{DD} \cdot \left(C_1 \int_0^\infty dV_1 + C_2 \int_0^\infty dV_2 \right)$$

$$E_{supply,1->0} = V_{DD} \cdot C_1 \cdot (V_1(\infty) - V_1(0)) + V_{DD} \cdot C_2 \cdot (V_2(\infty) - V_2(0))$$

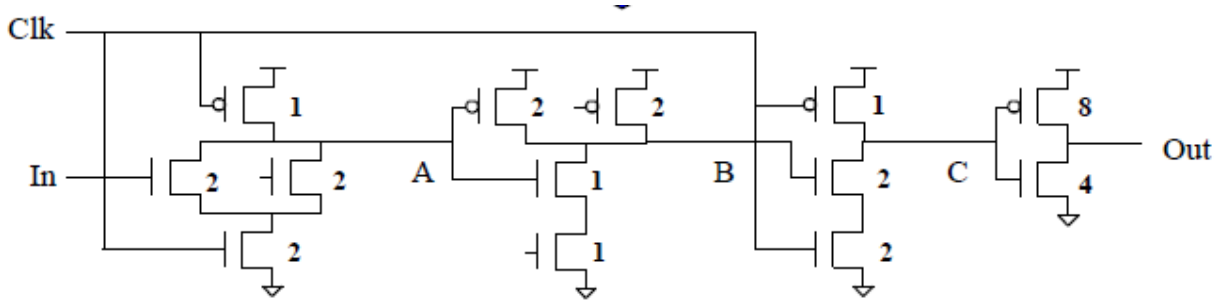
$$E_{supply,1->0} = 1.0V \cdot 90fF \cdot (1.0V - 0.1V) + 1.0V \cdot 90fF \cdot (0.6V - 0.1V) = 126fJ$$

Proplem 7:

1. Given the cstatic logic as shown in figure below, Converted to dynamic logic and size the device accordingly



Solution :



Proplem 8:

What is difference between clk skew and jitter

Skew and Jitter: Definition

Skew and Jitter are the enemy of a clocking system.

Skew is the “static” time difference between any 2 electrical nodes. Typically with reference to clock signals that should in theory switch simultaneously.

There are techniques to reduce or eliminate skew.Skew can be “managed” to your advantage (i.e. intentional skew can be used to provide “cycle-stealing” capability)

Jitter is a “dynamic” time difference of a signal with respect to an ideal signal.Jitter can not be typically “designed-out”.

Jitter can result from various time-dependent noise events.

Proplem 9:

Clock distribution is one of the most critical areas in the design of high performance VLSI chips. Poor clock distribution can result in excessive clock skews between clusters on the chip, reducing the maximum operating frequency. In general we need to reduce the effect of clock skew on the chip. What are the list of things that is required to do that ?

Reducing the wire delay and RC effects by making the effective delay small and balancing the delays of all the paths. (This changes a total delay problem to a matching delay problem.)

Matching the clock buffer delay

Reducing the process variations sensitivities by careful placement and design of the of clock buffers.

A side effect of long clock distribution delays is increased jitter due to supply voltage variations. This adversely affects the PLL used to generate the chip clock frequency.

Proplem 10

Write the equation for dynamic power consumption and the equation for static power consumption. Explain the circuit characteristics (e.g., Vt, temperature, or gate size) that each depends on. Point out recent trends for these characteristics.

Slides have solutions

Proplem 11

The simplified layout of a pMOS transistor in a 0.5µm process is shown here with the "actual" fabricated dimensions. Determine the device parasitics below using the following process model values:
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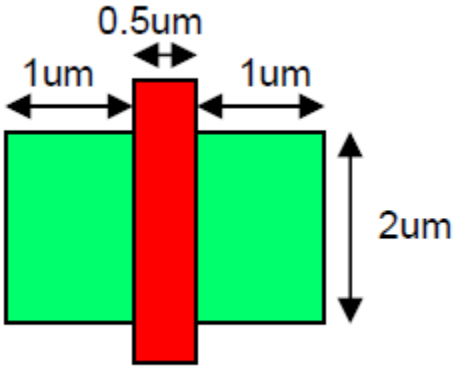
e) If the drain node RC time constant is 4psec, what is channel resistance?



solution:

a) $C_G = Cox\ (W\ L) = (1.8fF/\mu m^2)\ (2\mu m)\ (0.5\mu m) =$ **1.8fF**

b) $C_{GD} = \frac{1}{2}\ C_G = \frac{1}{2}\ (2f) =$ **0.9fF**

c) $C_{DB} = C_j\ A_{Dbot} + Cj_{SW}\ P_{DSW}$

$A_{Dbot} = 2\mu m \times 1\mu m = 2\mu m^2$

$P_{DSW} = 2\ (2\mu m + 1\mu m) = 6\mu m$

$C_{DB} = C_j\ A_{Dbot} + Cj_{SW}\ P_{DSW} = 0.75f\ (2) + 0.25f\ (6) =$ **3fF**

d) Total capacitance at the drain node is

$C_D = C_{GD} + C_{DB} = 0.9 + 3 =$ **3.9fF**

e) $\tau = Rn\ C_D$ ⇒ $Rn = \tau / C_D = 4p/3.9f =$ **1,025 Ω**

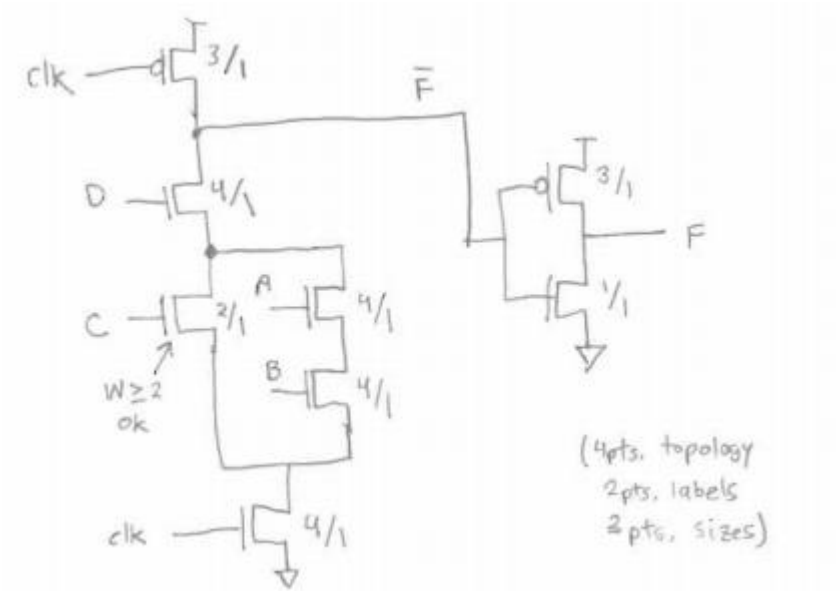
Problem 2.2 (2 points) Suppose the inverter you designed in Problem drives a total capacitance of 45fF at 4.1GHz. How much power does it consume assuming VDD = 5V?

$P = C V_{DD}^2 f$ (1pt.)

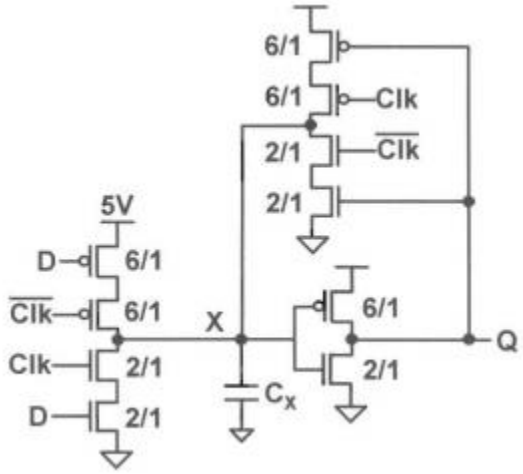
$= (45 \times 10^{-15}\ F)(5\ V)^2 (4.1 \times 10^9\ Hz) = \boxed{4.61\ mW}$ (1pt.)

P roblem 3

Implement the logic function F = AB + CD using a 4-input dynamic CMOS logic gate with a minimum number of transistors and a single minimum-sized inverter ration (1/3). Size the 4-input gate such that the worst case rise and fall times at its output are equal to the minimum-sized inverter.



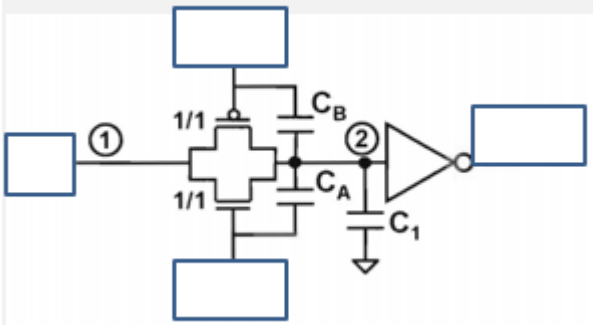
What kind of circuit is the circuit below ? is it dynamic or static circuit ? is it aa latch or ff ?

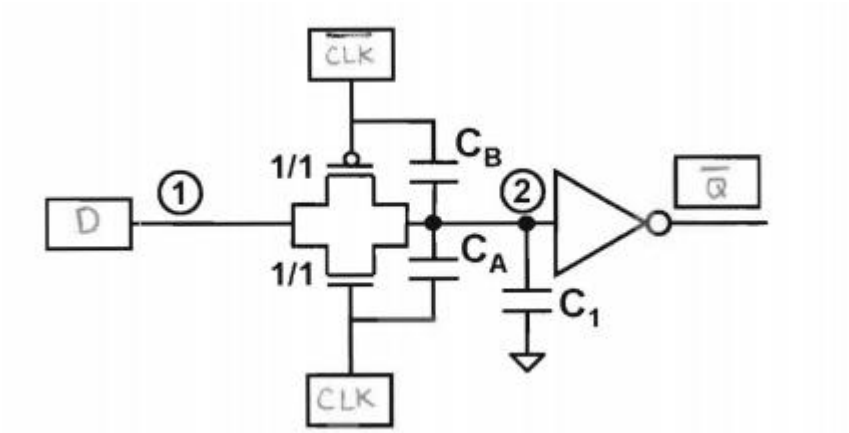


Static positive edge latch

Proplem

For the latch circuit shown in Figure below, label the boxes D, C LK, CLK, Q such that the circuit works as a positive transparent inverting latch.

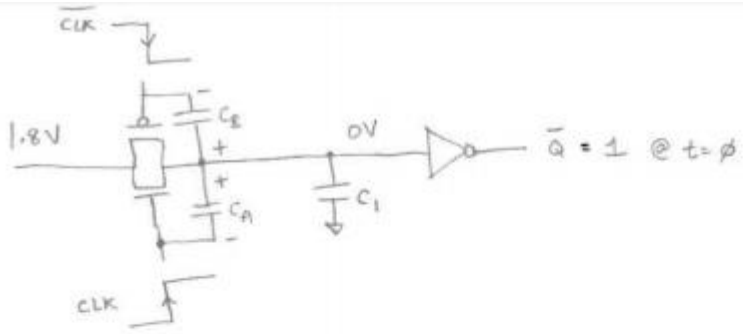




Is the circuit in a static or dynamic latch (circle one)? Justify your answer.

• Dynamic No positive feedback, logic level stored as capacitor charge.

Suppose the latch is used as the slave stage of an edge-triggered flip-flop and that node 1 and node 2 in Figure above are initially at 1.8V and OV, respectively. Assuming Rp = 300ohm for a PMOS device with W/ L = 1/1 and Rn = lOOohm for an NMOS device with W/L = 1/1 , CA = 19fF, CB = 23fF, C1 = 150fF, and tpHL for the inverter is 8.9ps, estimate the clock-to-Q delay for the latch using the switch RC model for the transistors.



$R_{eq} = R_n \| R_p = 100\,\Omega \| 300\,\Omega = 75\,\Omega$

$t_{C \to Q} = 0.69\, R_{eq}\, C_{TOT} + t_{pHL}$

ΔV for $C_B = 1.8V - (-1.8V) = 3.6V$ ← Miller effect

ΔV for $C_1 = 1.8V - 0V = 1.8V$

ΔV for $C_A = 0V - 0V = 0V$ ← ignore C_A's contribution to delay

$C_{TOT} = C_1 + 2C_B = 150\,fF + 2 \cdot 23\,fF = 196\,fF$

$t_{C \to Q} = 0.69 \cdot 75\,\Omega \cdot 196\,fF + 8.9\,ps$

$\boxed{t_{C \to Q} = 19.043\,ps}$

$C_{TOT} = C_1 + C_A + C_B = 192\,fF \Rightarrow t_{C \to Q} = 18.836\,ps$

$C_{TOT} = C_1 + 2 \cdot (C_A + C_B) = 234\,fF \Rightarrow t_{C \to Q} = 21.01\,ps$