Student Name : _____ ID: _____

Question	Full Grade	Student Grade	ABET OUTCOME
1	20		
2	20		
3	20		
4	15		
5	25		

Question 1: (20POINTS)

1. **Integrated circuits (IC) is a complex set of electronic components and their interconnections etched on a chip (T / F)**

2. **Role of IC Package : Package of IC providing possibilities of Power supply connections, Input and output of information signals, Protection from external environment and Heat removal (T / F)**

3. **CMOS ICs are fabricated on circular slices of silicon called _____**

4. **We can define the 'threshold voltage' as the V_{GS} that below it the transistor's current (I_{DS}) effectively reach maximum value. (T / F)**

5. **CMOS domino logic has**
   a) smaller parasitic capacitance b) larger parasitic capacitance c) low operating speed d) very large parasitic capacitance
6. **The IN and OUT bus lines in IC design should be in**
   a) metal b) polysilicon c) diffusion d) silicon
7. **Buffers are needed to drive**
   a) small capacitance b) large capacitance c) small resistance d) large resistance
8. **What type of power <u>short circuit</u> or <u>dynamic</u> or <u>Leakage</u> does the Sub-threshold current affect the most?**

9. **Body effect will result in <u>larger</u> OR <u>smaller</u> VT? How does that affect performance of the device, does it make it <u>Slower</u> OR faster? (2 Point)**

10. **Hot-e degradation in devices happens When a MOS transistor is in <u>Linear</u> OR <u>cut off</u> OR <u>saturation</u> region. This affect which gate the most _____ (2 Point)**
11. **GDSII file is _____ RTL/schematic/Layout file and it is in _____ the form of ASCI/DECEMEL/BINARY format, therefore it is not readable by the user. (2 Point)**
12. **List 2 methods used for Low power design techniques : (2 Point)**

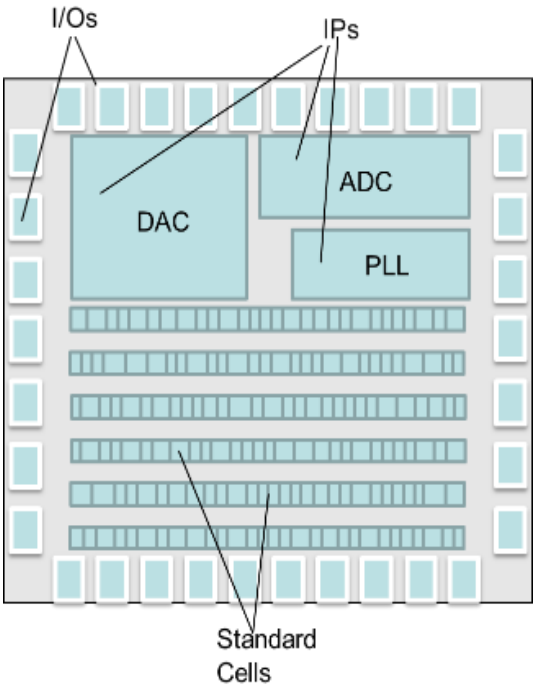
13. **The design flow of IC VLSI design system is : (2 Point)**
    1. architecture design 2. Market requirement 3.Layout 4. HDL coding 5. logic design
    a) 2-1-5-4-3 b) 4-1-3-2-5 c) 5-3-2-1-4 d) 5-1-2-3-4
14. **Basic Steps/flow of Synthesis: (2 Point)**
    1- Circuit description 2. Logic Circuit 3. Layout 4. Physical Synthesis 5.Logic Synthesis

    a) 2-1-5-4-3 b) 4-1-3-2-5 c) 1-5-2-4-3 d) 5-1-2-3-4

Question 2: (20 POINTS)

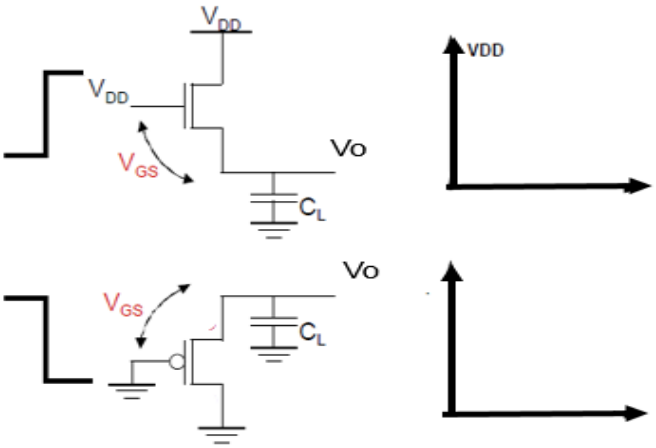
A. Figure below shows IC Component. Please explain Type of design and what does each one of the following cell do : (3 points)

- **Input/Output (I/O) Cells :**
- **Digital Standard Cells**
- **Intellectual Property (IP) Blocks :**

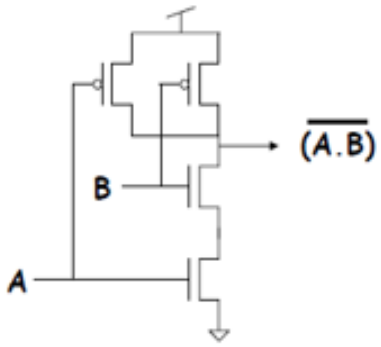


B. Physical structure of devices, draw the NMOS and PMOS structure (CROSS SECTION) and label all parts for each device like Gate, Drain, source , channel, P+, N+, N-WELL, Substrate. (4 points)

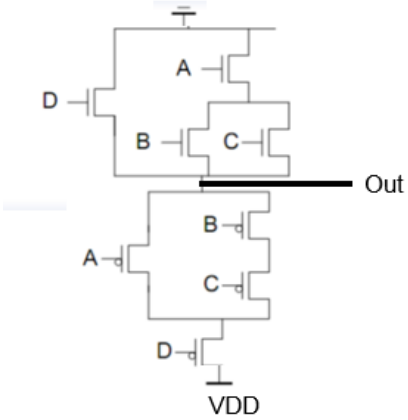
C. In the figure below draw Vo for each device and make the Source and Drain for each device (6 points)



D. For the circuit below draw the complete detailed layout(5 points)



E. What is the output of this function? (2 points)



Question 3: (20 POINTS)

A. Draw transistor level for F= NOT ((ABC)+D) , consider D is the signal that comes the latest (5 POINTS)

B. Given the spice netlist below, draw the circuit (transistor level) (3 points)

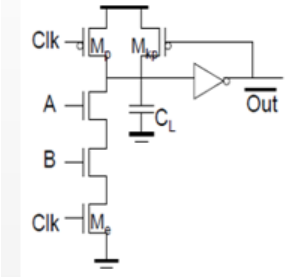
*.subckt **xxy***

mt1 out in vdd nmos l = 0.1u w = 0.75u

mt2 out in vdd pmos l = 0.1u w = 0.55u

.ends

C. For the circuit shown below, what Type of circuit we have? What is the output of this circuit? What does the transistor Mkp used for? Is there another way to connect Mkp to do the same job? (5 points)

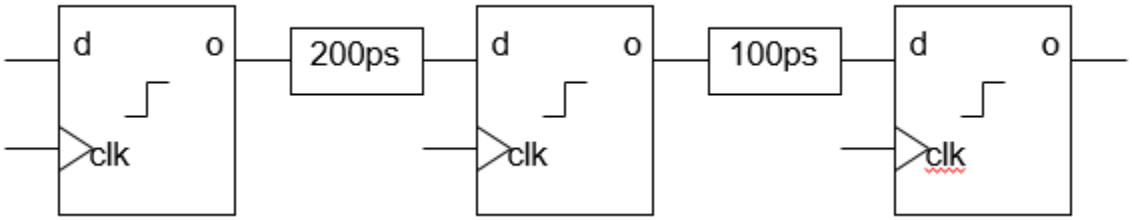


D. Draw circuit level for Traditional P-Latch (Phase 2 Latch) (using inverters symbol and transistor) (5 points)

E. What are the two paths delay in the above latch OR ANY LATCH ? (2 POINTS)

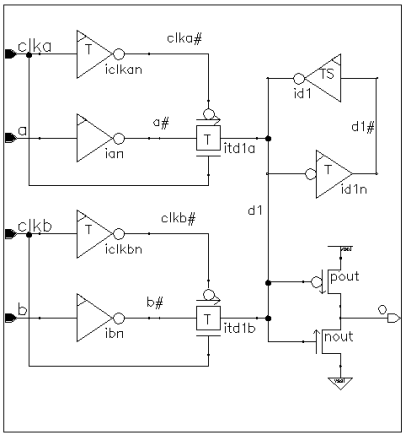
Question 4: (15 POINTS)

A. Given the circuit below, Assuming 100ps setup time, skew and clk-out delay , How many paths are there and how many cycles? What is max frequency this circuit could run? (10 points)



B. How can we increase frequency of the above system? (2 points)

C. What does this circuit do? (3 Points)



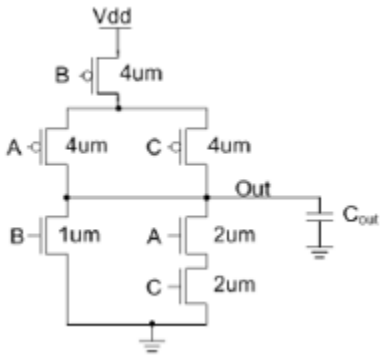
Question 5: (25POINTS)

A. In 0.18um TSMC technology, 5x minimum inverter with effective resistance of 3Kohm , driving FO4 load (25fF) , what is delay ? if we change process to 0.10um do you expect delay to increase or decrease, explain your answer (3 points)

B. For the circuit shown below, (6 points)

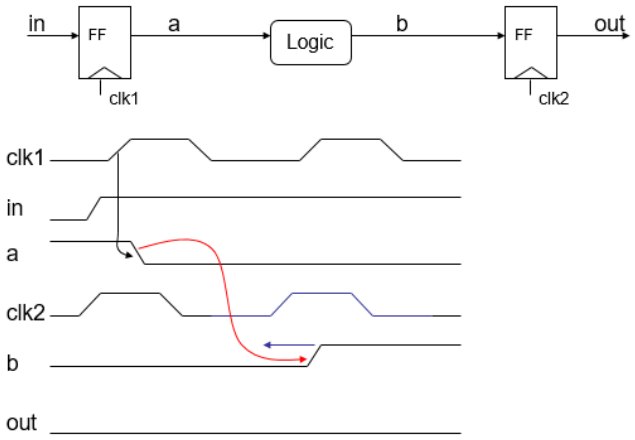
For this problem you should assume that L_{min} = 100nm, C_g=2 fF/μm, C_d=1.6 fF/μm, R_p=20 kΩ/□, and R_n=10 kΩ/□, C_{out} = 12fF.

a) If A = 1 and B = 0, draw the switch model you would use to calculate the delay of the gate when C transitions from 1 to zero (i.e., the output going high).

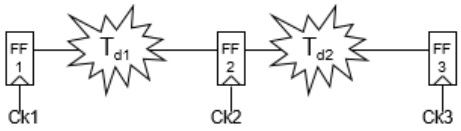


b) What is the delay of the gate in this case?

C. For the circuit below, based on timing diagram what type of failure we have ? How can you fix it? (3 points)



F. What is the Setup Margin in the circuit below from FF1→FF2 (5 points)



T_{d1}	0.185		T_{d2}	0.155
Clk->Q_{FF1}	0.023		$Setup_{FF1}$	0.038
Clk->Q_{FF2}	0.025		$Setup_{FF2}$	0.037
Clk->Q_{FF3}	0.024		$Setup_{FF3}$	0.041
$MaxSkew_{Ck1-Ck2}$	0.015		$MaxSkew_{Ck2-Ck3}$	0.010
Tcycle	0.250		Jitter	0.016

G. What type and Where Does Power Go in CMOS logic? How we can minimize the power loss in CMOS logic? (3 points)

H. What type of clock buffers usually we have in a system? (2 points)