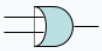
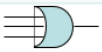
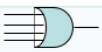
Question	Full Grade	Student Grade	ABET OUTCOME
1	10		a
2	20		a
3	20		c
4	20		c
5	20		k
6	20		k

Question 1 (10)

A) Show how you can optimize the design for power given that: **(4 points)**

Y= a + b + c + d given that power per cell is given as shown below

Cell	Power
	2
	2.5
	3

B) Explain the difference between latch and FF? **(4 points)**

C) What do we mean by Transparency? Does it affect latch based design or FF based design? **(2 points)**

Question 2 (20)

A) Consider the following CMOS logic circuits: What is the function for each? **(5points)**

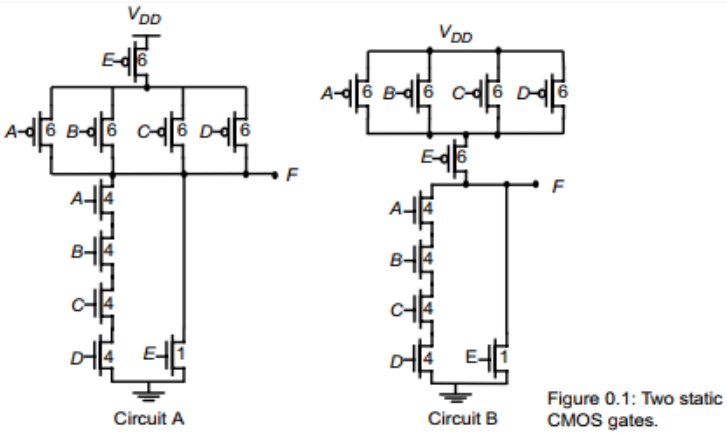
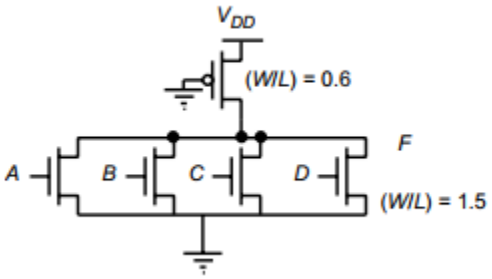
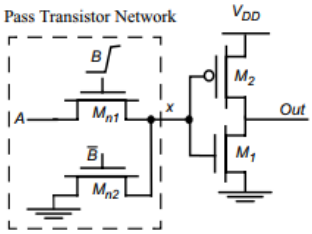


Figure 0.1: Two static CMOS gates.

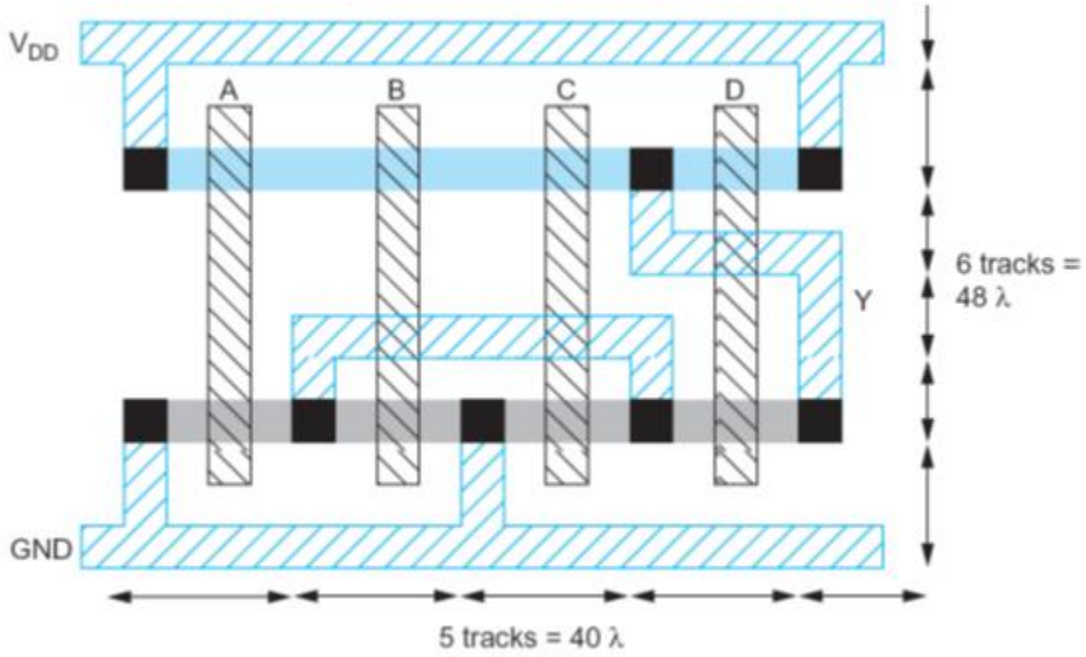
B) For the circuit below, what is the output voltage if only one input is high? If all four inputs are high? Explain your answer. **(4 points)**

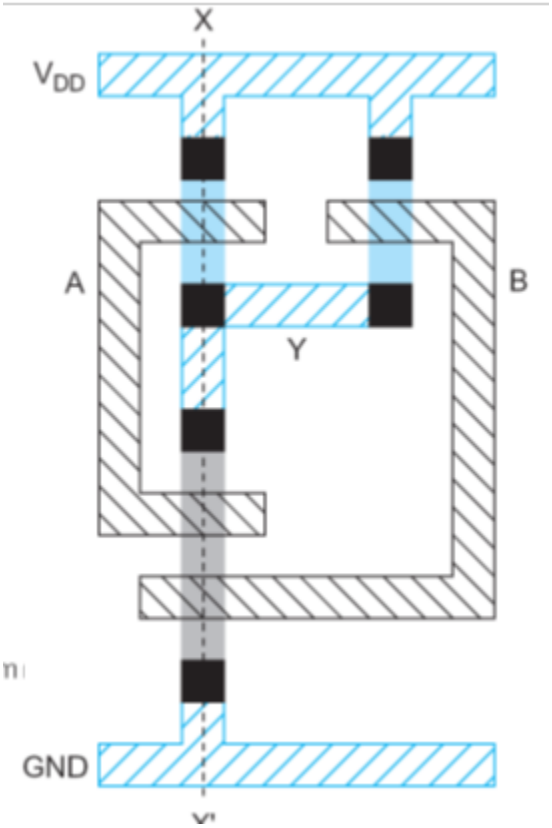


C) Explain why the circuit below has **non-zero static power** dissipation. **(5 points)** Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.



D) What function does this layout represent? **(6 points)**



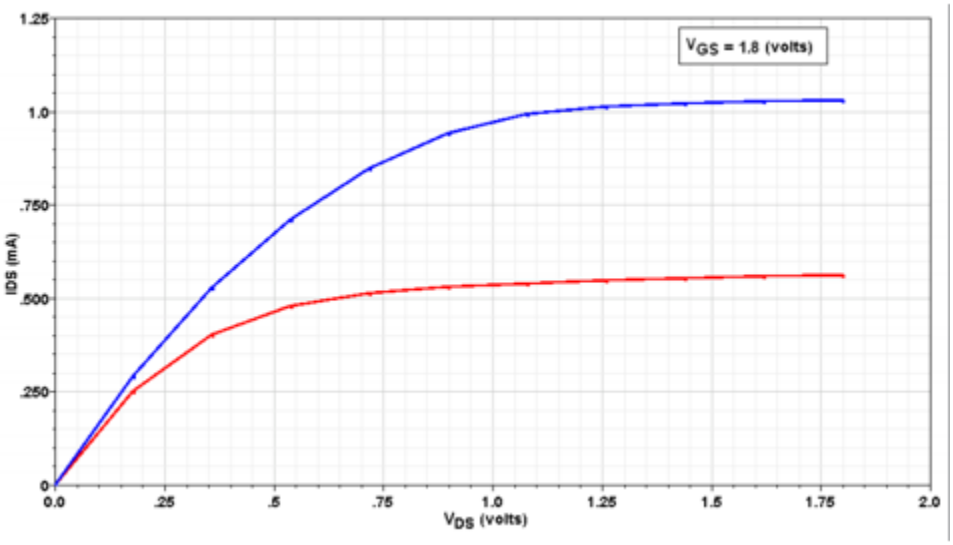


Question 3 (20)

A) If we simulate using 0.18 µm CMOS technology environment, the following two CMOS transistors (NMOS type) and we plotted the VDS versus ID for a VGS = 1.8 volts afte we Sweep VDS from 0 volt up to 1.8 volts using 9 steps

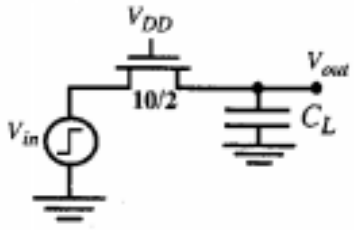
Transistor no.1: was L1 = **0.18 µm** & W1= 5*L1
Transistor no.2: L2 = **1.2 µm** & W2= 5*L2

Below graph shows the simulation results, What do you conclude from comparing both plots , which transistor for which curve? **(6 points)**



B) Consider the following below circuit :

C_L can be assumed to be large and equals 10 pF.



a. Assume that $V_{out}(t = 0) = 0$ V. Determine V_{out} (t = ∞) when V_{in} is raised from 0 V to V_{DD} at $t = 0$. Assume $V_{DD} = 3$ V. You may assume that $L = L_{eff}$, or that the lateral diffusion can be ignored in this problem. **(4 points)**

c. Determine the energy that is stored on C_L at the end of the low-to-high transition. How much energy was dissipated in the MOS transistor? How much was delivered by the input source? **HINT: Derive the results; Do not take the equations in the book for granted!** **(6 points)**

d. Assume that the NMOS is replaced by a PMOS device of the same size with its gate connected to GND. Determine the impact on the following design parameters, and give a short explanation

(6 points)

1. V_{out} (t = ∞)
   - o Larger
   - o Equalm
   - o Smaller

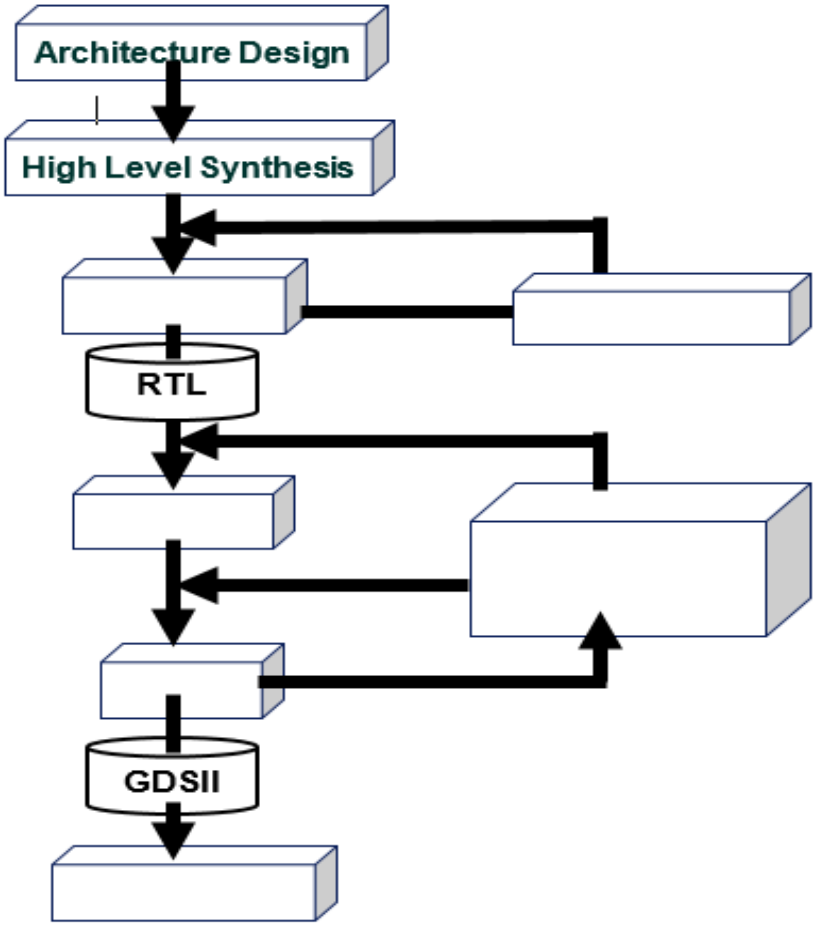
2. t_{pLH}:
   - o Larger
   - o Equalm
   - o Smaller

e. Describe in a couple of sentences how you would decrease the delay of this gate. Is there an absolute lower limit on the delay, and if yes explain why and give an approximate value of this delay.:

(3 points)

Question 4: (20 points)

A) Complete the missing block name from the level design flow for chip/IC (6 points)



B) The transistor **current changes** with the operating temperature mainly through the mobility and Vt temperature dependences. Explain how does Te temperature affect the current? **(2 points)**

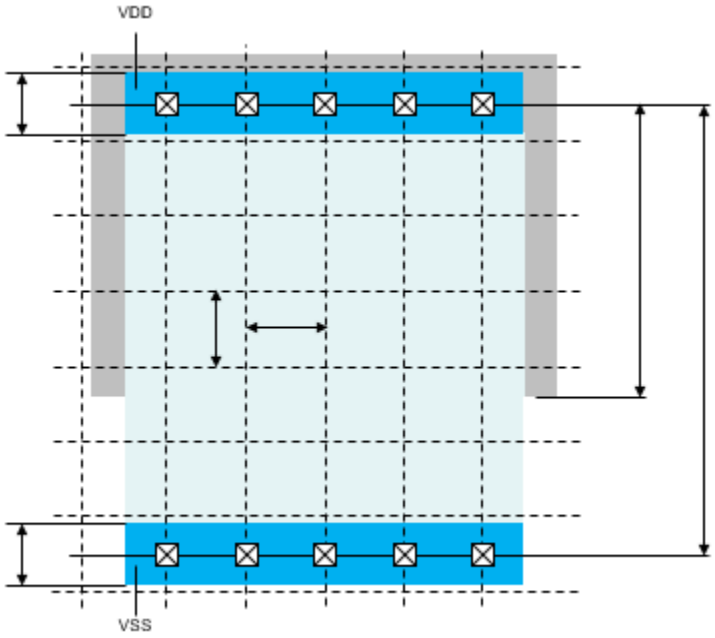
C) When the hot-e happens (which region of operation) and how can we avoid it? **(2 points)**

D) What are the main three Physical Synthesis Steps? **(3 points)**

E) Is it true that all clock pins are driven by a single clock source for the same chip? If yes/no explain why? **(2 points)**

F) Given that the physical structure for standard cell design is shown below, match or mark the following parameters to the cell **(5 points)**

Parameter	Symbol
Cell height	H
Power rail width	W_1
Vertical grid	W_2
Horizontal grid	W_3
N-Well height	W_4



Question 5: (20 points)

A) Draw dynamic logic gates for F= $\overline{((AB)+C)}$ **(2 points)**

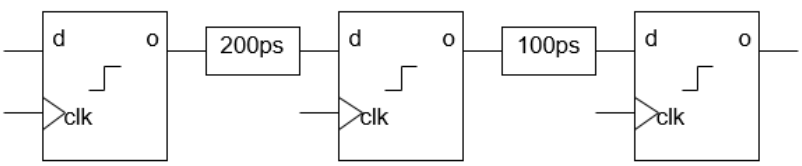
B) What are the main Issues in Dynamic Design and how we can fix/avoid ? **(2 points)**

C) Define (4 points)

- Setup time
- Hold time
- Clk to out delay
- Data to out delay

D) Based on the figure below, Assuming 100ps setup time, skew and clk-out delay **(8 points)**

- How many paths are there and how many cycles? **(2 points)**
- What is max frequency this circuit could run? **(3 points)**
- What are the advantage of time borrowing? How can we benefit of time borrowing in this question ? **(3 points)**

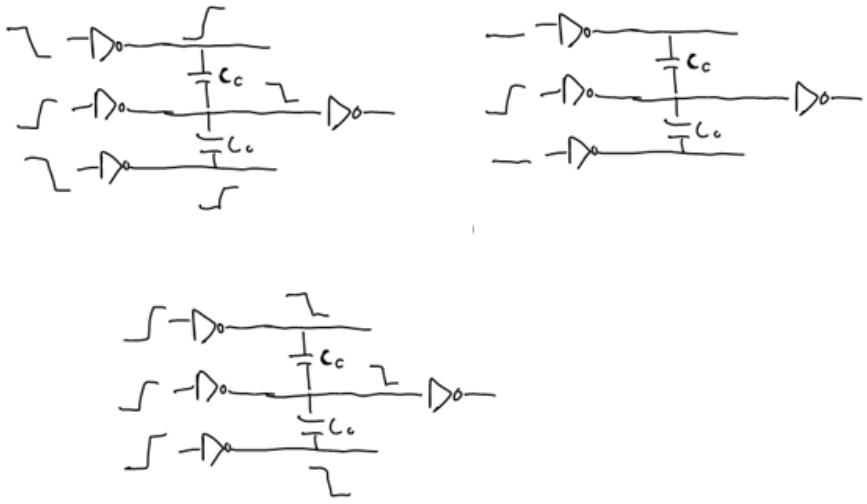


Question 6: **(20 points)**

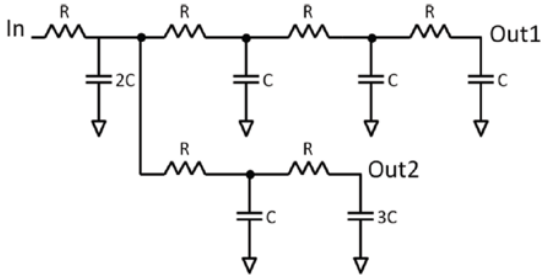
A) What are the two line model? **(2 points)**

B) Why and where we use repeaters? **(3 points)**

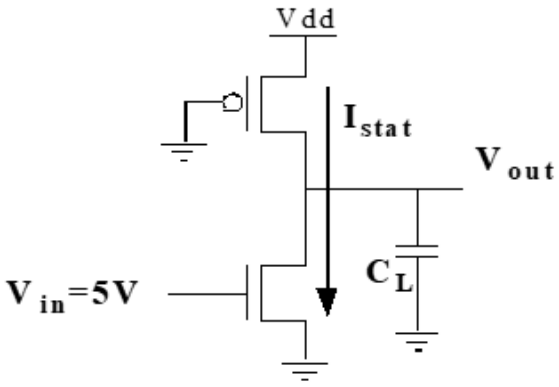
E) What is Coupling Capacitance? Which of the below figures have bigger coupling caps? **(4 points)**



F) Calculate Elmore delay from In to out1 and from In to out2? (5 points)



G) What kind of power dissipation in each circuit below : (3 points)



H) What type of power we define as : $P = \alpha f C V_{DD}^2$, what does each factor represent and how it affect the power ? (3 points)