1. Need to understand and solve all HW questions
2. Area will be covered in :
* Semiconductor material: pn-junction, NMOS, PMOS
* IC Manufacturing Process
* Design Metrics CMOS
* Transistor Devices
* The CMOS inverter
* Combinational logic structures
* Layout design rules
* basic gates
* Static & Dynamic CMOS Logic
1. What are the main design matrices ?
2. Determine the region of operation (Cut off, Linear, Saturation, ..) in the following configurations.
3. What are the three regions of operation of a MOS transistor?
4. Determine the region of operation (Cut off, Linear, Saturation, Vel. saturation) in the following configurations. You may assume that all transistors have identical sizes. VDD = 2.5V. Explain your reasoning, and show your derivations if needed (5 pts).
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1. How does Increasing W of devices affect it’s resistance, Gate capacitance and transconductance ?
2. Q5. What is transconductance of a MOS transistor? Explain its role in the operation of the transistor.
3. Explain the behaviour of a nMOS transistor as a switch.
4. Explain the behaviour of a pMOS transistor as a switch.
5. How one nMOS and one pMOS transistor are combined to behave like an ideal switch.
6. The input of a lightly loaded transmission gate is slowly changes from HIGH level to LOW level. How the currents through the two transistors vary?
7. How its ON-resistance of a transmission gate changes as the input varies from 0 V to Vdd, when the output has a light capacitive load.
8. Draw stick digral/layout for 2-INPUT AND?
9. Mark or point to the active, via/contact , M1, poly , NWELL IN THE FIGURE BELOW



1. Draw schematic and stick diagram for Out= (ABC+D)’
2. What is the difference between Average, maximum and instantious power?
3. Why leakage power dissipation has become an important issue in deep submicron technology?What are the main factors that affects leakage ?
4. Show the basic structure of a MOS transistor.
5. What are the commonly used conducting layers used in IC fabrication?
6. Consider the CMOS inverter from below. If the NMOS transistor has channel width

*Wn* and the PMOS transistor has channel width, *Wp*, label the voltage transfer characteristics from FIG. 2.b that correspond to following device sizes:

A: *Wn* = 5m, *Wp* = 5m

B: *Wn* = 1m, *Wp* = 5m

C: *Wn* = 5m, *Wp* = 1m



1. A CMOS inverter with supply voltage VDD1 = 2V, has to interface to a second CMOS inverter with VDD2 = 2.5V supply, as shown below

The transistor widths of the second inverter *Wn*2, *Wp*2, should be determined to assure reliable

interfacing, since the high output voltage level of the first inverter is *VOH*1 = 2V. If

*Wn*2 = 5m, determine the value of *Wp*2, such that these inverters are interfaced with maximum

and symmetrical noise margins.



1. The inverter from FIG. below . has Wn = 1 mm and Wp = 2.5mm. VDD = 2.5V.

Determine the value of *VOH*. Assume that the PMOS transistor operates in triode region and

, Determine VoH also the value of *VOL*.

