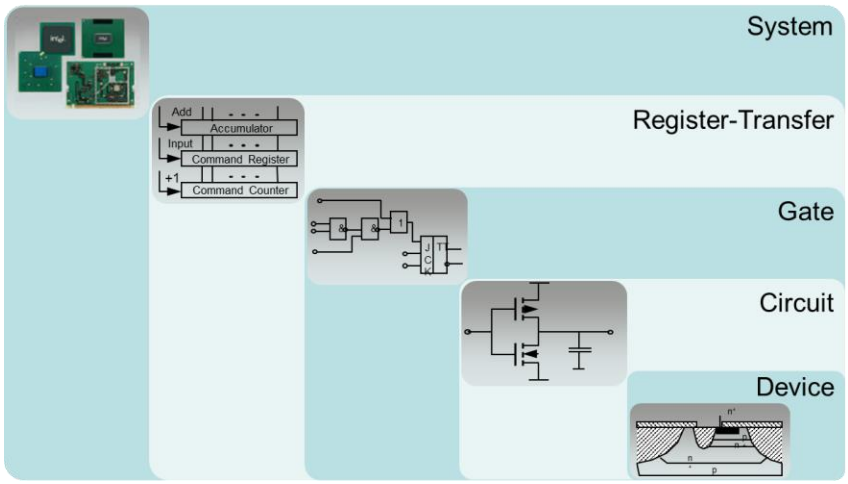
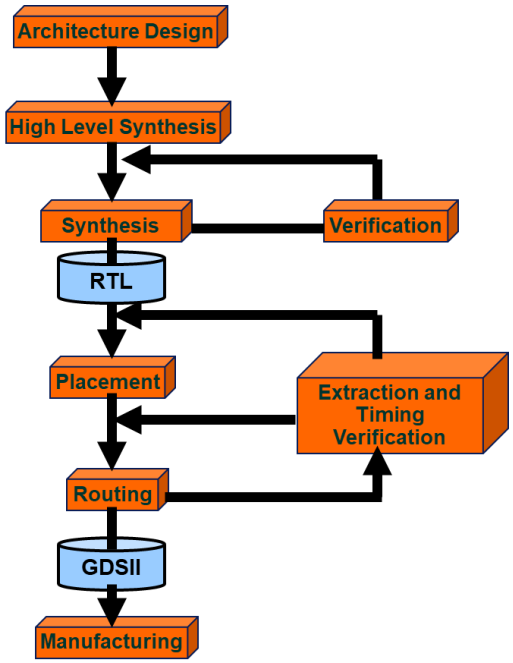
Question	Full Grade	Student Grade	ABET OUTCOME
1	30		
2	20		
3	16		
4	20		
5	30		

Question 1 (30)

1- Describe the flow of the design from specification to manufacturing **(10points)**



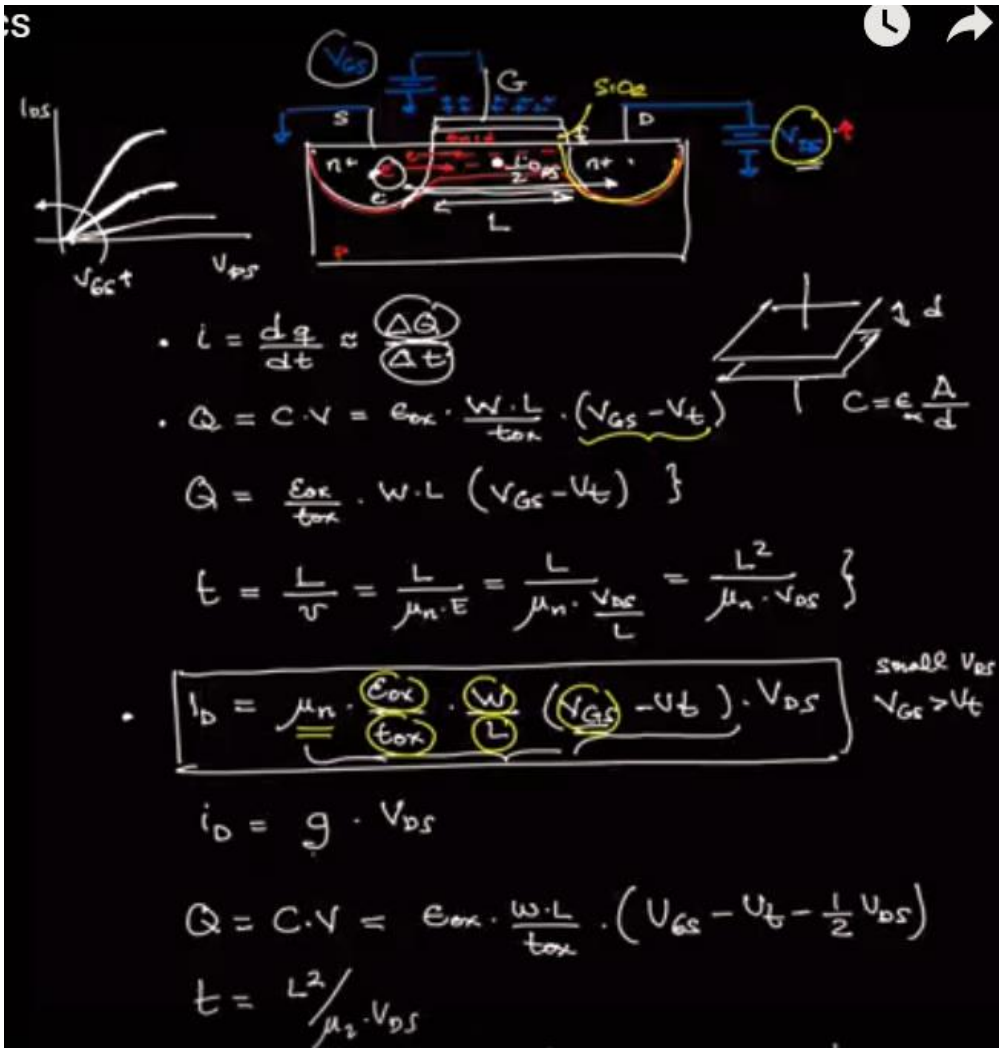
Or

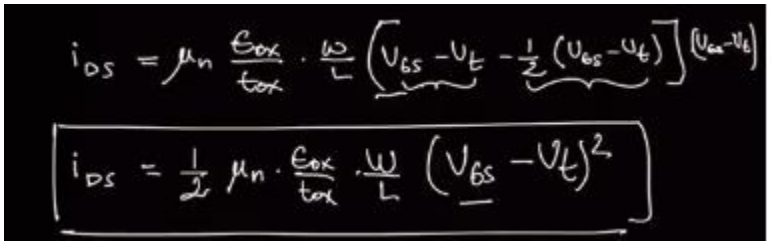


2- Derive the current equation for the NMOS transistor in linear region giving that : **(10 points)**

- Q=CV V=Vgs-Vt I=*dq/dt*

  From slides :

- 

- 

3- How do you differentiate between two designs in terms of performance? (5points)

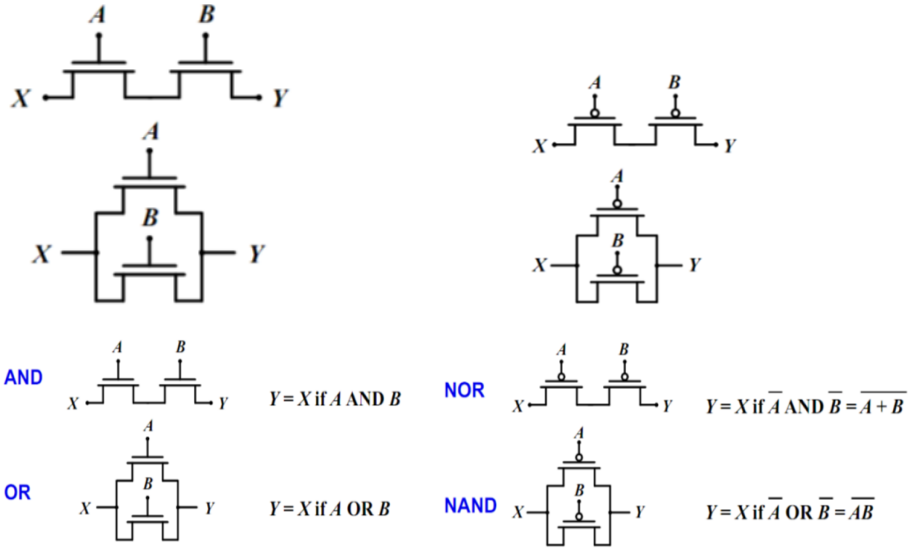
a. Area/Cost
b. Reliability
c. Scalability
d. Speed (delay, operating frequency)
e. Power dissipation
f. Energy to perform a function

2. *What are the main variables/parasitic that affects power dissipations* (5 points)

- ***Voltage? Increases***
- ***Leakage current , increase leakage power , V^2***
- ***Supply current , increase***
- ***Size of the load C_L? increases***
- ***Smaller devices ? less power***

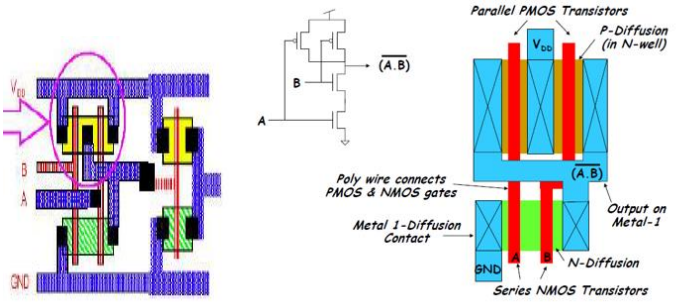
Question 2 (25)

1. *What type of logic function does these circuit do?* (5 points)

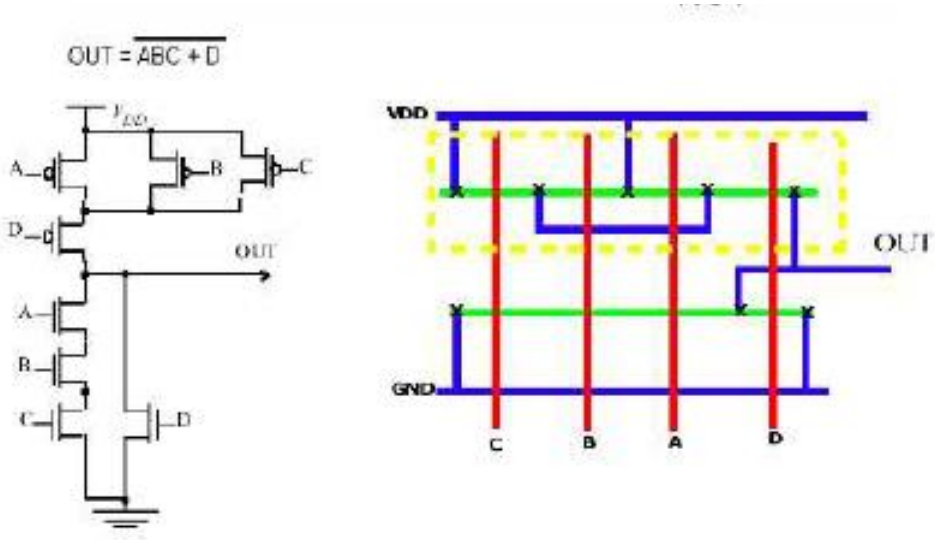


2. *Given the truth table below, (5 points)*

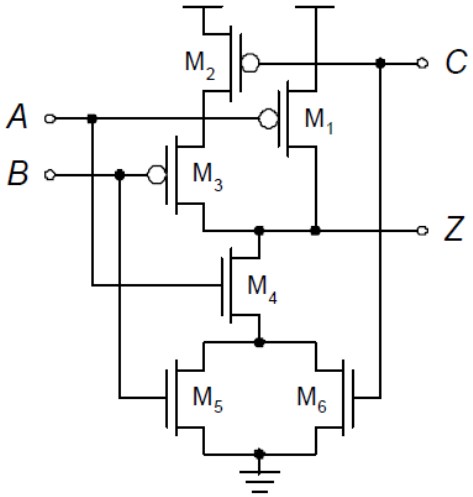
a. Draw stick digral/layout for 2-INPUT AND?



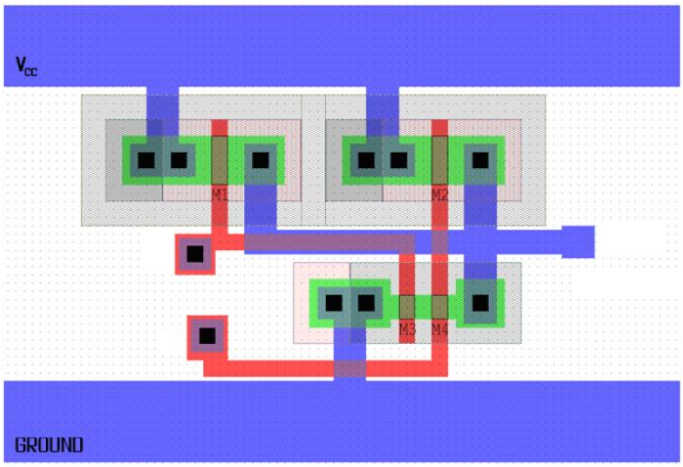
b. Draw stick diagram for Out= (ABC+D)' ***(5 points)***



c. Draw static implementation for F=(C+B).A (5 points)



1. Consider the following figure below, what type of logic gate is this? (5 points)



NAND2. The pull-up network has two PMOSFETs in parallel and the pull-down network has two NMOSFETs in series

Question 4 (24)

1- What is the output voltage of each of these devices: **(15 points)**

- If Vgd < Vt , channel pinches off near drain when Vds > Vdsat = Vgs – Vt

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} & \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{Saturation} \end{cases}$$

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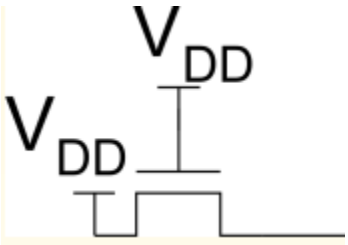
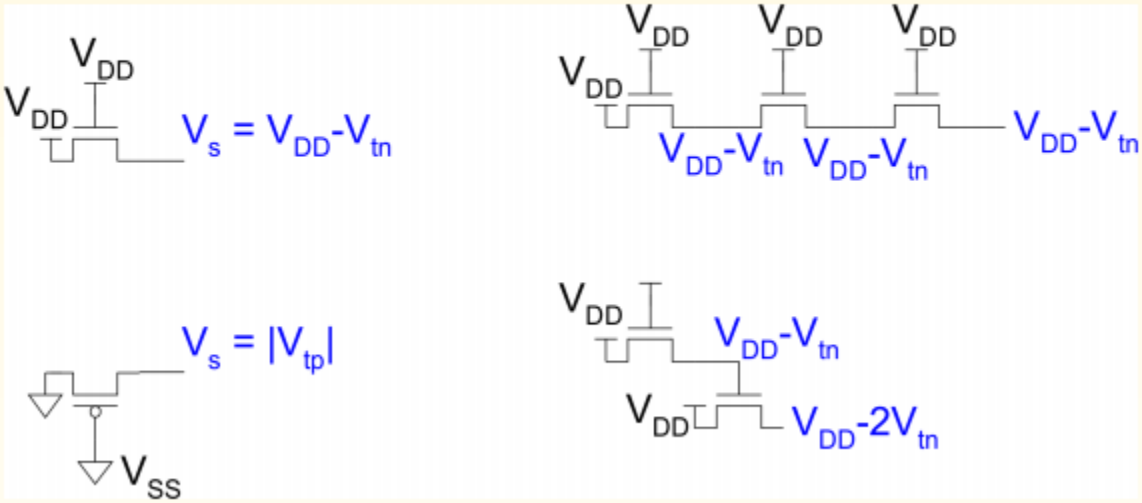
- Example, pass transistor passing VDD Vg = VDD If Vs > VDD − Vt, Vgs < Vt Hence, transistor would turn itself of

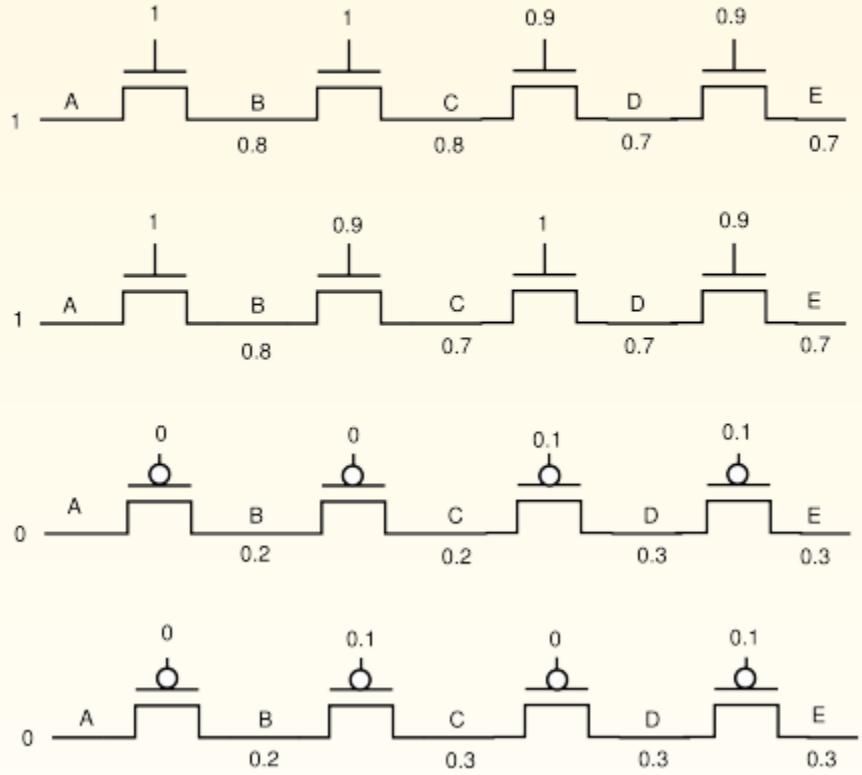


What would be the voltages on the different nodes?

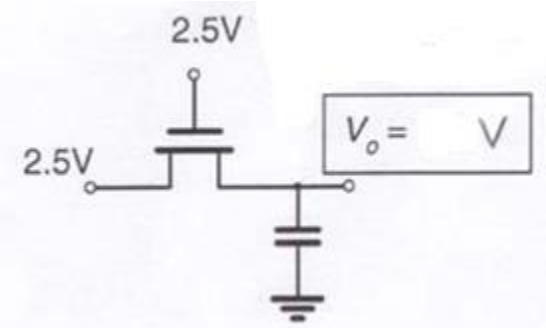


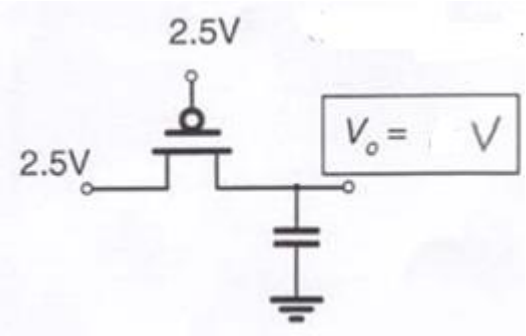
Assume: initial voltage of 0.5V on all the internal nodes

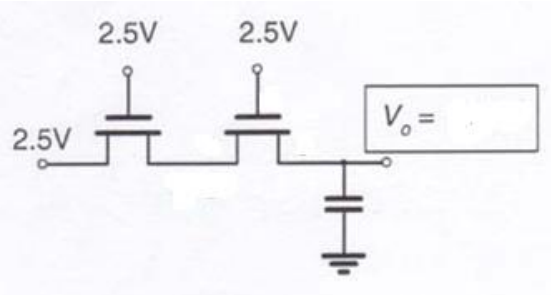
$V_{dd} = 1.0V$, $V_{t_n} = 0.2V$ and $|V_{t_p}| = 0.2V$

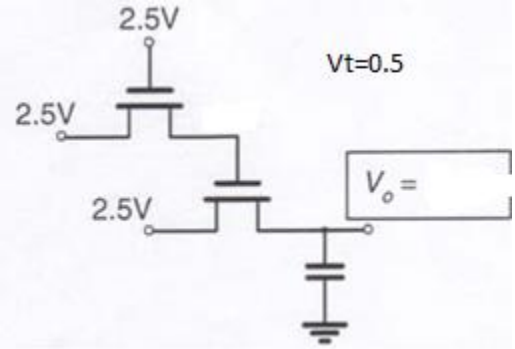


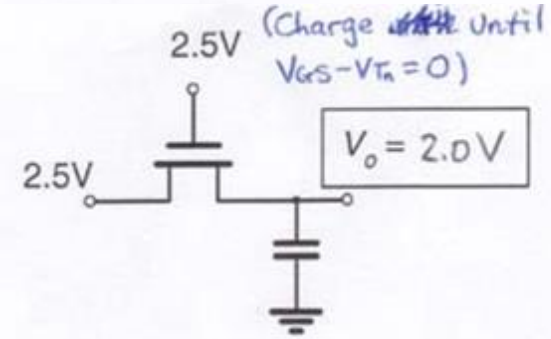
Extra thing just to understand … these we asked in previous exam

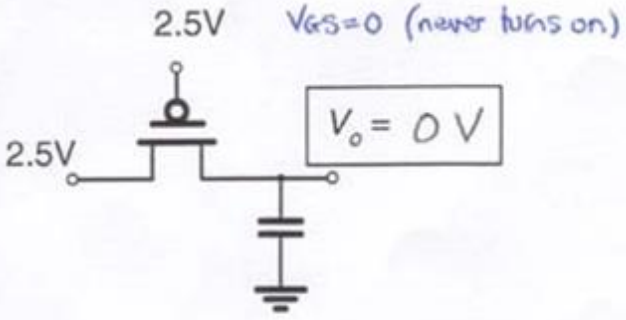

2.5V
2.5V
V_o = V

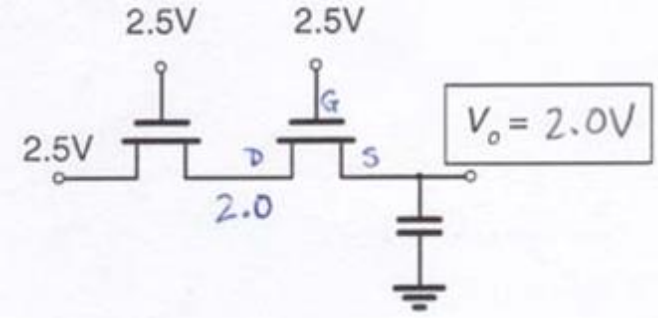

2.5V
2.5V
V_o = V

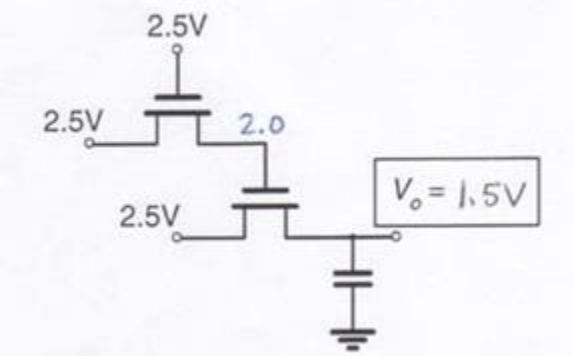

2.5V
2.5V
2.5V
V_o =


2.5V
Vt=0.5
2.5V
2.5V
V_o =


2.5V
(Charge until
$V_{GS}-V_{Tn}=0$)
2.5V
V_o = 2.0V

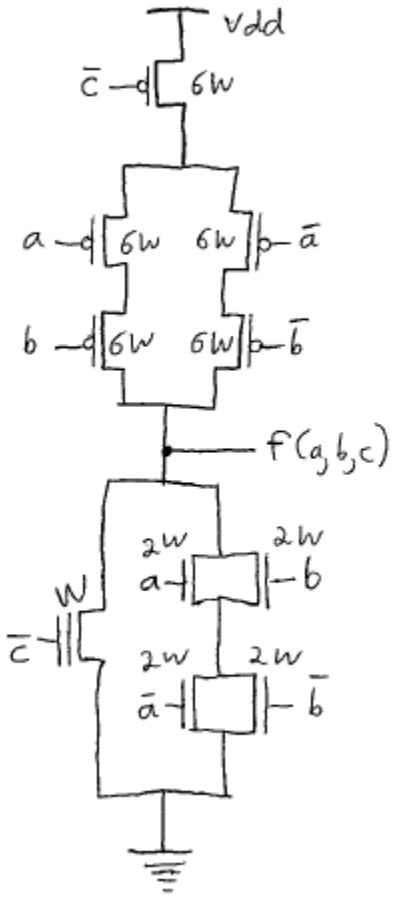

2.5V
$V_{GS}=0$ (never turns on)
2.5V
V_o = 0 V


2.5V
2.5V
G
2.5V
D
S
2.0
V_o = 2.0V



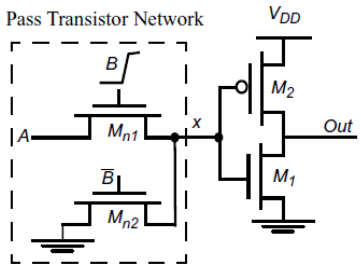
Question 4 (16)

A. a) Shown the circuit diagram for a static CMOS implementation what function it represent ? ***(4 points)***



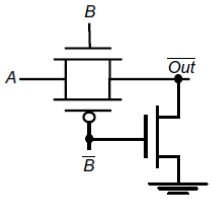
$$f(a,b,c) = (ab + \bar{a}\bar{b})c$$

B. What is the logic function performed by this circuit?**(3 points)**



The circuit is a NAND gate.

C. Implement the same circuit using transmission gates. (3 points) -AND GATE



D. In this problem, the circuits are implemented in 0.25um technology, and all the transistors have the minimum channel lengths.a. Consider the CMOS inverter from Fig. 2.a. If the NMOS transistor has channel width W_n and the PMOS transistor has channel width, W_p, label the voltage transfer characteristics from FIG. 2.b that correspond to following device sizes:(6 points)

A: $W_n = 5\mu m$, $W_p = 5\mu m$

B: $W_n = 1\mu m$, $W_p = 5\mu m$

C: $W_n = 5\mu m$, $W_p = 1\mu m$

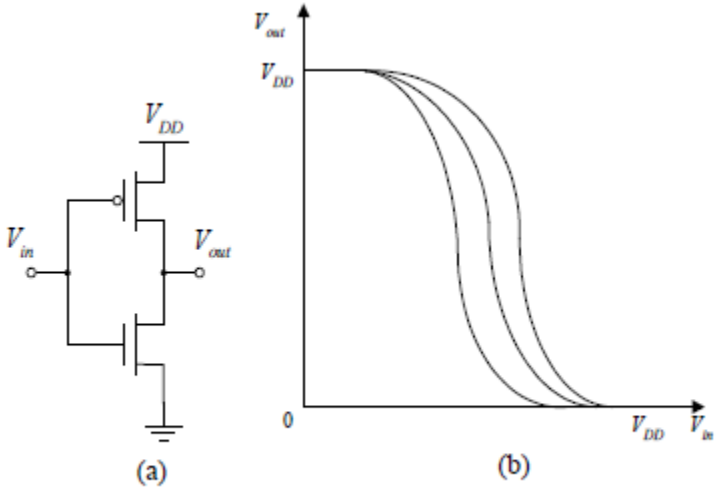
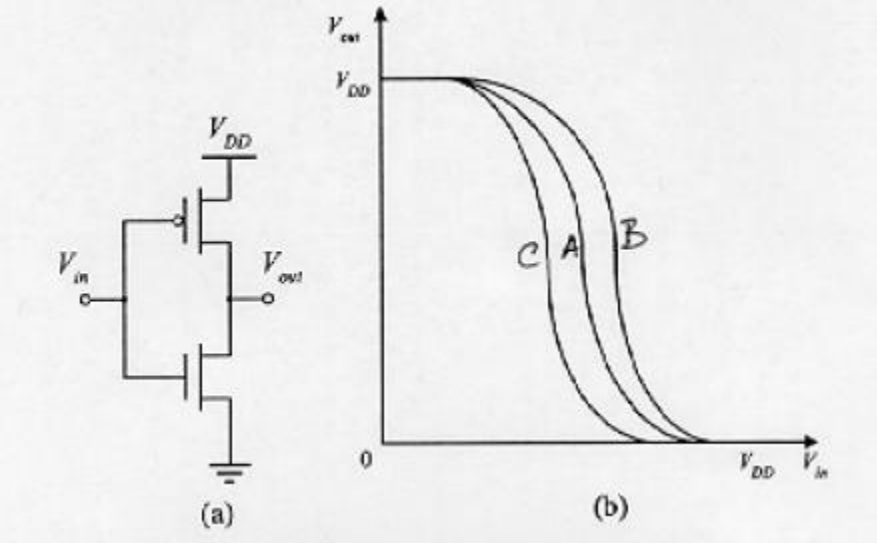


FIG. 2 CMOS inverter and Voltage Transfer Characteristics



NEED ALSO TO EXPLAIN RATION OF MOBILITY FOR N AND P