Question	Full Grade	Student Grade	ABET OUTCOME
1	10		
2	15		
3	12		
4	13		

Question 1: (10 POINTS)

1. CMOS stands for:

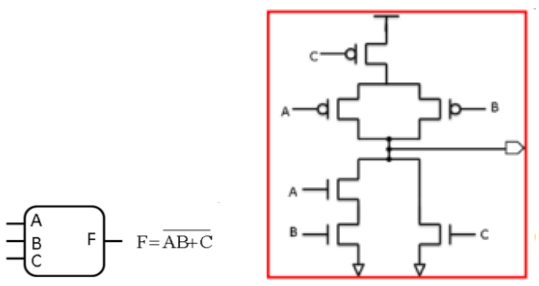
   A. complementary material oxide semiconductor
   B. complementary metal oxide semiconductor
   C. complex metal oxide semiconductor
   D. complex material oxide semiconductor

2. Chip Yield refers :
   A. Yield drops as chip area increases
   B. low yield means high cost
   C. Yield depends on process parameters
   D. All of the above
3. Which of the following metal layer has Maximum resistance?
   A. Metal1
   B. Metal2
   C. Metal3
   D. Metal4
4. How do you size NMOS and PMOS transistors to increase the threshold voltage?
   A. Increase voltage on gate
   B. Increase voltage on the bias(substrate)
   C. Lower drain voltage
   D. Lower drain current
5. What happens to delay if you increase load capacitance?
   A. Increase if driver size stay the same
   B. Decrease if driver size stay the same
   C. Has no effect if we make driver smaller
   D. Delay stay the same

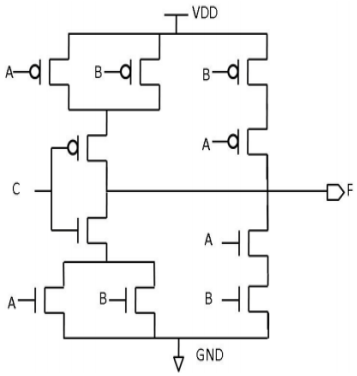
6. What are the limitations in increasing the voltage (power supply) to reduce delay?
   A. Delay limits: Increasing voltage increases delay
   B. Power limits: Increasing voltage will result in more power
   C. Area limits: increasing voltage will affect chip area significantly
   D. A and B
7. What happens if we increase the number of contacts or via from one metal layer to the next?
   A. Power dissipation decreased
   B. Increases resistance and power dissipation
   C. Overall resistance decrease
   D. A and C
8. What is the difference between LVS and DRC FOR LAYOUT?
   A. The layout must be drawn according to certain strict design rules DRC
   B. Both used in layout to verify delay
   C. None of the above
   D. LVS compares the netlist extracted from the layout with the schematic to ensure that the layout is an identical match to the cell schematic
   E. A and D
9. What are pros/cons of using low Vt, high Vt cells?
   A. low Vt cell violates design rules DRC
   B. high Vt cells affect delay of the cell so we should not use in speed path
   C. high Vt cells affect leakage power
   D. None of the above
   E. B and C
10. The main variables/parasitic that affects power dissipations
    A. low Vt cell violates design rules DRC
    B. high Vt cells affect delay of the cell so we should not use in speed path
    C. high Vt cells affect leakage power
    D. None of the above
    E. B and C

Question 4: (15 POINTS)

A. Implement the logic function F = $\overline{A \cdot B + C}$ by using a complex static CMOS Gate. Place the PMOS and NMOS driven by input A closest to the output node, F, in your transistor stacks. (3 points)



B. What is the logic function of the circuit shown below? Is this a static logic gate? Why or why not? (3 points)



Solution:

$$PDN = \overline{AB + C(B + A)}$$

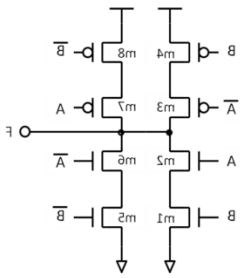
$$\left(PUN = \overline{AB} + \overline{C}(\overline{A} + \overline{B}) = \overline{A} + \overline{B} + \overline{C} + \overline{AB} = (A + B)C(AB) = \overline{AB + C(B + A)}\right)$$

$$F = \overline{AB + C(B + A)}$$
$$= \overline{AB + BC + CA}$$
$$= \overline{AB + C(B + A)}$$
$$= \overline{AB} + \overline{C}(\overline{A} + \overline{B})$$

$$F = \overline{AB + BC + CA} = \overline{AB + C(B + A)}$$

Yes. It is a static gate because the output is always connected to a low impedance path to VDD or GND.

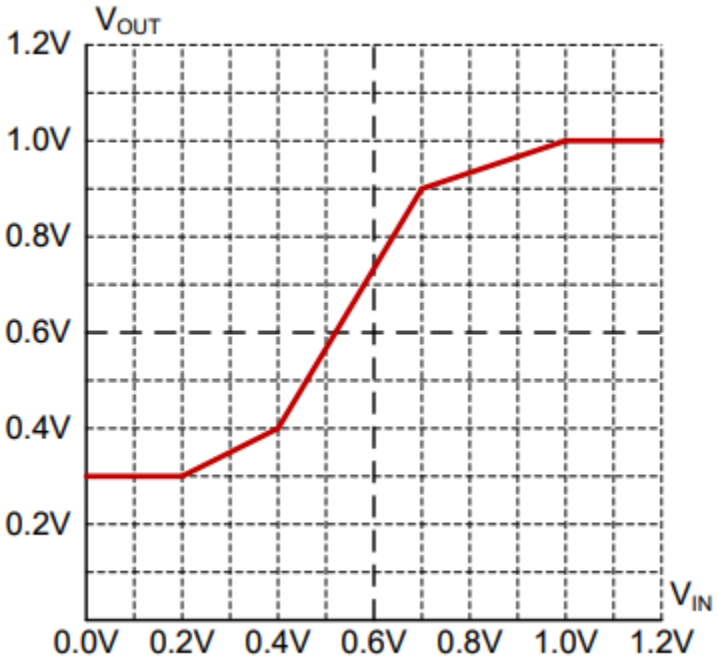
C. Draw the true table and determine the logic function of the complex gate shown below (3 points)



A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

This is an XOR gate

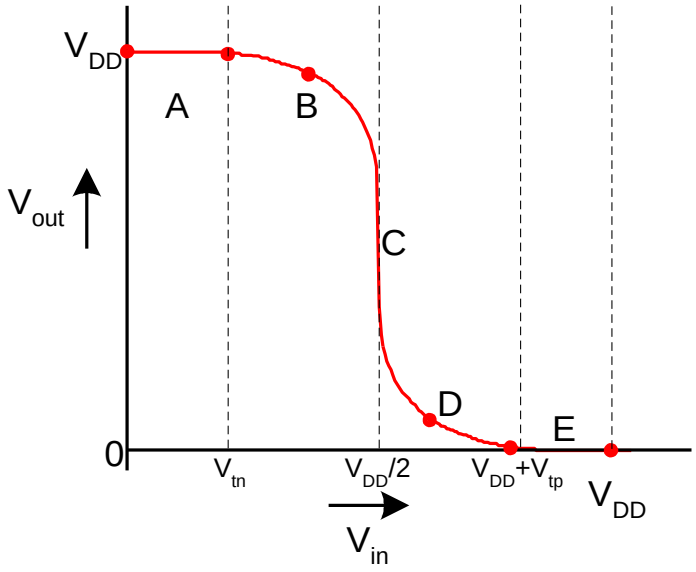
D. Simulation below is for Digital CMOS buffer VTC (3 points)



Compute V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, and NM_H.

(i) VIL = 0.4V (ii) VIH = 0.7V (iii)VOL = 0.3V (iv)VOH = 1.0V (v) NML = 0.1V (vi)NMH = 0.3V NML = VIL - VOL = 0.1V NMH = VOH - VIH = 0.3V

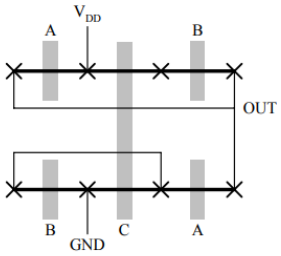
E. Transistor operating regions: Fill the table based on the figure below for each region (3 points)



Region	nMOS	pMOS
A	Cutoff	Linear
B	Saturation	Linear
C	Saturation	Saturation
D	Linear	Saturation
E	Linear	Cutoff

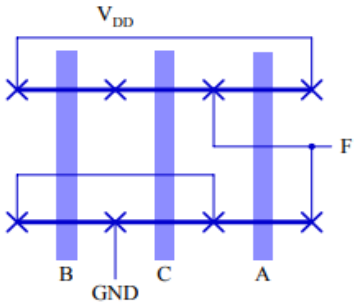
Question 3: (12 POINTS)

F. Write out the truth table that corresponds to the following stick diagram (3 Points)



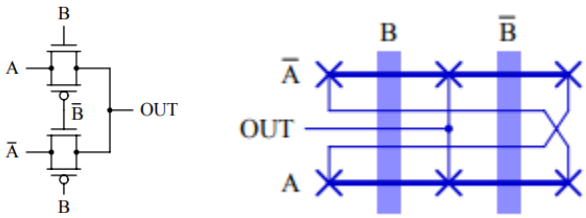
A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

A. Implement F = $\overline{AB+AC}$ using stick diagram. Each gate must be used for both PMOS and NMOS. Use static CMOS. Clearly denote if crossing wires are connected or not. **Use the fewest number of transistors possible**. (4 pts)



$F = \overline{A(B+C)}$

B. Implement the following circuit in stick diagram. Assume all inputs are given and do not break the diffusion. (4 pts)



Question 4: (13 POINTS)

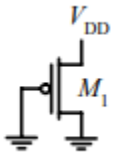
C. What is the effect of Increasing temperature on (4 Points)

A. Mobility → Reduces mobility
B. Vt → Reduces V_t

C. I_{ON} → **decrease**s with temperature
D. I_{OFF} → **increase**s with temperature

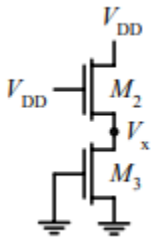
D. Determine the region of operation (Off, Linear, Saturation) in the following configurations. You may assume that all transistors are short-channel devices and have identical sizes, VDD = 2.5V. Assume following transistor parameters: Explain your reasoning and show your derivations if needed (6 Points)

NMOS: $V_{Tn} = 0.4V$, $k_n = 115\mu A/V^2$, $V_{DSATn} = 0.6V$, $\lambda = 0$, $\gamma = 0.4V^{1/2}$, $2\Phi_F = -0.6V$
PMOS: $V_{Tp} = -0.4V$, $kp = -30\mu A/V^2$, $V_{DSATp} = -1V$, $\lambda = 0$, $\gamma = -0.4V^{1/2}$, $2\Phi_F = 0.6V$



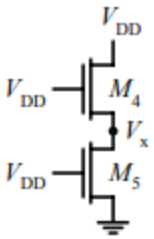
$V_{GS1} = V_{DS1} = -2.5V$

$|V_{DSAT1}| < |V_{GT1}| < |V_{DS1}| \Rightarrow$ **M_1 velocity saturation**



$V_{GS3} = 0 < V_{T3} \Rightarrow$ **M_3 off**

$V_x = V_{DD} - V_{T2} \Rightarrow$ **M_2 off**



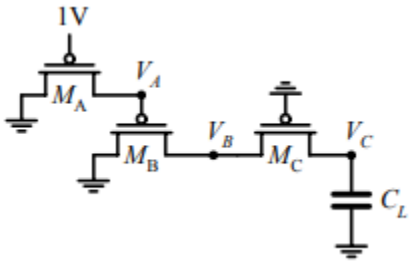
$V_{T4} > V_{T5}$ (body effect) $\Rightarrow V_{DS5} < V_{GT5} \Rightarrow$ **M_5 linear** (

Assume M_4 **vel sat** and ignore body effect in the first iteratio

$$(V_{DD} - V_{T4}) \cdot V_x - \frac{V_x^2}{2} = (V_{DD} - V_x - V_{T5}) \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}$$

$V_x = 0.435V \Rightarrow$ **M_4 velocity saturation** (

E. For the circuit in below determine the final value of VA, VB, VC, assuming initial condition at each of the nodes is 3V and VTP = −0.5V. (3 pts)



No current flows into the gate ⇒ IDA = 0 ⇒ VA = VGA – VTA = 1.5V

Since VA < initial VB, MB is also off ⇒ VB = VA – VTB = 2V

Finally, MC passes logic “1” to the output ⇒ VC = 2V