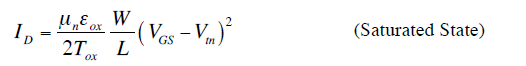
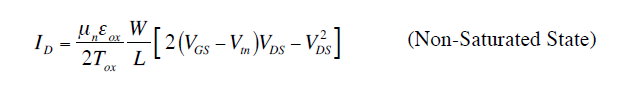
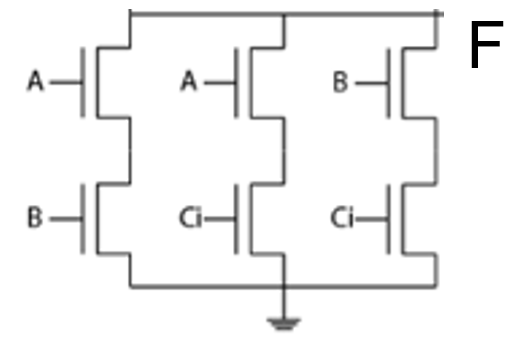
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| --- | --- | --- | --- |
| **Question** | **Full Grade** | **Student Grade** | **ABET OUTCOME** |
| **1** | **20** |  |  |
| **2** | **25** |  |  |
| **3** | **25** |  |  |
| **4** | **24** |  |  |
|  |  |  |  |



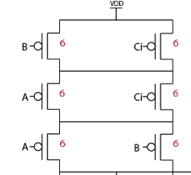


**Question 1 (20)**

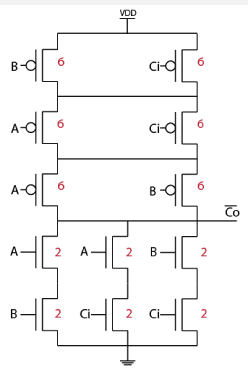
1. **Given pull-down network for function F :**



* 1. **What will be the pull-up Network?**

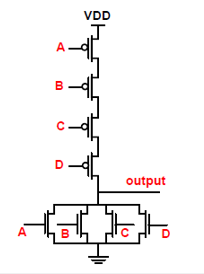
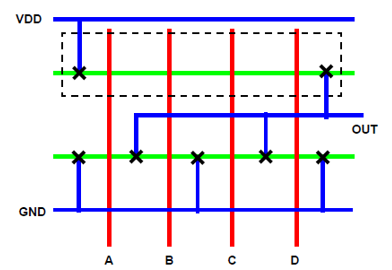


* 1. **What is the logic function from pull-up and pull-down network F =** 
  2. **What are the device sizes if it is going to match inverter with ratio of 2 for p and 1 for n (10 points)**

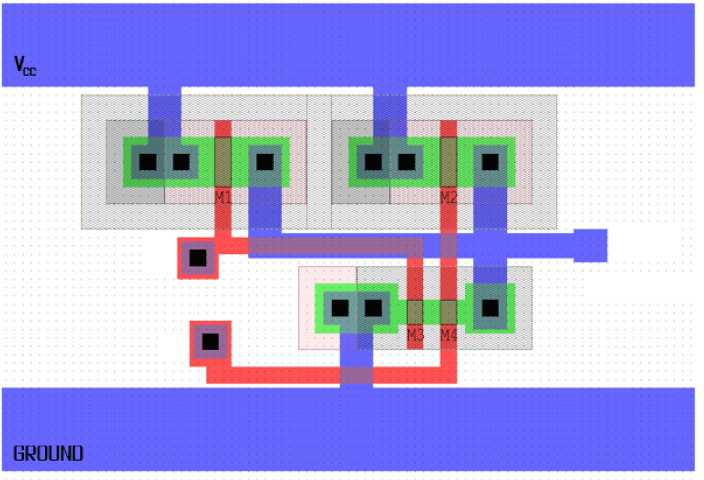


***Question 2 (25)***

1. Draw THE CIRCUIT that is represented by stick diagram below (5 points)



1. Consider the following figure below, what type of logic gate is this, draw transistor level? (5 points)



1. Design an inverter from schematic to layout , use the following assumptions and sequence

Assumptions: Process 25nm, Un/Up =2 **(15 points)**

1. Schematic ( transistor view) use P/N assumption **(2 points)**
2. Sketch Layout view of inverter including contact, taps ..etc ? **(4 points)**
3. DRC reports, List or describe things that DRC should have? **(2 points)**

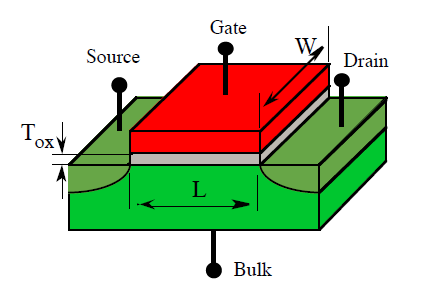
1. VTC (Voltage Transfer Characteristics), how does it look? **(3 points)**
2. 7. Waveforms of high-to-low and low-to-high propagation delays from both

Schematic and post layout simulation. Mark the delay values in the plots? (**2 points)**

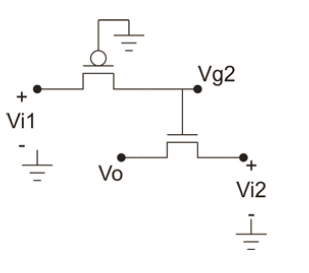
1. What will happen to the Propagation delay values if we change the process to smaller process (like 10Nm)? (2 points)

***Question 3 (25)***

* 1. Draw the PMOS cross section and label each part ( Drain, source, Gate, width, Length, Tox, bulk ) **(7 points)**



* 1. Using the rules given in lecture notes, find Vg2 and Vo required for both transistors to be ON in the two-transistor circuit shown below for each of the listed input voltage combinations. Assume VDD = 2.5V, Vtn = 0.5V, and |Vtp| = 0.5V. (6 points)



1. Vi1 = 0V, Vi2 = 0V

(b) Vi1 = 2V, Vi2 = 2V

*solution*

(a) Vi1 = 0V, Vi2 = 0V

Vi1-Vg1 = 0-0=0 < |Vtp|, so **Vg2** = Vg1+|Vtp| = 0+0.5 = **0.5V**

Vg2-Vi2 = 0.5-0 = 0.5V = Vtn, so **Vo** = Vi2 = **0V**

(b) Vi1 = 2V, Vi2 = 2V

Vi1-Vg1 = 2-0 =2 > |Vtp|, so **Vg2** = Vi1 = **2V**

Vg2-Vi2 = 2-2=0 < Vtn, so **Vo** = Vg2-Vtn = **2-0.5 = 1.5V**

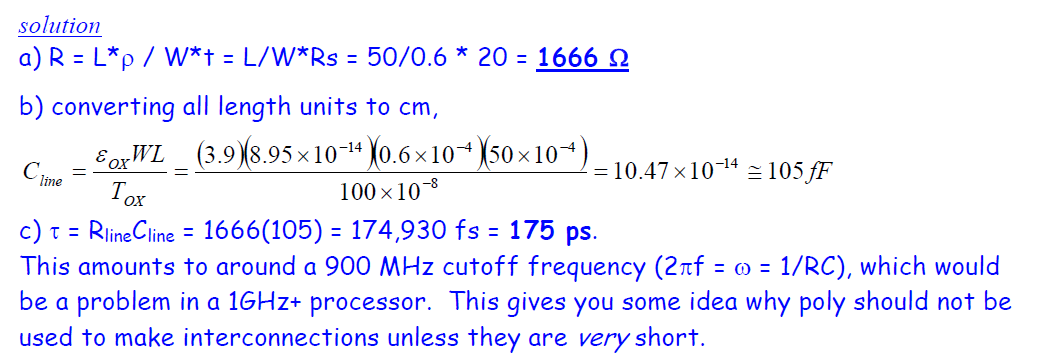
Vg2-Vi2 = 0.5-1 = -0.50V < Vtn, so **Vo** = Vg2-Vtn = 0.5-0.5= **0V**

* 1. A polysilicon trace that is 0.6μm wide, 0.05mm long, and 0.5μm thick has a sheet resistance of 20Ω. It is used to form a high frequency signal trace. (12 points)

a) Calculate the resistance of the poly trace. **(4 points)**

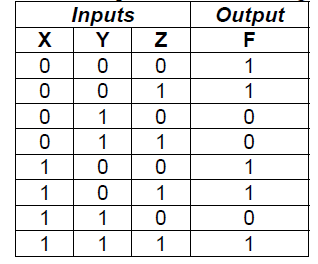
b) Calculate the line capacitance of this signal trace assuming the line is separated from a conducting plate by a 100Å thick oxide layer. Express your answer in fF (10-15) **(4 points)**

c) Calculate the time constant (RC-delay) associated with this trace. **(4 points)**



***Question 4 (35)***

1. A design has three input (XYZ ) and one out F, the output becomes One (1) only when X and Z are one or when Y equals zeor Draw the schematic for the CMOS circuit that implements the function F described (Hint) can start with the truth table. Use the least possible number of transistors. Explain your procedure to design the schematic. **(8 points)**



**solution (corrected)**

There are two basic approaches: we can construct a K-map or write a sum of products expression and reduce it. Let’s try the sum of products option.

We can write the sum of products for either the high terms (F) or the low terms (F’). Because there are fewer low/zero terms, let’s try those.

F’ = (X’YZ’ + X’YZ + XYZ’) = X’Y (Z’+Z) + XYZ’

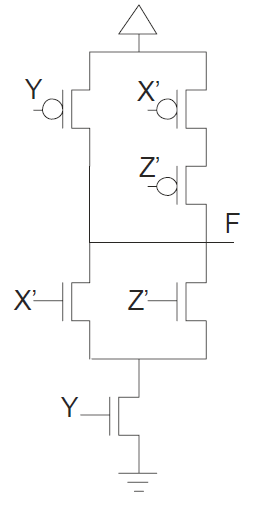
F’ = X’Y + XYZ’ = Y (X’+XZ’) 􀃆**F’ = Y (X’+Z’)**

Thus **F = Y’ + XZ**

Alternatively, by observation we can see that F = 1 when Y’ OR XYZ is true. Thus, F = Y’ + XYZ. Using the property covered in HW1 we can reduce this to

**F = Y’ +XZ**

which matches our sum of products results. Note that we should get the same results if we started with the high terms sum of products

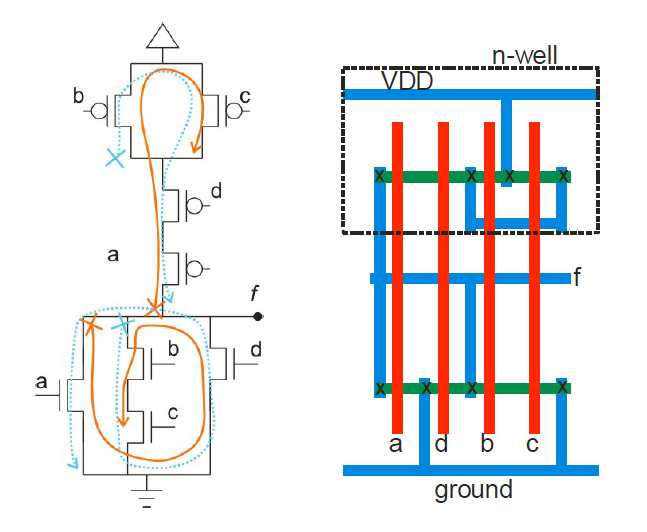


1. Sketch a color-coded stick diagram for the circuit that implements the function

***f =~( a+bc+d)***  Organize the layout so that the transistors can be implemented on a continuous strip of active (i.e., do not break the active**). (8 points)**

**solution:**

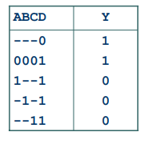
An interesting feature of this function is that you have to organize the transistors within the schematic correctly in order to achieve the ‘one continuous strip of active’ layout goals. The schematic below shows one possible implementation. Notice the b || c pMOS devices must be directly attached to either the ground or output nodes in order to draw a loop that does not violate the rules. Two possible loops (with X at the start and an arrow at the end) for this schematic implementation are shown (solid-orange line and dotted-blue line). The solid-orange loop is used to set the order of poly traces in the stick diagram below to a, d, b, c. However, there are many possible layouts for this function.



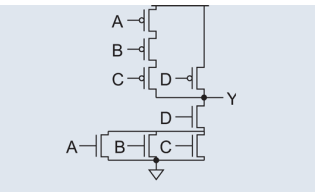
1. Shown the truth table for a static CMOS implementation below what

function it represent ? draw transistor level for the function ***(6 points)***

note - : means do not care .







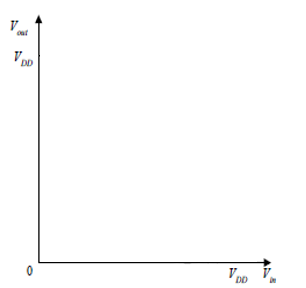
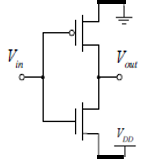
1. In this problem, the circuits are implemented in 0.25um technology, and all the transistors

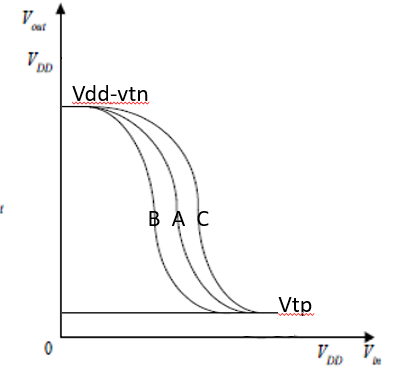
have the minimum channel lengths .a. Consider the CMOS circuit from Fig. 2.a. If the NMOS transistor has channel width *Wn* and the PMOS transistor has channel width, *Wp*, label and sketch the voltage transfer characteristics from FIG. 2.b that correspond to following device sizes assuming Vtn and Vtp are threshold voltages for n and p devices :**(8 points)**

A: *Wn* = 5m, *Wp* = 5m

B: *Wn* = 1m, *Wp* = 5m

C: *Wn* = 5m, *Wp* = 1m





1. What is the noise margin? Which design is better , having bigger noise margin or smaller noise margin (5points)