Question 1 (15)

1- Describe PMOS, NMOS Explain how they work? I am not looking for ON/OFF answers. A discussion of the Vgs.Id curve and region of operation should ensue. **(5points)**

```
If Vds = 0,
  Accumulation   Vgs << Vt
  Depletion      Vgs ~ Vt
  Inversion      Vgs > Vt

If Vds >0,
  Unsaturated    Vgs - Vt > Vds
  Saturation     Vgs - Vt < Vds
  Cutt-off       Current flow is essentially zero.
```

2- How do you evaluate performance of a digital circuit, please name at least three? (3 points)

a. Area/Cost
b. Reliability
c. Scalability
d. Speed (delay, operating frequency)
e. Power dissipation
f. Energy to perform a function

2. ***Yield & Defects : What is the yield and how do we calculated ?*** **(2 points)**

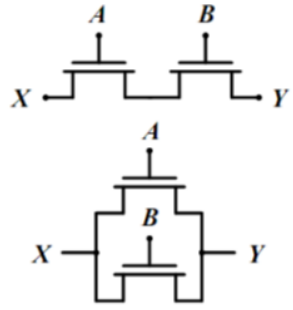
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

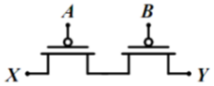
3. What are the three types of power? **(5 points)**

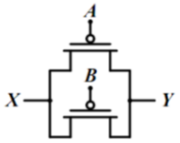
- ***p(t) = v(t)i(t) = Vsupplyi(t)***
- ***Peak power:***
- ***Ppeak = Vsupplyipeak***
- ***Average power:***
- $$P_{ave} = \frac{1}{T}\int_t^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_t^{t+T} i_{supply}(t)dt$$

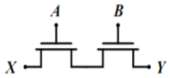
Question 2 (25)

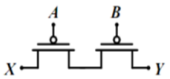
1. ***What type of logic function does these circuit do?*** **(12 points)**

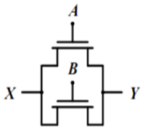


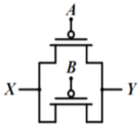




AND  $Y = X$ if A AND B

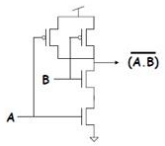
NOR  $Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$

OR  $Y = X$ if A OR B

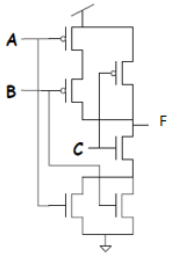
NAND  $Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

2. ***Given the truth table below, (8 points)***
   - ***1- Draw the CMOS circuit in transistor level***
   - ***2- Draw the layout stick diagram***

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0



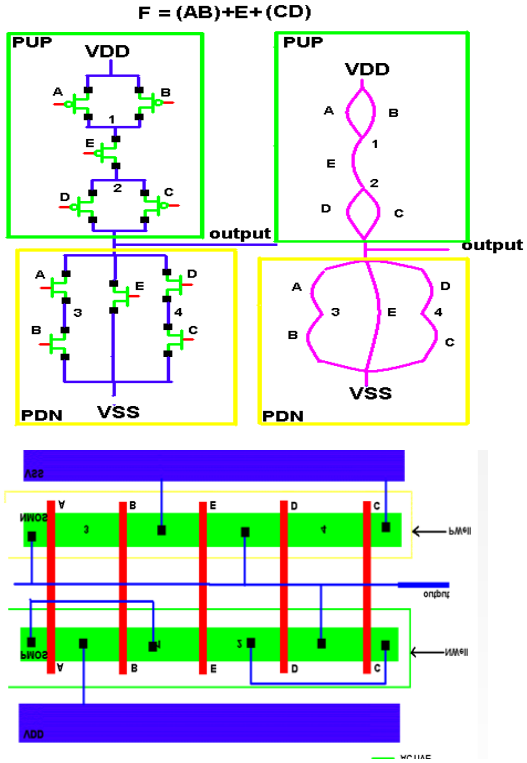
   - ***3- Given a complex gate as shown below, what the function of the circuit?*** **(5 points)**



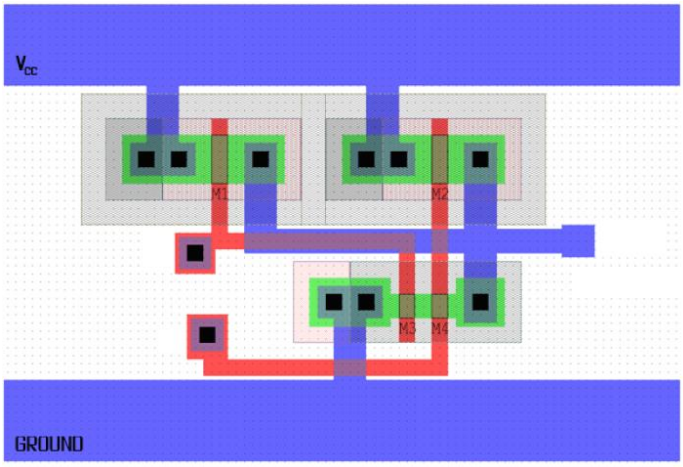
F=((A+B).C}'

Question 4 (25)

1. ***Draw the CMOS transistor level for this complex Gate and draw the stick diagram for it F=E+(AB)+CD(15 points)***



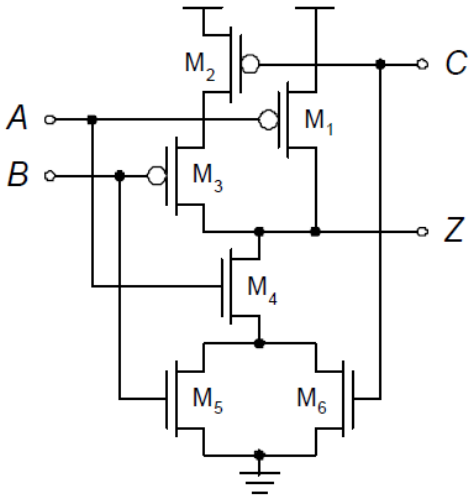
2. ***Consider the following figure below, what type of logic gate is this? Do you think the designer balance the rise and fall time? (10 points)***

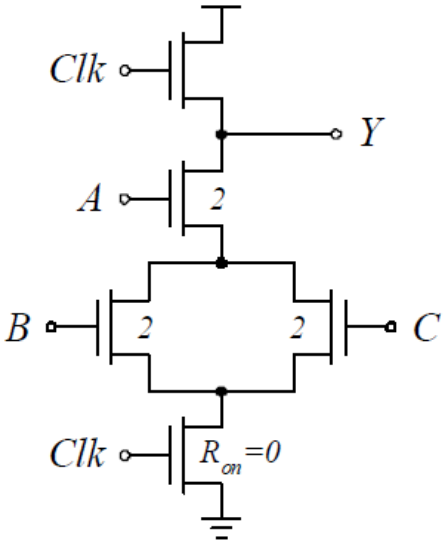


NAND2. The pull-up network has two PMOSFETs in parallel and the pull-down network has two NMOSFETs in series. Interestingly, we can see that the designer didn't balance t_{phl} and t_{plh}.

Question 4 (25)

Draw static and dynamic implementation for F=(C+B).A **(10 points)**



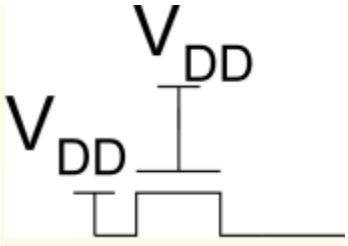


4- What is the output voltage of each of these devices: **(15 points)**

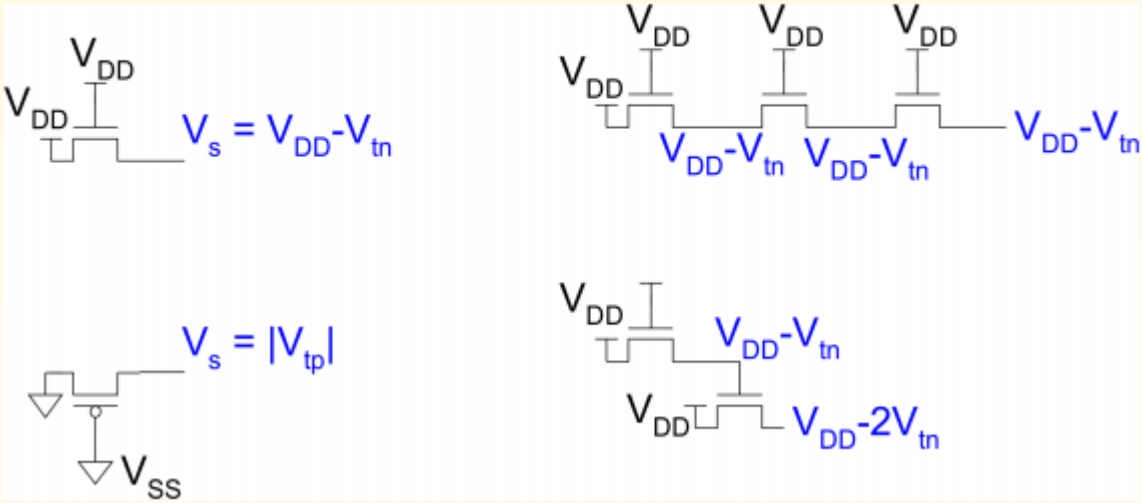
- If Vgd < Vt , channel pinches off near drain when Vds > Vdsat = Vgs – Vt

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ \beta\,(V_{gs} - V_t - V_{ds}/2)\,V_{ds} & V_{ds} < V_{dsat} & \text{Linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{Saturation} \end{cases}$$

-
- Example, pass transistor passing VDD Vg = VDD If Vs > VDD − Vt, Vgs < Vt Hence, transistor would turn itself of

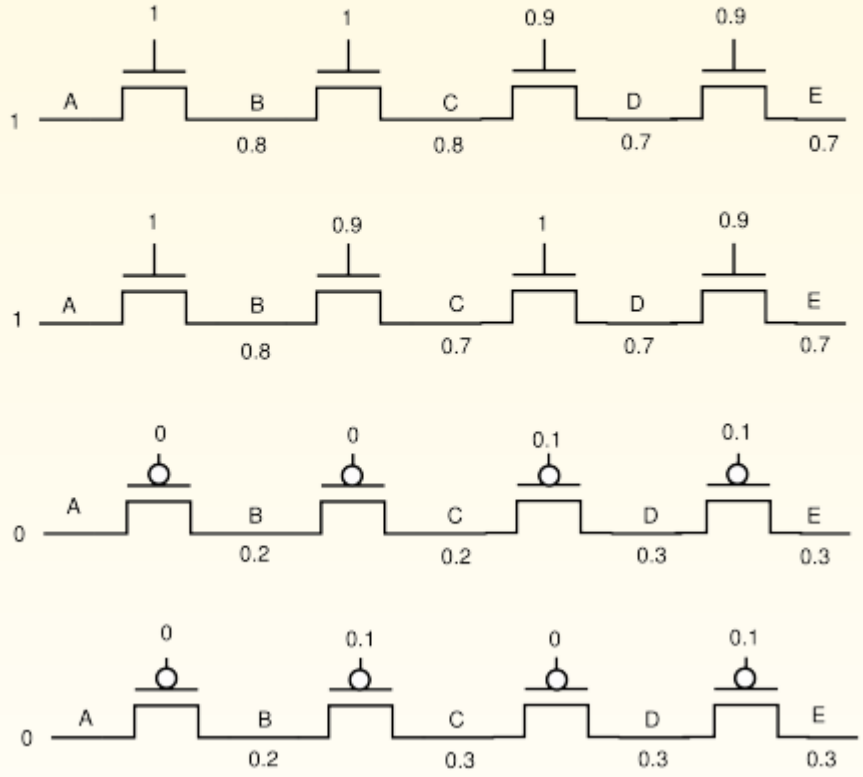


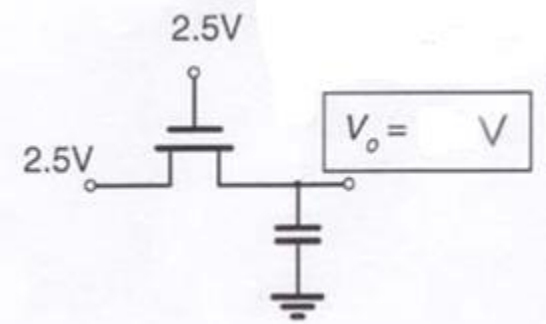
What would be the voltages on the different nodes?

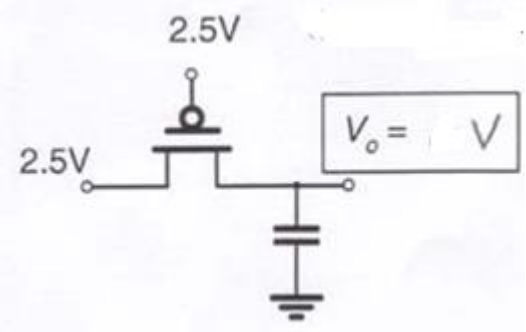


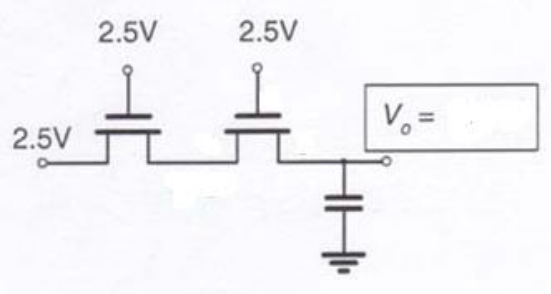
Assume: initial voltage of 0.5V on all the internal nodes

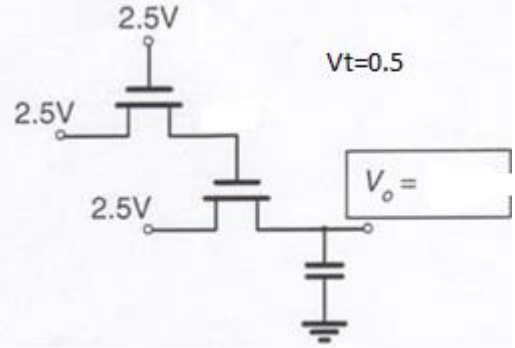
$V_{dd} = 1.0V$, $V_{t_n} = 0.2V$ and $|V_{t_p}| = 0.2V$

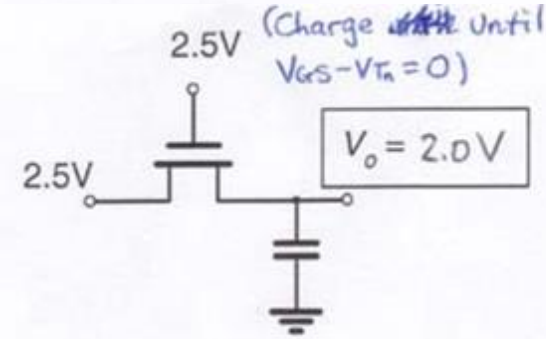


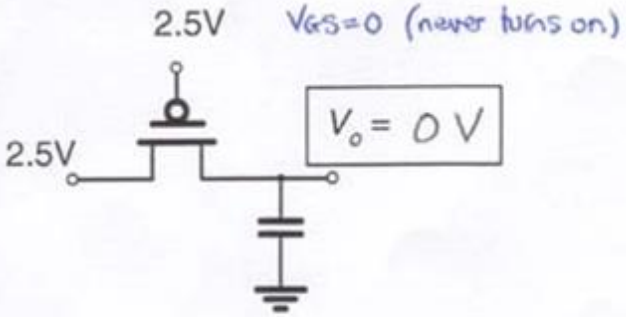

2.5V
2.5V
V_o = V

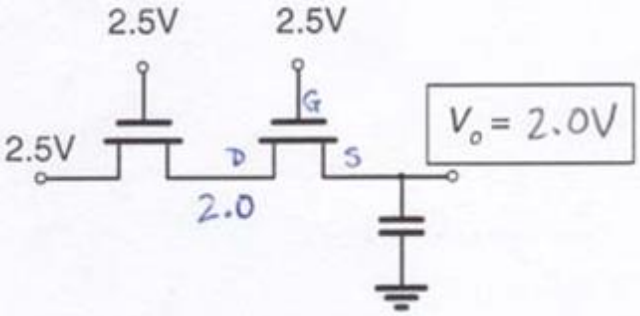

2.5V
2.5V
V_o = V

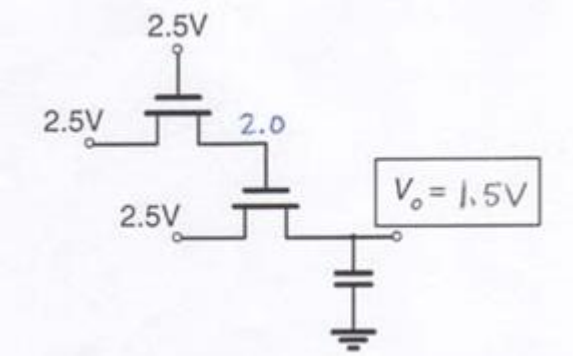

2.5V
2.5V
2.5V
V_o =


2.5V
Vt=0.5
2.5V
2.5V
V_o =


2.5V
(Charge until $V_{GS}-V_{Tn}=0$)
2.5V
V_o = 2.0V

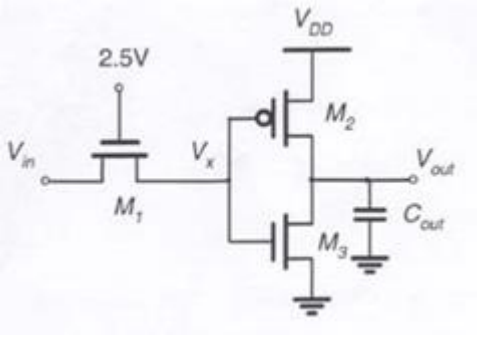

2.5V
$V_{GS}=0$ (never turns on)
2.5V
V_o = 0 V


2.5V
2.5V
G
2.5V
D
S
2.0
V_o = 2.0V



Question 4 (10)

Consider a three trainsitor circuit as shown in figure below. Vdd=2.5V and input signal switch between 0 and Vdd with sharp rise and fall times. All transistor are minimum length l=0.25UM, trainsestor width W2=2um, W1=1um. Note: ignore body effect. Find M3 transistor width such that the switching point of the inverter (Vm) is placed in the middle of Vx signal swing **(10 points)**



$V_{IN} = 2.5V \rightarrow V_{XH} = 2.5 - 0.4 = 2.1V$

$V_{IN} = 0 \rightarrow V_{XL} = 0V$

$$V_m = \frac{V_{XH} - V_{XL}}{2} = 1.05V$$

At $V_{out} = V_m$, $V_{DS} = -1.45V$ for PMOS M_2 and $V_{DS} = 1.05V$ for NMOS M_3, which means both M2 and M3 are velocity Saturated ($V_{DSATP} = -1$, $V_{DSATn} = 0.6$).

We know for the inverter $I_{M2} = I_{M3}$, so we can solve for the width of M3 using the velocity saturated current equations.

$$\frac{I_{DS3}}{I_{SD2}} = \frac{W_n k_n' V_{DSATn}\left(V_m - V_{tn} - \frac{V_{DSATn}}{2}\right)}{W_p k_p' V_{DSATP}\left((V_{DD} - V_m) + V_{tp} + \frac{V_{DSATP}}{2}\right)} = 1$$

$$\frac{W_p}{W_n} = \frac{k_n' V_{DSATn}\left(V_m - V_{tn} - \frac{V_{DSATn}}{2}\right)}{k_p' V_{DSATP}\left((V_{DD} - V_m) - V_{tp} - \frac{V_{DSATP}}{2}\right)} = 1.46 ; \quad W_n = \frac{W_2}{1.46} \simeq 1.37\,\mu m$$