Chapter - 6-Structures For Discrete-Time Systoms

* Difference equation, Inpulse Response (hon) and system Function (H(2)) an equivelant characterization of Input-output relation of LTI system.

* For Implementing LTI system characterized by diff. equation or System Function by discrete-time analogue or digital Hondwan => Diff. eg. or system function must be converted to an algorithm or structure that can be realized.

x In this chapter - system, can be represented by 5 tructures consisting of an Interconnection of the basic operations of Daddition D Multiplication by a constant and I delay.

e-g.

H(Z) = 1 - a Z / 1 > 1 = 1

h(n) = bo à u(m + b) à u(n-1)

y(n) = ay(n-1) = box(n) + b1x(n-1) (x)

7 Since this system has an infinite-duration impulse response, it is not possible to implement the system by discrete convolution.

Howevere, re-writing (ok) in form

y(n) = ay(n-1) + b0 ×(n) + b1×(n-1)

provides the basis for an algorithm for recursive computation of the august at any time (n) in terms of previous output yen-v g current input sample. zeln), and previous input sample occin-1).

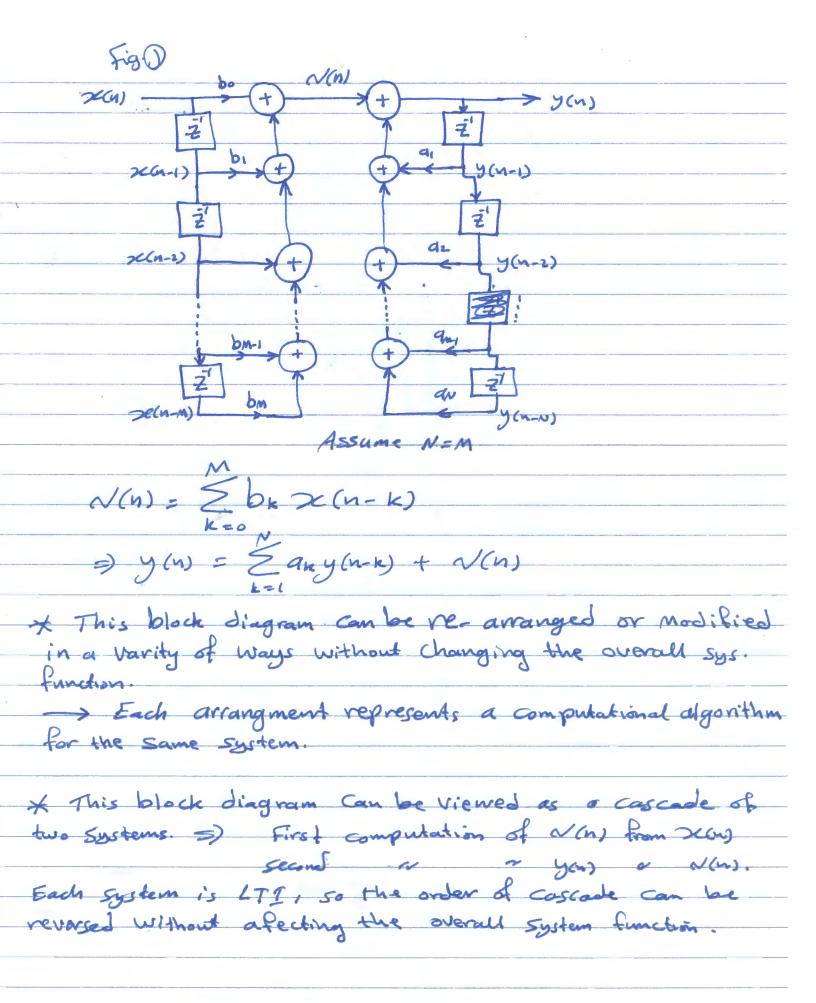
(If we assume initial reset condition, (i.e. x(n) = 0 for n(0), then y(N=0 Fr nco).

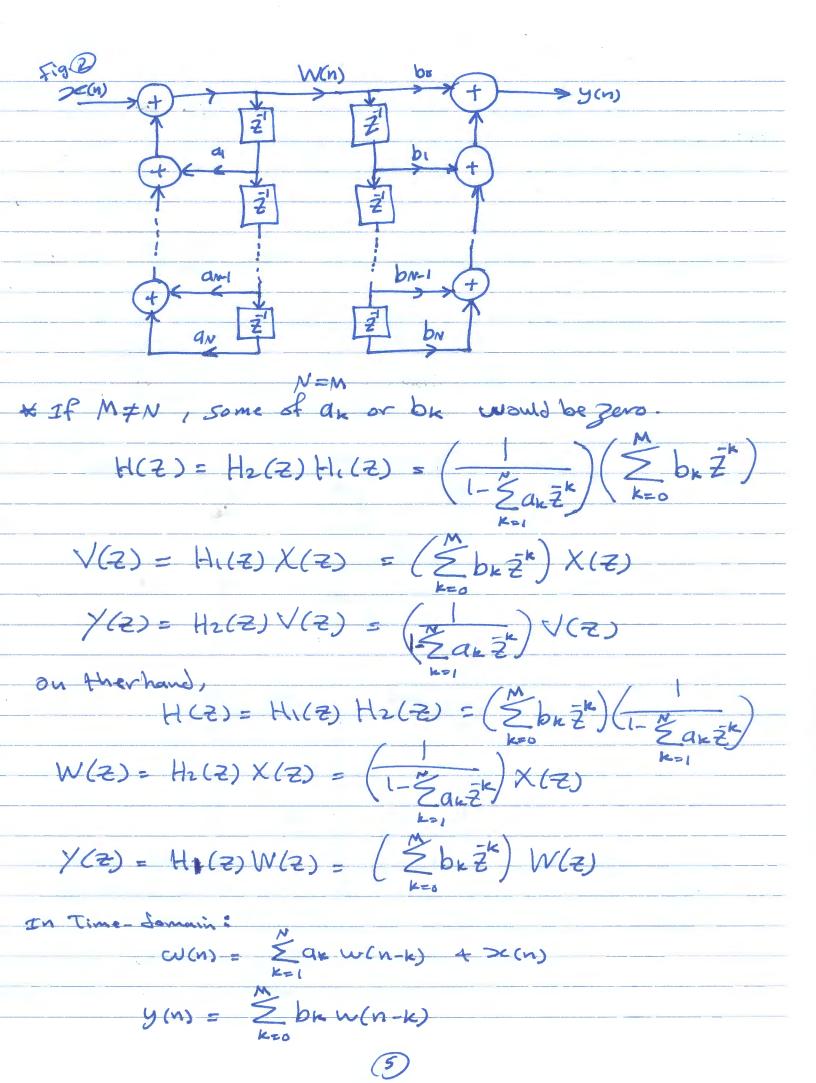
* Similar procedure con le applied to more general cose of an NHA order difference equation.

* However, this algorithm is not the only computational algorithm and it is not the most preferable one.
Implementation of LTI systems
Block diagram representation of LCCDE for Implementation:
Multiplication of delayed sop. Values by the Coefficients.
So, the basic elements for implementing LTI system are a
Multiplication of delayed sq. Values by the Coefficients. Addition for adding the resulting product. So, the basic elements for implementing LTI system are of 122(n) **Adders 2(n) + > ×(n) + ×2(n) (But we use only two in the course). **Multiplies (he a combant) 2(n) 9 - 126(n)
The first Cay a section of the secti
* Memory for Storing delayed seg. Values.
$z(n) \rightarrow z(n-1)$
* In digital implementation, delay operation can be implemented by storage Register for each Unit delay. (or Shift-Register).
X In analogue discrete - time Implementation, delay unit is a Charge Strage device.
+ Delay of more than one sample (M samples) can be done by coscading M unit delays. In IC- implementation, these unit delays are a Shift-Reg. clocked at sampling rate of input signal.
* In Software Implementation of M Cascades unit Jelays can be Implemented as M consecutive memory registers.

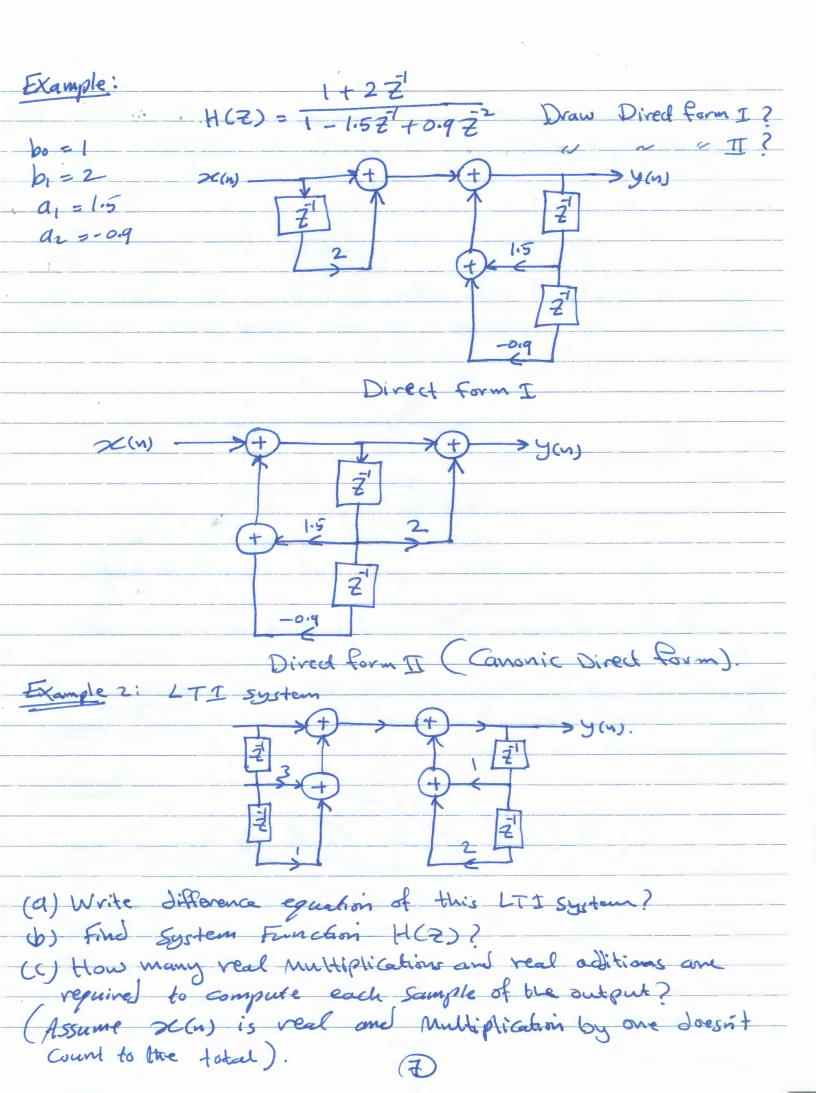
Example: 2nd order Sift. 9. y(n) = a, y(n-1) + az y(n-z) + box(n) * Implementing system on general purpose Computer or DSP Chip.

this network structure is the basis for the program that Implement this System => What we need for this Implementation * Storage for delayed samples (y(n-1), y(n-2)) × Multiply of y(n-1) and azyon-z) and adding them * ADD the result to be se(n) * This Example can be generalized Into higher order diff. og. $y(n) - \begin{cases} \begin{cases} a_k y(n-k) \\ k = 0 \end{cases} \end{cases} = \begin{cases} \begin{cases} b_k x(n-k) \\ k = 0 \end{cases}$ y(n) = Zaxy(n-k) & Zbx x(n-k)

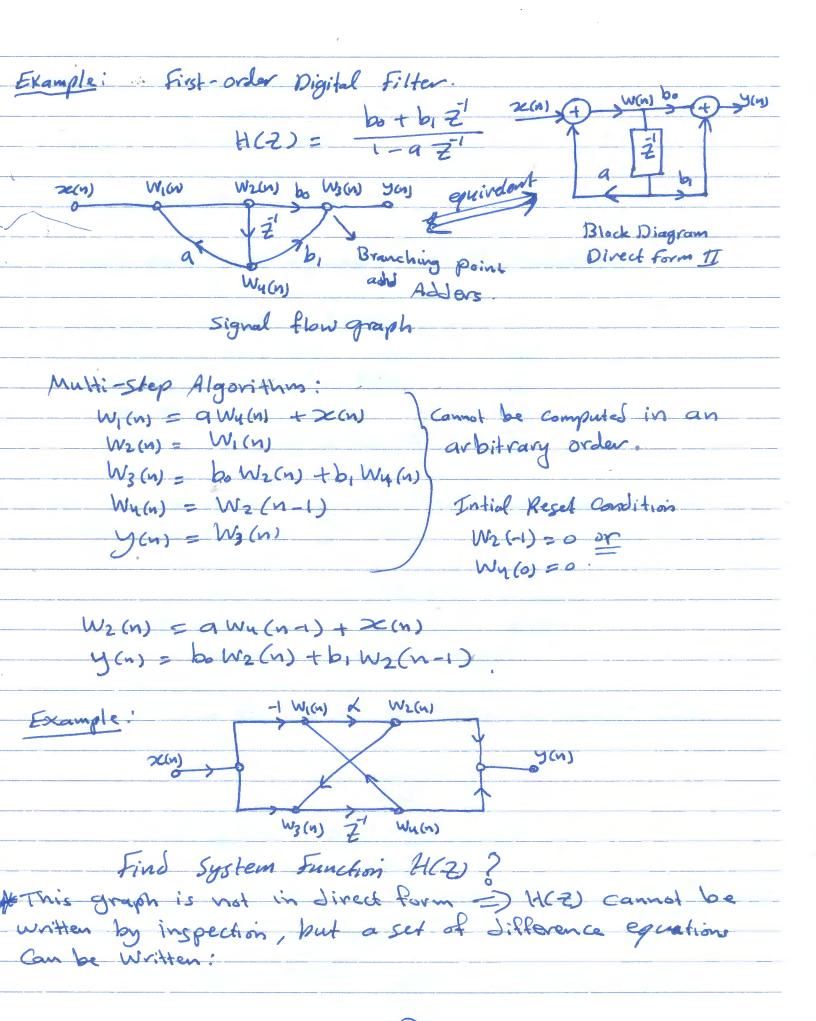




* Differences between Fig and Fig 2 o 1- In the first block diagram (figD), zeros of H(Z) [the (H1(Z))) are implemented first followed by the Poles (H(2)). 2. In Fig. 2 poles are Implemented first, then zerois. (N+M). Fig 3 * No. of delay elements is less than in Fig D => Minimum Number of delay Units is max (N.M). => This Implementation (with min no. of delays) is called =) Canonic form. or Direct Form I & Block diagram in Fig. D is called Direct form I.

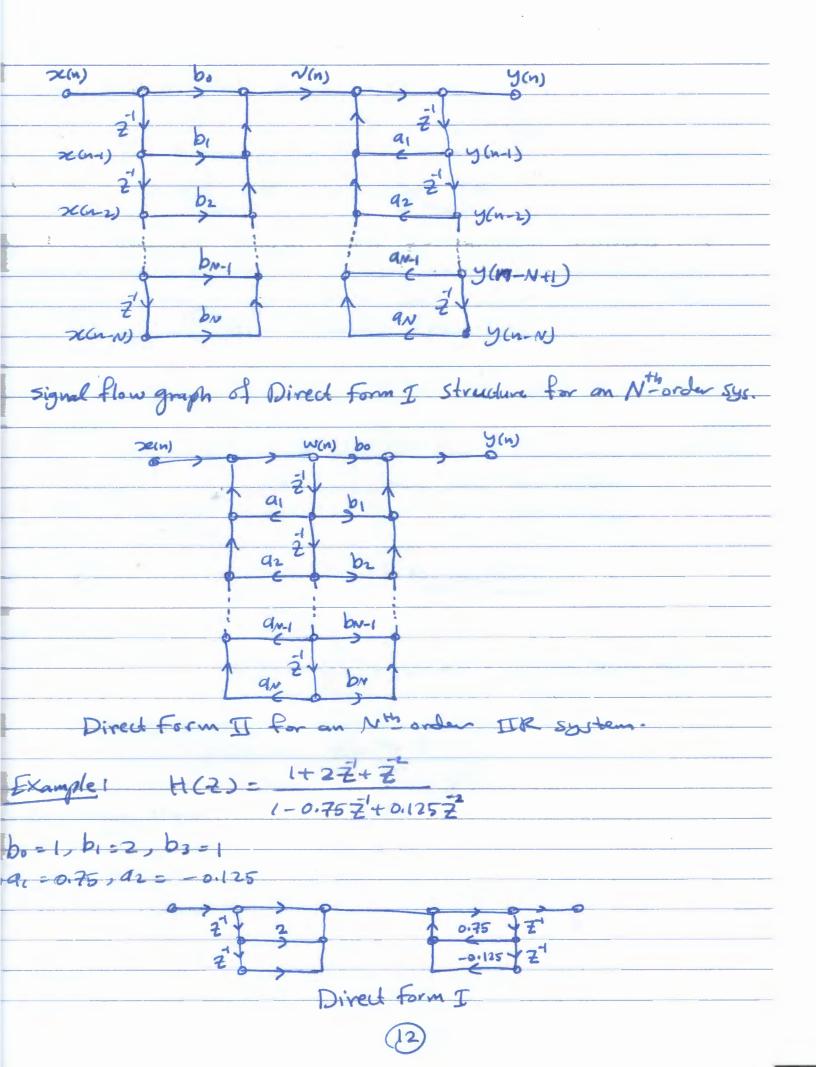


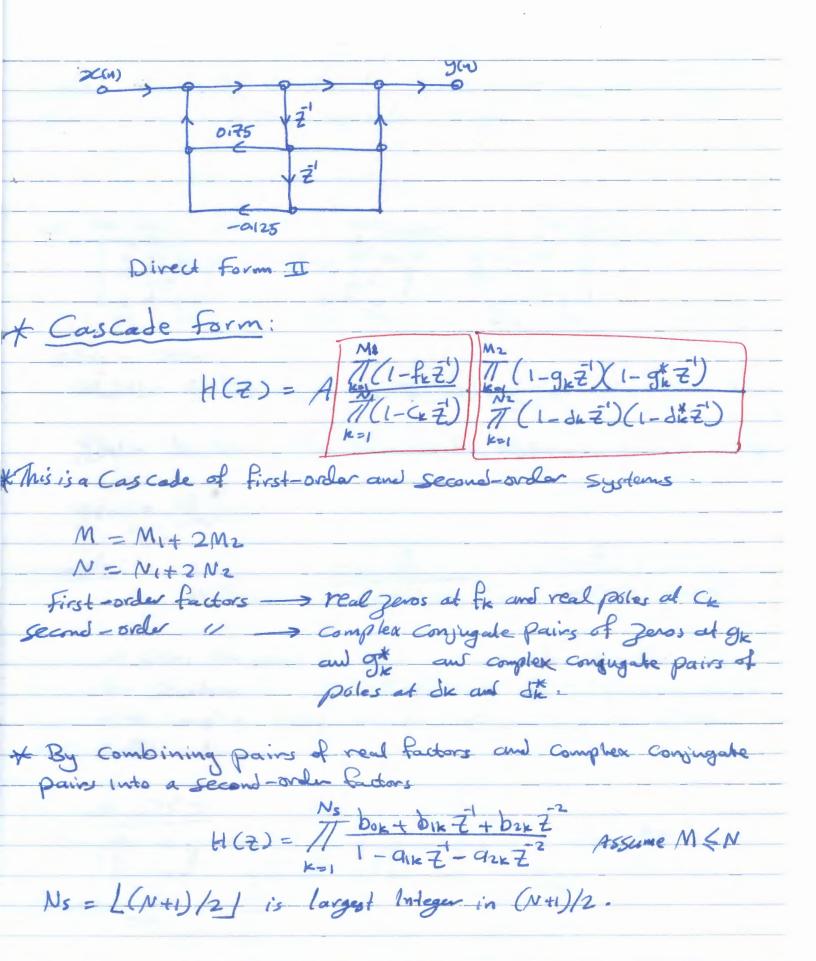
Is it possible to reduce no of storage Registers? If so, draw M. Stricture.
Signal Flow Graph
is a network of directed branches that connect at nodes. Associated with each node is a variable or node value.
W; (n) > Q Wk (n) Modek Y each Branch has input and out (nt.
* Input to branch (j,k) is Wj(n) * Output of Branch = in put * Constant or (1).
* The value at each mode = { Support of all Branches entering the mode.
Source Node: No entering Bromches (used for source signal) Sink Nodes! have only entering bromches (Extract output from graph)
Example: Source 2000) Willing Walns Jons Walns Jons
$W_{1}(n) = 2C(n) + q W_{2}(n) + b W_{2}(n)$ $W_{2}(n) = CW_{1}(n)$ $W_{2}(n) = d \times (n) + c W_{2}(n)$ $W_{2}(n) = -3$
Addition , Multiplication by a constant, delay of required for linear systems.
8 Systems.

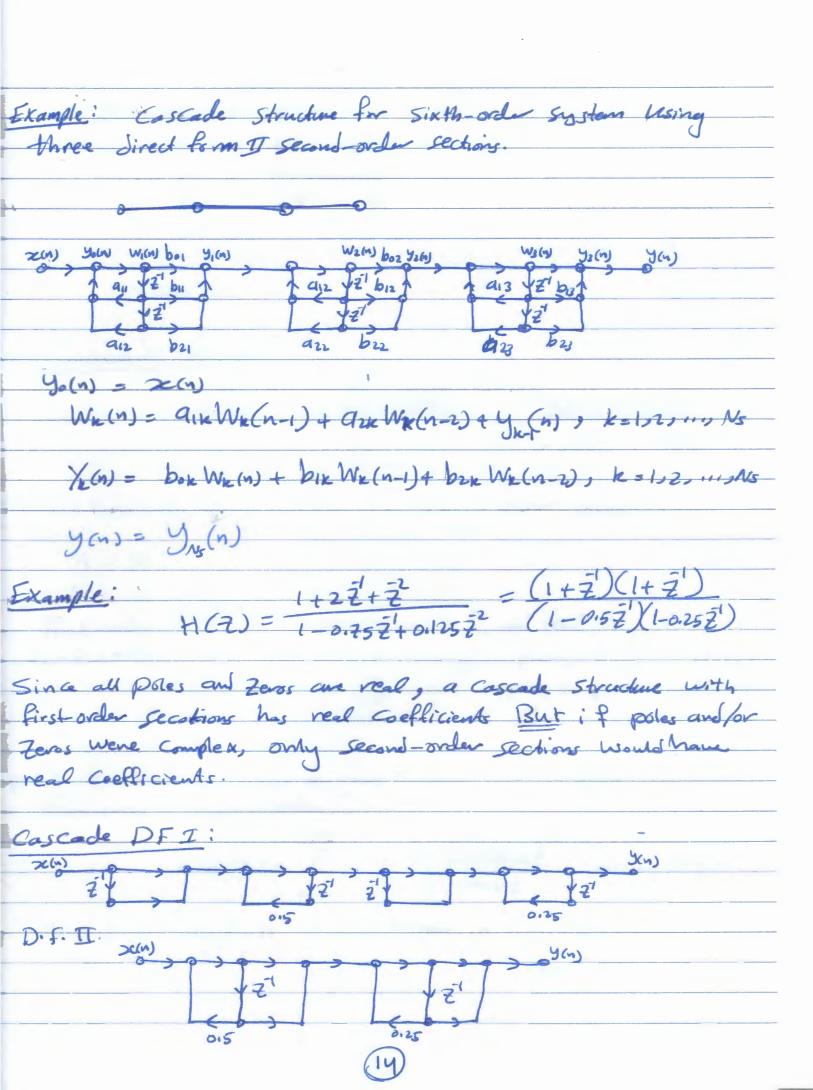


W,(n) = Wy(n) - >e(n) W2(n) = KW1(n) W3 (m) = W2(n) + >C(n) Wie (n) = W3 (n-1) y(n) = W2(n) + Wu(n). * convert these diff. equations Into Z-transform: W1(2) = W4(2) - X(2) - @ W3(2) = W2(2) + X(2) --- @ W4(2) = 7/W3(2) - - - -Y(2) = W2(2) + W4/2 --- @ * We can eleminate W1(2) and W3(Z) by substituting @ W2(2) = x (W4/2) - X(2)) $W_{4}(2) = \overline{2}'(W_{2}(2) + X(2))$ $Y(2) = W_{2}(2) + W_{4}(2)$ Can be solved for W2(Z) and W4(Z) => $W_2(z) = \frac{\chi(\overline{z}'-1)}{1-\chi\overline{z}'}\chi(\overline{z})$ Wy(2) = Z(1-K) X(2) H(7)= = = x=1 => h(n)= x u(n-1) - x u(n)

Direct form I Flow graph is &
X: This example shows how Z-transform Converts the
time-domain expressions, which Involves feedback and thus are difficult to Solve, Into linear equations that can be solved by algebraic techniques.
* By Comparing the original graph with direct form I graph. (mem) Original -> Requires one Multiplication and one delay Direct form I -> Two Multiplication and one delay N 1 II -> N 1 4 One delay.
6.3 Basic Structures for IIR Systems!
Assuming N=M.







Parallel Formi H(Z) = SCKZ+ SAK SBK(1-EKZ)

+ (Z) = L=1 - CKZ + SBK(1-EKZ)

- K=1 - CKZ + SC(1-dKZ)(1-dKZ) M7, N => Np = MN, Otherwise first N = N1+2N2 . II If ak and Sum is not included. to Parallel combination of first and second-order IIR systems with possibly NP scaled delay Paths. * Alternativity, we may group real pairs poles in pairs. =) $H(2) = \sum_{k=0}^{N_{p}} \frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} - \frac{1}{2} + \frac{1}{2} \right)$ $N_{s} = \frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} \right) \left(\frac{1}{2} + \frac{1}{2} \right)$ $N_{s} = \frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} \right) \left(\frac{1}{2} + \frac{1}{2} \right)$ $N_{s} = \frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} \right) \left(\frac{1}{2} + \frac{1}{2} \right)$ $N_{s} = \frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} \right) \left(\frac{1}{2} + \frac{1}{2} \right)$ $N_{s} = \frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} \right) \left(\frac{1}{2} + \frac{1}{2} \right)$ $N_{s} = \frac{1}{2} \left(\frac{1}{2} + \frac{1}{2} \right) \left(\frac{1}{2} + \frac{1}{2} \right)$ $N_{s} = \frac{1}{2} \left$ Sum disapear negative, First Example: N=M=6 913 PE 1 21/19

Example: ... parallel realization by executing H(2) as $H(2) = 8 + \frac{18}{1 - 0.25 \frac{7}{2}} - \frac{25}{1 - 0.25 \frac{7}{2}}$ Parallel Form Structure Using First-order

Feedback in IIR systems: Feedback loops: closed paths begin at node and return to that node only in the direction of arrows (implies node Variable depends directly or Indirectly y(n) = ay(n-1) + > e(n) $\chi(n)$ $\chi(n)$ $\chi(n)$ $\chi(n)$ * If x(n) = S(n), then the single sample continually circulates in the feedback loop with either Increasing (lat >1) or Jecreasing (lat <1) amplitude => h(n) = a"u(n). This is the way that Feedback loop can create an infinitely long impulse response. Herefore, longest delay between Input and Dutput occur for path that Passes through all delay elements in the => For Networks with no loops => H(Z) has only Zero's (except for poles at Z=0) and # of Zeros no more than # of Jelay elements.

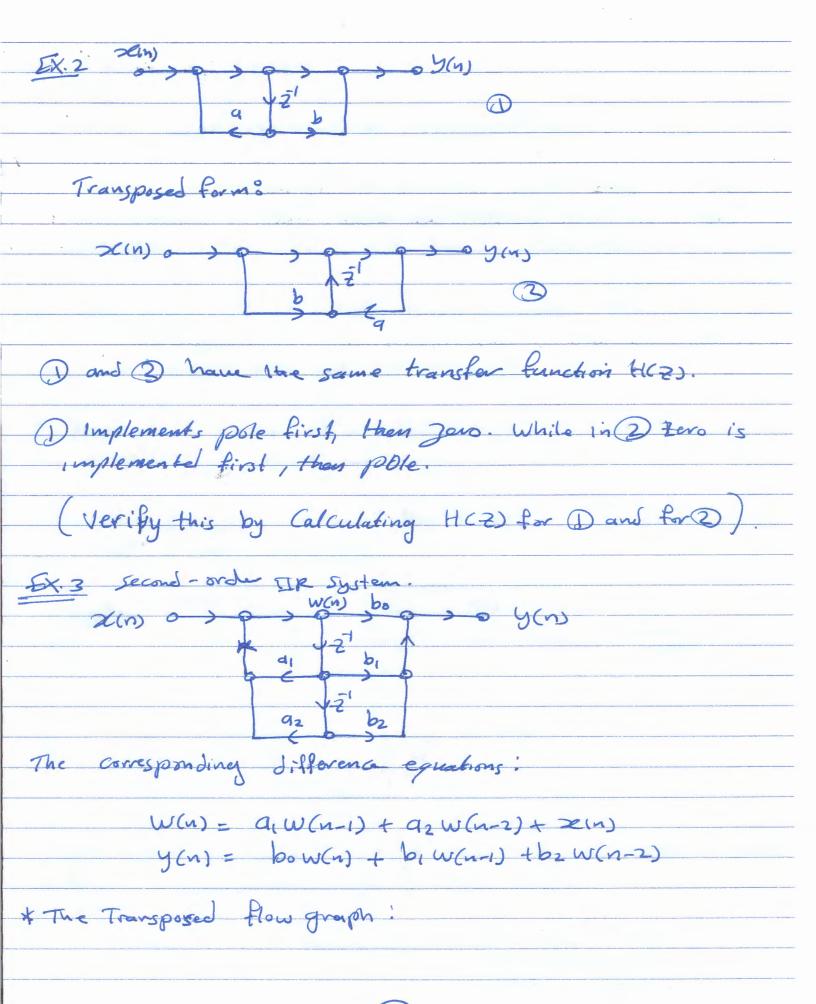
* IF H(Z) has poles => Network will have Feedback

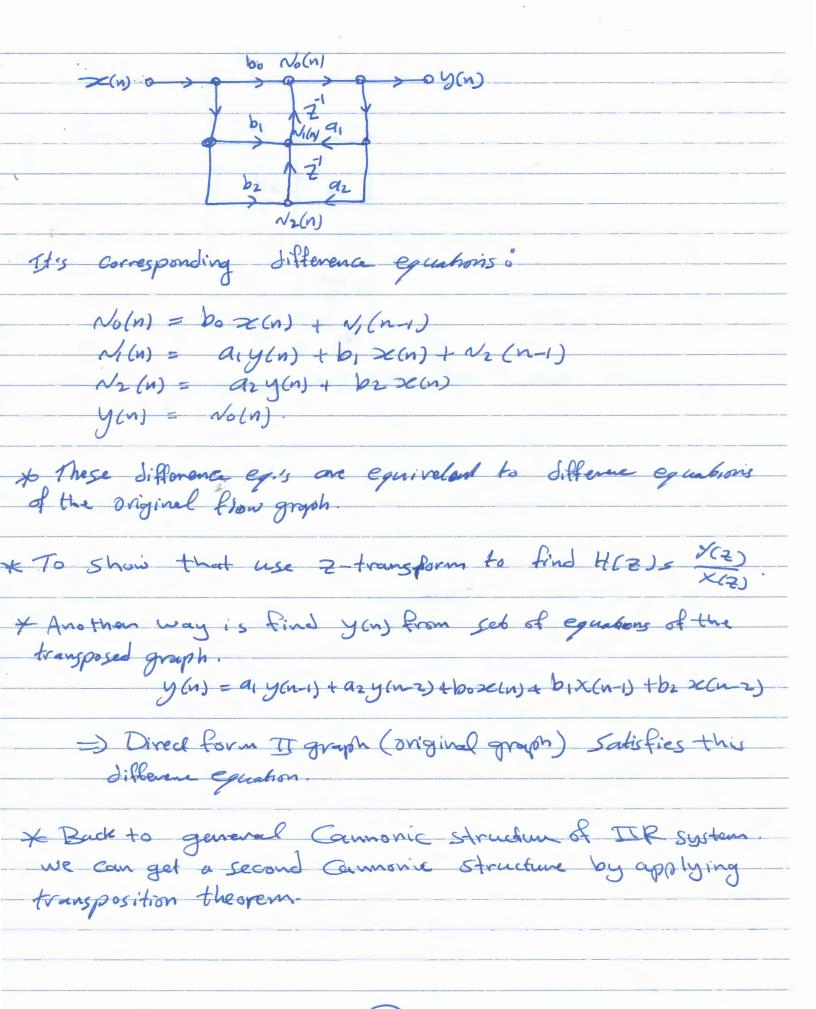
BUT Neithor Poles in H(Z) nor Fredback loops in Network are sufficient for how to be Infinitely long. is be cause pole cancels with a zono / Noncomputable Network eig. y(n) = ay(n) + x(n) * This means that cannot represent a set of difference equations that can be solved successively for the But It can be solved by y(n) - 2(n) X The key to computability of graph is that all loops must Contain at least one Jelay Clement * No delay free Loops

6.4 Transported Forms * Flow graph reversal or transposition Transmittances as they were and reversing the roles of shiputand output so that source node became sink node and vice Versa. of For Single - Input, Single-output systems, resulting flow graph has system function H(Z) same as original graph if input and output node are interchanged. 1. Reverse direction of all Branches 2. Interchange input and output Transfer function remains the same. (proof is not required!) () y(m) () H(2) = = y(n) $0 < 0 < \infty$ $0 < \infty$ 0of Flip it over to have input at right side and output at left

different only on order of 27 and multipliander by a.

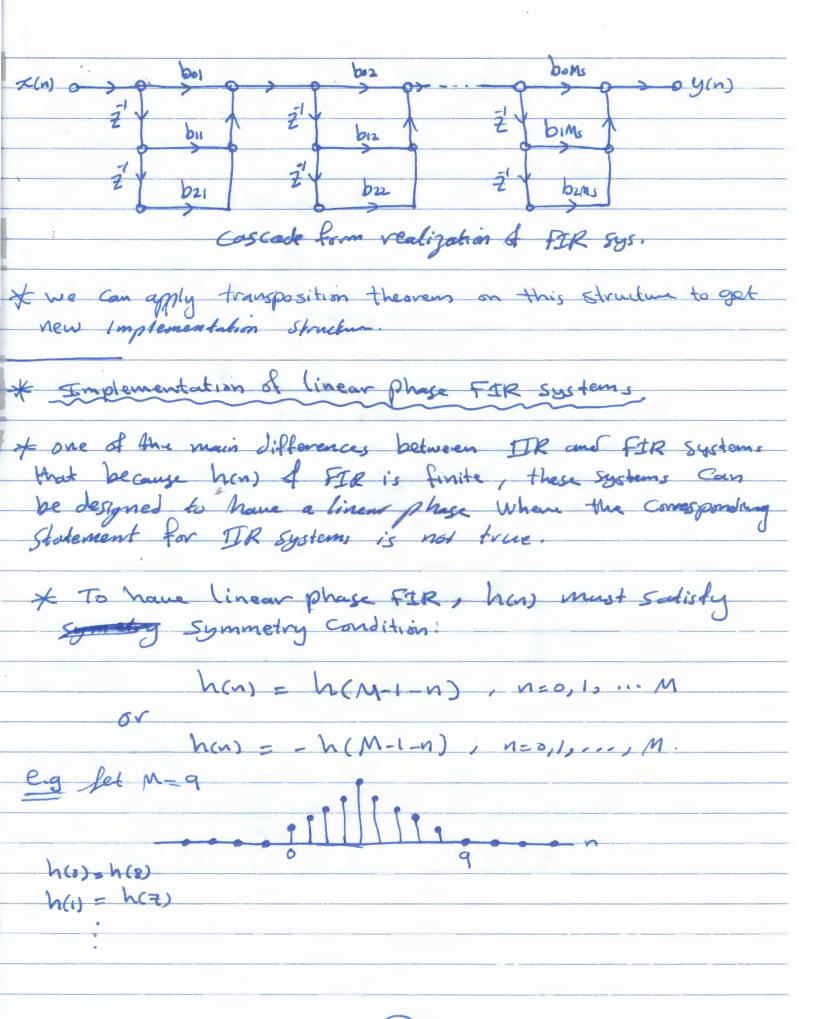
5) order not important.





60 >C(n) 0 9(n) pro-1 (Transposed

Basic Structures for FIR systems Causal FIR systems have only zero's (except for poles at 2=0), so diff. equation $= \begin{cases} h(n) = \int bn, n = 0, 1, \dots, M \\ 0, o + herwise \end{cases}$ Direct form I realization of FIR system * This is called tapped delay line structure or Transversal filter structure h(M) h(m-1) h(m-2) h(1) h(0) Transposed Direct Form I. * Cascade Forms H(Z) = = h(n) = T(box + b1x = + b2x =) Ms = L(M+1)/2/, if M is odd, one of box = 0



relation between H1 and H is only shift. h(n) = h(n+ M-1) H(ve) = jw(M=) HI(ve) hi(n) is even => Hi(ve) is real function of w. * If impulse response system, has, has this symmetry properity (i.e. has) = Th(M-1-n)), then the phase of Im System is linear. Same coeff. but H(Z)= 5 h(n) =" Jeb V = (M -1) - N Some M bue running in opposite at $N = \frac{M}{2} \Rightarrow V = M - 1 - \frac{M}{2} = \frac{M}{2} - 1$ at N=M-1 = N= M-1-(M-1) = 0 = 5 has 2" + 5 has 7 (M+1-11) # & coeff. Multipliers = 3 h(n) (7 + 7 (M-1-n)) is be-halved * requires M different Coefficients instead of M.

(25)

