Birzeit University

Computer Systems Engineering Department

Computer Organization- ENCS 238

First Exam, February, 28th, 2010

2nd semester, 2009/2010

(2 hours)

Section 1: Dr. Abdalkarim Awad Section 2: Mohammad Abu- Ayyash

Section 3: Aziz Qaroush

Name: **ID:**

Question#1(28 points)

A computer system uses two separated memories; one to store the instructions, and other to store the data. The instruction memory size is 1Mbytes, and both of the word size and instruction length in this memory is 32 bits. The data memory size is 64Kbytes, and the word size (data size) in this memory is 32 bits. Answer the following questions:

A. What is the minimum size required for the PC register? Why?

18 bits
# of words in the instruction memory = 1M/ 4Bytes = 256K words→ needs 18 address lines to access.

B. What is the size of MDR (MBR) (Memory Data(Buffer) Register) for the instruction memory? Why?

32 bits, because the size of word in instruction memory is 32 bits

C. What is the size of IR (Instruction Register)? Why?

32 bits, because the instruction length 32 bits.

D. What is the size of MDR (MBR) (Memory Data(Buffer) Register) for the data memory? Why?

32 bits, because the size of word in data memory is 32 bits

E. What is the size of MAR (Memory Address Register), which is a register used to access the instruction memory? Why?

18 bits
# of words in the instruction memory = 1M/ 4Bytes = 256K words→ needs 18 address lines to access.

F. What is the size of MAR (Memory Address Register), which is a register used to access the data memory? Why?

14 bits
# of words in the data memory = 64K/ 4Bytes = 16K words→ needs 14 address lines to access.

G. Draw the instruction format given that this machine uses only memory direct addressing mode and have 21 general registers and 13 operations.

13 operations needs 4bits

21 registers needs 5 bits

The remaining bits could be used all for memory which are 32-4-5 = 23 bits

Question#2(20)

A. Consider a common bus system shared among 11 registers, 21 bits each:

1. What is the number of Multiplexers needed to implement this bus? (3 points)

21 Muxes

2. What is the size of each multiplexer (# of inputs and # of selection lines) (3 points)

16 X 1 (4 selection lines), also 11X1 (4 selection lines), is acceptable answer

B. Compare between RISC & CISC in the following items? Briefly explain(8 points)
-Number of addressing modes
-Compiler design
-Control unit design
-Flexibility of development or enhancements
-Number of general purpose registers

C. Draw the circuit for the following RTL pseudo code: (6 points)

If (P = 1 OR Q = 0) then R1 gets (R1 + 1)
Elseif (W = 1 NAND Q = 1) then R2 gets (R1 + R2)

Where P, Q, and W are the input signals to the control unit, and R1, R2, R3 are general registers with size equal to 16 bit.

Question#3(30 points)

A. Consider a 16-bit floating-point format given in Figure below(12 points)

Sign(1bit)	Exponent (6 bits)	Significand (9 bits)

Figure.1

Let A= 3833 H and B = 362D H are two floating-point numbers, expressed in hexadecimal. Let S = A + B, find the representation of S in 16-bit format given in figure above (show how the floating point calculations are performed).

A = 3833 H = 0 011100 000110011
B = 362D H= 0 011011 000101101
Bias = 2^{6-1}-1 = 31
A exponent = 011100 = 28, real exponent =28-31 = -3
B exponent = 011011 = 27, real exponent = 27 – 31 = -4

So,
A = 1.000110011 x 10^{-3}
B = 1.000101101 x 10^{-4} = 0.100010110 x 10^{-3}
S=A+B = 1.101001001 x 10^{-3}

Representation of S:
0 011100 101001001

B. By filling in the table below (next page), run Booth's algorithm to compute the product of M (multiplicand) = 001001, and Q (multiplier) = 000111. What is the final result of multiplication? (12 points)

A	Q	Q_{-1}	M	
000000	**000111**	**0**	**001001**	**Initial values**
			001001	**First cycle** -(Q Q_{-1}) = 1 0
110111	000111	0		-A = A – M
111011	100011	1		-Shift
111101	110001	1	001001	**Second cycle** -(Q Q_{-1}) = 1 1 -Shift
111110	111000	1	001001	**Third cycle** -(Q Q_{-1}) = 1 1 -Shift
000111	111000	1	001001	**Fourth cycle** -(Q Q_{-1}) = 0 1
				- A = A + M
000011	111100	0		-Shift
000001	111110	0	001001	**Fifth cycle** -(Q Q_{-1}) = 0 0 -Shift
000000	111111	0	001001	**Sixth cycle** -(Q Q_{-1}) = 0 0 -Shift

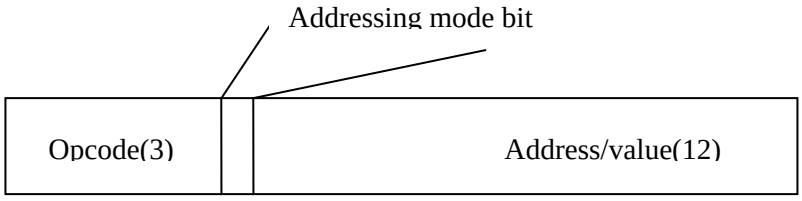
C. Which is more difficult to implement; floating point addition or floating point division operations? Why? (6 points)

Addition is more difficult because it needs exponents alignment

Question#4(22 points)

A computer has a 2-bytes addressable memory and 16-bit Instruction; the format of the instruction is shown below. Integers are 16 bit length stored in 2's complement.

Memory Address	Instructions & Data
:	:
700	**4 3 0 0**
701	**2 2 1 3**
:	**:**
3F0	**4 7 0 1**
3F1	**4 7 0 0**
3F2	**7 7 0 1**
3F3	**A 4 F 4**
:	**:**
4F4	**9 3 F 0**
4F5	**2 0 0 0**
:	:



Instruction Format

The computer has the flowing instructions:

A. What is the range of values that can be used in the immediate field? (3 points)

-2^{11} to $(2^{11}-1)$

B. What is the range of addresses that can be used in the direct field? (3 points)

0 to 2^{12}

C. Start with PC=3F1H, execute the program stored in the memory above and for each instruction show the final content the registers PC, IR, AC, MAR, MBR (or MDR), and of the memory (if changed) after the execution of each instruction. (16 points)

opcode	**instruction**
001	Stop execution
010	Load (Imm/direct) into AC If Imm AC← Imm If Direct AC← M(x) where x is the address from the Instruction
011	ADD (Imm/direct) to AC If Imm AC← AC + Imm If Direct AC← AC + M(x) where x is the address from the Instruction
100	Store into memory location M(x)←AC where x is the address from the instruction
101	Jump to a location in the memory, the address is given in the instruction

	PC	IR	AC	MAR	MDR
	3F1H	--	--	--	--
After 1st instruction	3F2	4700	700	3F1	4700
After 2nd instruction	3F3	7701	2913	701	2213
After 3rd instruction	4F4	A4F4	2913	3F3	A4F4
After 4th instruction	4F5	93F0	2913	3F0	2913
After 5th instruction	4F5	2000	2913	4F5	2000

Table 2(q