BIRZEIT UNIVERSITY

ENCS336 – 1st Exam

Dr. Emad Hamadeh

1st Semester 08/09
Date: 28/10/2008

Student ID :_____

Student Name :_____SOLUTION_____

☐ **Section 1 (1:00PM SMW)**

☐ **Section 2 (8:00AM SMW)**

Instructions:

- **You have 90 minutes, so budget your time carefully!**
- **Turn OFF your mobile.**
- **To make sure you receive credit, please write clearly and show your work.**

Question	Maximum	Your Score
1	20	
2	25	
3	15	
4	15	
5	10	
6	15	
Total	100%	

Question 1 (20 marks**) :**

a) TRUE or FALSE :

TRUE	FALSE	
○	💣	PCI Express consists of lanes such that each lane is 32-bit wide
💣	○	Performance of x machine is better than y machine if y has more execution time than x
○	💣	Extended PCI bus has 32-bit data/address lines and twice the speed of standard PCI
○	💣	Number of address lines for a 256K x 16 memory organization is 16
○	💣	Moore's Law states that the number of transistors on a chip will double every two years
○	💣	ENIAC was a binary machine programmed manually by switches
💣	○	In Booth's Algorithm, the number of Shift Arithmetic Right operations is equal to the number of bits in M or Q
💣	○	A 4-bit binary decrementer can be implemented by adding **1111b** to the desired register
○	💣	All Intel x86 family share the same basic organization in order to maintain code backwards compatibility
○	💣	AR is a special register used to store the address of next instruction to be read from memory

b) What are the main types of interrupts? And what are some of the approaches for dealing with multiple interrupts?

Main Types:

1) Hardware, 2) software, 3) special events (div by 0…)

Dealing with Multiple INTs:

1) first come first served (ignore others),

2) set priority

Question 2 (25 marks**) :**

a) An instruction encoder uses 5 bits for encoding the opcode. One of the 5-bit patterns is used as a special case, in which 3 other bits decide the actual opcode. How many unique opcodes can this computer have? (3pt)

$2^5 - 1 + 2^3 = 39$

b) A user code consists of the following four sequenced RTL lines:

T_0: **R2 ← NOT[R1]**
T_1: **R1 ← NOT[R1 + R2]**

T_2: **R2 ← ASR[R1] , R1 ← R1 U R2**
T_3: **R1 ← SHL[R1]**

Assuming 8-bit registers, with **R1 = AAh**, write out the values for R1 and R2 after the execution of each RTL line? **NOT** is bit negation operation, **SHL** is Shift Left, and **ASR** is Arithmetic Shift Right operation. **All values should be in hexadecimal**. (10pt)

After T0: R1 = ____AA_____, R2 = _____55_____

After T1: R1 = ____00_____, R2 = _____55_____

After T2: R1 = ____55_____, R2 = _____00_____

After T3: R1 = ____AA_____, R2 = _____00_____

c) Calculate the CPI and then find the CPU execution time of a computer running at 500 MHz, and the following Instruction Class distribution for a program with 100 instructions:

Class 1:	**3 CPI**	**40%**
Class 2:	**5 CPI**	**20%**
Class 3:	**3 CPI**	**30%**
Class 4:	**1 CPI**	**10%**

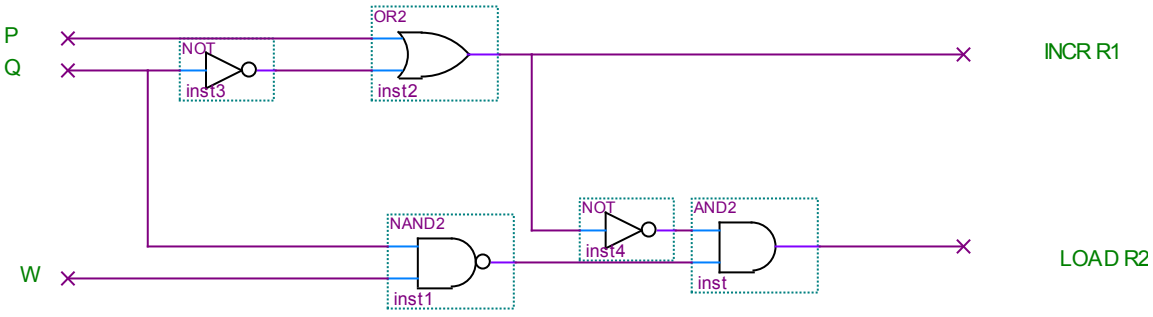
CPI = 3*0.4 + 5*0.2 + 3*0.3 + 1*0.1 = 3.2

E.T. = 100 * 3.2 / (500*10^6) = 640 ns

d) Draw the control logic (only) for the following RTL pseudo code:

If (P = 1 OR Q = 0) then R1 gets (R1 + 1)
Elseif (W = 1 NAND Q = 1) then R2 gets (R1 + R2)

Where P, Q, and W are the input signals to the control unit. (6pt)



Question 3 (15 marks):

a) Show the steps for doing **(- 8 x - 5)** using Booth's algorithm? Write final result. (10pts)

A	Q	Q_{-1}	M	Comments
00000	11011	0	11000	Initial Values

Result = AQ = 00001 01000 = 40

b) How many addition and how many subtraction operations are needed when using Booth's algorithm to multiply a number X by the multiplier **"11101001110b"**

Number of Addition Operations: _____2_____

Number of Subtraction Operations: _____3_____

Just count the pairs of "01" for addition and "10" for subtraction

Question 4: (15 marks)

a) Given the 32-bit pattern

1011	1111	1100	1000	0000	0000	0000	0000

What is the value in **decimal** if the above pattern is for:

I) Unsigned integer? 2pts

$2^{31} + (2^{30} - 2^{22}) + 2^{19} = 3{,}217{,}555{,}456$

II) Two's complement integer? 3pts
Sign bit is 1, negative

0100	0000	0011	1000	0000	0000	0000	0000

$= - (2^{30} + (2^{22} - 2^{19}) = - 1{,}077{,}411{,}840$

III) Single format floating point number? 5pts

Sign = 1, i.e. negative
Biased Exponent = $(2^7 - 2^0) = 127$
True exponent = 127 – 127 = 0
Fraction = $2^{-1} + 2^{-4} = 0.5625$

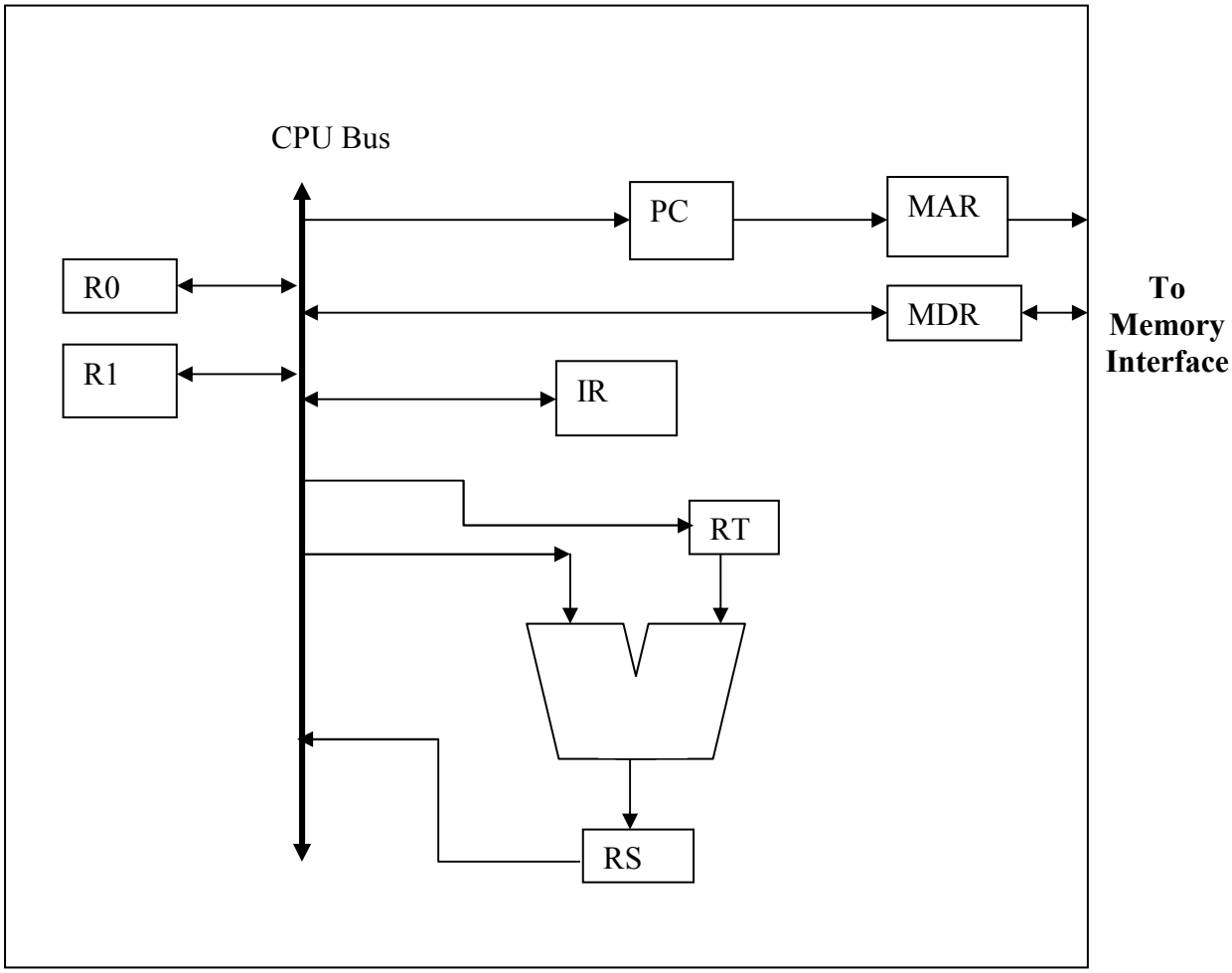
Value = - 1.5625 x 2^0 = -1.5625

b) Which is more difficult to implement; floating point addition or floating point division operations? Why?

Floating point Addition
Need alignment of exponents

Question 5: (10 marks)
Draw a block diagram of the data path for a CPU that has the following hardware components: 2 general purpose registers **(R0, R1)**, Program Counter **(PC)**, Instruction Register **(IR)**, an **ALU** that can perform logical and arithmetic functions, Memory Address Register **(MAR)**, Memory Data Register **(MDR)**, a register that temporarily holds one operand for the ALU **(RT)**, and a register to temporarily hold the result from the ALU **(RS)**.

Use a single CPU bus, drawn below, to interconnect the hardware resources.



Question 6 (15 marks):

A **4K x 16** memory, shown below, is used to store instructions set and data for a basic computer architecture based machine. The first instruction is stored at memory address location **FF0h**;

a) fill in the table below with the values for **PC**, **IR**, and **AC**? Initial values mean the values of the registers prior to fetching the first instruction from memory.

Opcode **1h** is to load AC from memory
Opcode **3h** is to store AC to memory, while
Opcode **5h** is to add to AC from memory.
(All numbers are in hex representation)

Instruction Phase	PC	IR	AC
Initial Values	FF0	--	--
After 1st Instruction Fetch	FF1	1FF3	--
After 1st Instruction Execution	FF1	1FF3	3402
After 2nd Instruction Fetch	FF2	5401	3402
After 2nd Instruction Execution	FF2	5401	8402

Memory Address	Instructions & Data
:	:
400	0 A C E
401	5 0 0 0
402	3 1 0 0
403	0 F F 1
:	:
FF0	1 F F 3
FF1	5 4 0 1
FF2	3 F F 1
FF3	3 4 0 2
:	:

b) Using the above memory organization, what is the value of the operand stored in memory if the instruction format indicated an **indirect memory access** with an **address field** value of **403h**?

5401

BIRZEIT UNIVERSITY

ENCS336 – 1st Exam

2nd Semester 07/08
Date: 20/4/2008

ID :_____

Name :_____

☐ **Section 1** **Dr. Emad Hamadeh**

☐ **Section 2** **Eng. Mamoun Nawahdah**

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Question 1 (15 marks) :

a) TRUE or FALSE :

TRUE	FALSE	
●	○	Design of common bus for 16 registers of 32-bits each requires 32 multiplexers
○	●	Performance of x machine is better than y machine if x has **more** execution time than y
○	●	Extended PCI bus has **32-bit** data/address lines and twice the speed of standard PCI
○	●	Number of address lines for a 512K x 16 memory organization is **16**
○	●	The clock rate for a clock with a period of 250 nanosecond is 4 **G**Hz
○	●	MIPS stands for **Multi** Instructions Per Second
●	○	In Booth's Algorithm, the number of Shift Arithmetic Right operations is equal to the number of bits in M or Q
●	○	The ASCII code for the character '7' is 55 in decimal
○	●	All Intel x86 family share the same basic **organization** in order to maintain code backwards compatibility
○	●	ENIAC was a **binary** machine programmed manually by switches

---

Question 2 (15 marks) :

a) State whether the following none related register transfer statements are legal or not?

If not, why?

1. **D.T : AR ← AR' , AR ← 0**

Illegal, can't assign to operations to AR at once

2. **X : PC ← AR**

Legal

b) Use register transfer statements with required control to represent the following pseudo code:

```
If (x = 1)   then
      R1 gets R2
else
   If (y = 1) then
        R1 gets R3
```

X: R1 ← R2
X'Y: R1 ← R3

c) If operand **A** is $\mathbf{01001_b}$, and operand **B** is unknown, what logic operation and **B** value would you use to obtain a $\mathbf{10001_b}$ result? Draw any needed logic blocks.

A XOR B with B = 11000b,
Draw an XOR gate

Question 3 (15 marks):

a) A system with three I/O devices: printer, disk, and communication line. The devices have interrupt priority of **3** for printer, **6** for disk, and **8** for communication line such that the higher the number the higher the priority, and vv. It takes any ISR **10** time-units to process its interrupt. A User Program starts executing at **t = 0**. If a disk interrupt occurs at **t =20**, and a communication line interrupt occurs at **t = 28**, and a printer interrupt occurs at **t = 35**, when will each ISR completes its execution of its interrupt?

Communication Line Interrupt completes at t = 38
Disk Interrupt completes at t = 40
Printer Interrupt completes at t = 50

b) Computer A, running at **500 MHz**, has a program with the following instruction classes, CPI budget, and number of instructions distribution.

Instruction Class	CPI	Number of Instructions
A	3	50
B	2	20
C	4	30

1. Find the Average CPI for running the above program?

Ave CPI = 3x(50/100) + 2x(20/100) + 4x(40/100)
= 3.1

2. Find the CPU execution time for computer A?

CPU Time = (# of Instructions) x (Ave. CPI) x (Clock Cycle Time)
= 100 x 3.1 x (1/(500x10^6)) = 620 ns

Question 4 (15 marks):

A **2K x 16** memory, shown below, is used to store instructions set and data for a basic computer architecture based machine. If first instruction is stored at memory address location **400h**, fill in the table below with the values for **PC**, **IR**, and **AC**? Initial values mean the values of the registers prior to fetching the first instruction from memory.

Opcode **1h** is to load AC from memory
Opcode **3h** is to store AC to memory, while
Opcode **5h** is to add to AC from memory.
(All numbers are in hex representation)

Instruction Phase	PC	IR	AC
Initial Values	400	---	---
After 1st Instruction Fetch Cycle	401	1 F F 0	---
After 1st Instruction Execution Cycle	401	1 F F 0	0 1 0 0
After 2nd Instruction Fetch Cycle	402	5 F F 3	0 1 0 0
After 2nd Instruction Execution Cycle	402	5 F F 3	0 F 0 F

Memory Address	Instructions & Data
:	:
400	1 F F 0
401	5 F F 3
402	3 F F 2
:	:
FF0	0 1 0 0
FF1	5 0 0 0
FF2	3 1 0 0
FF3	0 E 0 F
:	:

Question 5 (20 marks):

a) What is the range of two's complement integers that can be represented using **12 bits**? Give your answers in decimal.

$$-2^{11} \leftrightarrow +2^{11}-1$$
$$-2048 \leftrightarrow +2047$$

b) Given the bit pattern:

1011 1111 1110 0000 0000 0000 0000 0000

What is the value (in *decimal*) that this pattern represent, assuming that it is:

1. A two's complement integer?

```
  0100 0000 0001 1111 1111 1111 1111 1111
+ 0000 0000 0000 0000 0000 0000 0000 0001
-------------------------------------------
  0100 0000 0010 0000 0000 0000 0000 0000
```

$$\begin{aligned} -2^{30} + 2^{21} &= -(2^9 + 1) \times 2^{21} \\ &= -(513 \times 2 \times 1024 \times 1024) \\ &= -1.075 \times 10^9 \end{aligned}$$

2. A single format floating-point number?

1	0111 1111	110 0000 0000 0000 0000 0000

$$\begin{aligned} S &= 1 \\ exponent &= 2^7 - 1 = 128 - 1 = 127 \\ fraction &= 2^{-1} + 2^{-2} = 0.5 + 0.25 = 0.75 \\ N &= (-1)^1 \times 1.75 \times 2^{127-127} = -1 \times 1.75 \times 1 = -1.75 \end{aligned}$$

d) Consider the division of a **dividend X=8** and a **Divisor D=3** using unsigned algorithm. Show your work step by step in the following table?

Q ← Dividend (8d ➔ 1000b)
M ← Divisor (3d ➔ 0011b)
-M ← (-3d ➔ 1101b)

	A	Q	M	Comments
	0000	1000	0011	Initial value
N=4	0001	0000		Shift left A,Q
	1110	0000		A ← A - M
	0001	0000		A < 0 ? YES Restore
N=3	0010	0000		Shift left A,Q
	1111	0000		A ← A - M
	0010	0000		A < 0 ? YES Restore
N=2	0100	0000		Shift left A,Q
	0001	0000		A ← A - M
	0001	0001		A < 0 ? NO Restore
N=1	0010	0010		Shift left A,Q
	1111	0010		A ← A - M
	0010	**0010**		A < 0 ? YES Restore
	Reminder	**Quotient**		

Question 6 (20 marks):

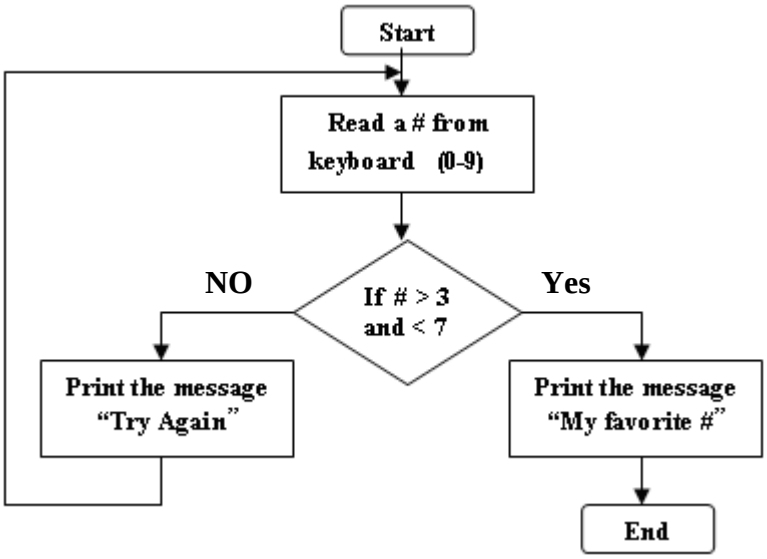
a) Write an assembly code to find the average of two numbers stored in **AL** and **DL** using *ONLY* the following assembly instructions:

MOV ➔ move
ADD ➔ add
ADC ➔ add with carry
SAR ➔ shift arithmetic right

```
MOV AH, 00H
ADD AL, DL
ADC AH, 00H
SAR AX, 1
```

Result in AL is the average of AL and DL

b) Convert the following flow chart to an assembly program




```
ideal
p286n
model tiny
codeseg
        org 100h
        JMP ABAS
        mesg2 db "Try Again $"
        mesg1 db "My favorite # $"


ABAS:
        ; Read character from keyboard
        MOV DL, 0FFH
        MOV AH, 06H
        INT 21H
        JZ ABAS
        SUB AL, 30H      ;convert ASCII # to a binary number

        ; IF
        CMP AL, 3
        JLE NO
        CMP AL, 7
        JGE NO

        ; THEN    print the message "My Favorite #"
        MOV DX, OFFSET mesg1
        MOV AH, 09
        INT 21H
        JMP EXIT

        ; ELSE    print the message "Try Again"
NO:     MOV DX, OFFSET mesg2
        MOV AH, 09
        INT 21H
        JMP ABAS

EXIT:
        mov ax, 4c00h
        int 21h
end
```

c) Show the absolute addresses formed by **SP** contains **0040h** and **SS** contains **B42Ah**

SS:SP ➔ B42A:0040 ➔ **B42Ah * 16d + 0040h ➔ B42E0h**
B42Ah * 10h + 0040h ➔ B42E0h

BIRZEIT UNIVERSITY

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	0001	0000		A < 0 ? YES Restore
N=3	0010	0000		Shift left A,Q
	1111	0000		A ← A - M
	0010	0000		A < 0 ? YES Restore
N=2	0100	0000		Shift left A,Q
	0001	0000		A ← A - M
	0001	0001		A < 0 ? NO Restore
N=1	0010	0010		Shift left A,Q
	1111	0010		A ← A - M
	0010	**0010**		A < 0 ? YES Restore
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Question 6 (20 marks):

a) Write an assembly code to find the average of two numbers stored in **AL** and **DL** using *ONLY* the following assembly instructions:

MOV ➔ move
ADD ➔ add
ADC ➔ add with carry
SAR ➔ shift arithmetic right

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MOV AH, 00H
ADD AL, DL
ADC AH, 00H
SAR AX, 1
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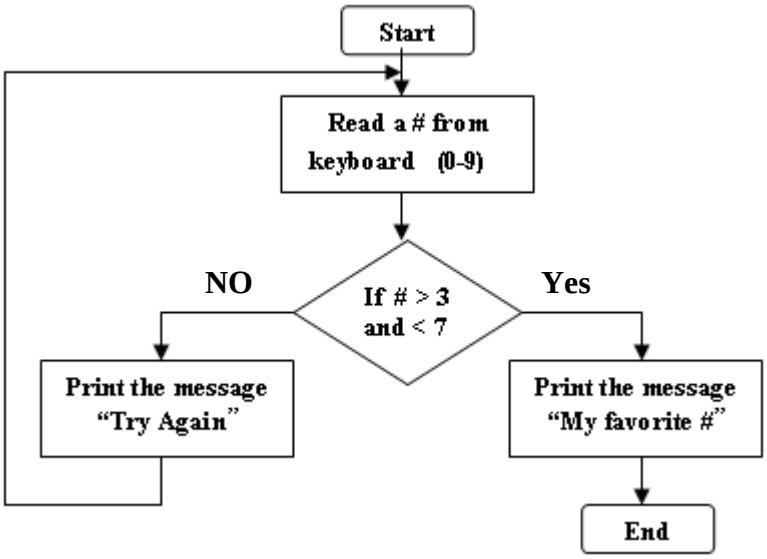
Result in AL is the average of AL and DL

b) Convert the following flow chart to an assembly program

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        JMP ABAS
        mesg2 db "Try Again $"
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        ; Read character from keyboard
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        ; IF
        CMP AL, 3
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        CMP AL, 7
        JGE NO

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        INT 21H
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        JMP ABAS

EXIT:
        mov ax, 4c00h
        int 21h
end
```

c) Show the absolute addresses formed by **SP** contains **0040h** and **SS** contains **B42Ah**

SS:SP ➔ B42A:0040 ➔ **B42Ah * 16d + 0040h ➔ B42E0h**
B42Ah * 10h + 0040h ➔ B42E0h

Birzeit University

Computer Systems Engineering Department

Computer Organization- ENCS 238

First Exam, February, 28th, 2010

2nd semester, 2009/2010

(2 hours)

Section 1: Dr. Abdalkarim Awad Section 2: Mohammad Abu- Ayyash

Section 3: Aziz Qaroush

Name: **ID:**

Question#1(28 points)

A computer system uses two separated memories; one to store the instructions, and other to store the data. The instruction memory size is 1Mbytes, and both of the word size and instruction length in this memory is 32 bits. The data memory size is 64Kbytes, and the word size (data size) in this memory is 32 bits. Answer the following questions:

A. What is the minimum size required for the PC register? Why?

18 bits
# of words in the instruction memory = 1M/ 4Bytes = 256K words→ needs 18 address lines to access.

B. What is the size of MDR (MBR) (Memory Data(Buffer) Register) for the instruction memory? Why?

32 bits, because the size of word in instruction memory is 32 bits

C. What is the size of IR (Instruction Register)? Why?

32 bits, because the instruction length 32 bits.

D. What is the size of MDR (MBR) (Memory Data(Buffer) Register) for the data memory? Why?

32 bits, because the size of word in data memory is 32 bits

E. What is the size of MAR (Memory Address Register), which is a register used to access the instruction memory? Why?

18 bits
# of words in the instruction memory = 1M/ 4Bytes = 256K words→ needs 18 address lines to access.

F. What is the size of MAR (Memory Address Register), which is a register used to access the data memory? Why?

14 bits
# of words in the data memory = 64K/ 4Bytes = 16K words→ needs 14 address lines to access.

G. Draw the instruction format given that this machine uses only memory direct addressing mode and have 21 general registers and 13 operations.

13 operations needs 4bits

21 registers needs 5 bits

The remaining bits could be used all for memory which are 32-4-5 = 23 bits

Question#2(20)

A. Consider a common bus system shared among 11 registers, 21 bits each:

1. What is the number of Multiplexers needed to implement this bus? (3 points)

21 Muxes

2. What is the size of each multiplexer (# of inputs and # of selection lines) (3 points)

16 X 1 (4 selection lines), also 11X1 (4 selection lines), is acceptable answer

B. Compare between RISC & CISC in the following items? Briefly explain(8 points)
-Number of addressing modes
-Compiler design
-Control unit design
-Flexibility of development or enhancements
-Number of general purpose registers

C. Draw the circuit for the following RTL pseudo code: (6 points)

If (P = 1 OR Q = 0) then R1 gets (R1 + 1)
Elseif (W = 1 NAND Q = 1) then R2 gets (R1 + R2)

Where P, Q, and W are the input signals to the control unit, and R1, R2, R3 are general registers with size equal to 16 bit.

Question#3(30 points)

A. Consider a 16-bit floating-point format given in Figure below(12 points)

Sign(1bit)	Exponent (6 bits)	Significand (9 bits)

Figure.1

Let A= 3833 H and B = 362D H are two floating-point numbers, expressed in hexadecimal. Let S = A + B, find the representation of S in 16-bit format given in figure above (show how the floating point calculations are performed).

A = 3833 H = 0 011100 000110011
B = 362D H= 0 011011 000101101
Bias = 2^{6-1}-1 = 31
A exponent = 011100 = 28, real exponent =28-31 = -3
B exponent = 011011 = 27, real exponent = 27 – 31 = -4

So,
A = 1.000110011 x 10^{-3}
B = 1.000101101 x 10^{-4} = 0.100010110 x 10^{-3}
S=A+B = 1.101001001 x 10^{-3}

Representation of S:
0 011100 101001001

B. By filling in the table below (next page), run Booth's algorithm to compute the product of M (multiplicand) = 001001, and Q (multiplier) = 000111. What is the final result of multiplication? (12 points)

A	Q	Q_{-1}	M	
000000	**000111**	**0**	**001001**	**Initial values**
			001001	**First cycle** **-(Q Q_{-1}) = 1 0** **-A = A – M**
110111 111011	000111 100011	0 1		**-Shift**
111101	110001	1	001001	**Second cycle** **-(Q Q_{-1}) = 1 1** **-Shift**
111110	111000	1	001001	**Third cycle** **-(Q Q_{-1}) = 1 1** **-Shift**
000111	111000	1	001001	**Fourth cycle** **-(Q Q_{-1}) = 0 1** **- A = A + M**
000011	111100	0		**-Shift**
000001	111110	0	001001	**Fifth cycle** **-(Q Q_{-1}) = 0 0** **-Shift**
000000	111111	0	001001	**Sixth cycle** **-(Q Q_{-1}) = 0 0** **-Shift**

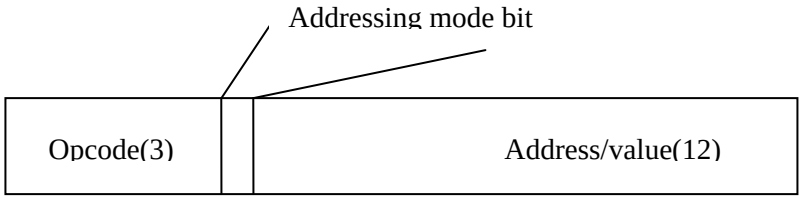
C. Which is more difficult to implement; floating point addition or floating point division operations? Why? (6 points)

Addition is more difficult because it needs exponents alignment

Question#4(22 points)

A computer has a 2-bytes addressable memory and 16-bit Instruction; the format of the instruction is shown below. Integers are 16 bit length stored in 2's complement.

Memory Address	Instructions & Data
:	:
700	**4 3 0 0**
701	**2 2 1 3**
:	**:**
3F0	**4 7 0 1**
3F1	**4 7 0 0**
3F2	**7 7 0 1**
3F3	**A 4 F 4**
:	**:**
4F4	**9 3 F 0**
4F5	**2 0 0 0**
:	:



Instruction Format

The computer has the flowing instructions:

A. What is the range of values that can be used in the immediate field? (3 points)

-2^{11} to $(2^{11}-1)$

B. What is the range of addresses that can be used in the direct field? (3 points)

0 to 2^{12}

C. Start with PC=3F1H, execute the program stored in the memory above and for each instruction show the final content the registers PC, IR, AC, MAR, MBR (or MDR), and of the memory (if changed) after the execution of each instruction. (16 points)

opcode	**instruction**
001	Stop execution
010	Load (Imm/direct) into AC If Imm AC← Imm If Direct AC← M(x) where x is the address from the Instruction
011	ADD (Imm/direct) to AC If Imm AC← AC + Imm If Direct AC← AC + M(x) where x is the address from the Instruction
100	Store into memory location M(x)←AC where x is the address from the instruction
101	Jump to a location in the memory, the address is given in the instruction

	PC	IR	AC	MAR	MDR
	3F1H	--	--	--	--
After 1st instruction	3F2	4700	700	3F1	4700
After 2nd instruction	3F3	7701	2913	701	2213
After 3rd instruction	4F4	A4F4	2913	3F3	A4F4
After 4th instruction	4F5	93F0	2913	3F0	2913
After 5th instruction	4F5	2000	2913	4F5	2000

Table 2(q

BIRZEIT UNIVERSITY

ENCS238 – First Exam

2nd Semester 08/09
Date: April 9, 2009

Student ID : _____

Student Name: _Typical Solutions__

☐ **Section 1**	**Abdel Salam Sayyad**
☐ **Section 2**	**Mohammad Abu Ayyash**
☐ **Section 3**	**Mahmoud Qasrawi**

Instructions:

- **You have 80 minutes to answer all questions, so budget your time carefully!**
- **Turn OFF your mobile**
- **To make sure you receive credit, please write clearly and show your work**

Question	Maximum	Your Score
1	36	
2	36	
3	30	
Total	102%	

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Question 1: Multiple Choice (36 marks)

Score	

1. Reading and writing to the memory unit (RAM) takes place via:

a. the ALU and the register unit
b. the memory address and memory data registers
c. the program counter and the memory data register
d. the Program Counter and the Instruction Register
e. the write enable line

2. Given an ISA computer specifying a word size of 4 bytes, byte addressability, and an address space of 16 MB: What is the size of the PC register?

a. 8 bits b. 16 bits c. 24 bits d. 32 bits e. 16 Mbits

3. Given an ISA computer specifying a word size of 4 bytes, byte addressability, and an address space of 16 MB: What is the size of the IR?

a. 8 bits b. 16 bits c. 24 bits d. 32 bits e. 16 Mbits

4. The Program Counter register is:

a. a binary counter that keeps track of the number of instructions executed
b. a register that stores the next instruction to be executed
c. a control circuit that steps through a sequence of instructions
d. a register that stores the address of the next memory location to be written to
e. a register that stores the memory address of the next instruction

5. The purpose of the control unit is:

a. to store the list of instructions
b. to fetch the next instruction from memory & decode it
c. to control the ALU
d. to control access to memory
e. to clock the transitions between states of the whole microprocessor

6. DS=1000h ES=1200h CS=1300h SS=1400h BP=5500h BX=0300h SI=0200h DI=0300h. Consider the instruction **MOV [BX+SI], BP**

The content of BP register will be copied to:

a. Memory physical addresses 10500h,10501h
b. Memory physical addresses 10700h,10701h
c. Memory physical addresses 0500h,0501h
d. Registers BX and SI.
e. Registers DS, BX and SI.

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7. Using Tasm Assembler , **MOV CX,100** will:

a. Copy 100 hexadecimal to CX
b. Copy 100 decimal to CX
c. Copy 100 binary to CX
d. Will give you a warning message: the source must be 100d or 100h
e. Will give you an error message: the source must be 100d or 100h

8. The following directive defines the Number 4503h using assembly language:

a. NUM1 DB 45h,03h
b. NUM1 DB 3h, 45h
c. NUM1 DB 45h,3h
d. NUM1 DW 45h,03h
e. NUM1 DD 45h,03h

9. The memory segment that holds the programs and procedures used by microprocessor is:

a. Code Segment
b. Data Segment
c. Extended Segment
d. Stack Segment
e. Data Segment and Extended Segment

10. If SP=FFEE BP=0000h SI=0000h DI=0000h DS=1500h ES=1100h SS=1600h CS=1400h IP=1200h , The microprocessor fetches its next instruction from the physical memory location:

a. 1200h **b.** 15200h **c.** 1400h **d.** 2600h **e.** 16200h

11. If the starting address of variable1 in memory is 0B00:0100, AX=1000h.

The instructions **LEA AX, VARIABLE1** or **MOV AX, OFFSET variable1** will:

a. Load AX with the value 0100h
b. Load AX with the value 0B00h
c. Load AX with value B100h
d. Load AX with value of DS register
e. Load AX with value DSx10+DI

12. If CH=22h, after executing the instruction **SUB CH,44H**; CH and flag bits will be:

a. CH=DEh, ZF= 0, CF=0, SF=0
b. CH=DEh, ZF= 0, CF=0, SF=1
c. CH=DEh, ZF= 1, CF=1, SF=0
d. CH=DEh, ZF= 0, CF=1, SF=1
e. CH=DEh, ZF= 1, CF=1, SF=1

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Student ID : _____

Student Name: _____

☐ **Section 1**	**Abdel Salam Sayyad**
☐ **Section 2**	**Mohammad Abu Ayyash**
☐ **Section 3**	**Mahmoud Qasrawi**

Question 2: Multiple Choice (36 marks)

Score	

13. At a given time, contents of registers R1=45d, R2=10d, the control line P=0, control line Q=1, after execution the RTL PQ:R1←R2, the contents will be

a. R1=45d, R2=10d, P=0, Q=1
b. R1=10d, R2=10d, P=0, Q=1
c. R1=45d, R2=10d, P=1 Q=1
d. R1=10d, R2=10d, P=0, Q=1
e. R1=45d, R2=45d, P=0, Q=1

14. A computer system has seven 8-bit registers. We need to implement a shared 8-bit data bus. We need:

a. Eight 8x1 multiplexers
b. Eight 4x1 multiplexers
c. Seven 8x1 multiplexers
d. Eight 2x4 decoders
e. Seven 2x4 decoders

15. What is the effect of the following instruction? **MOV CX, [BP + 8]**

a. Add 8 to the contents of BP and store the sum in CX.
b. Add 8 to the contents of DS+BP and store the sum in CX.
c. Add 8 to the contents of BP, treat the sum as a memory address and store the contents at that address in CX.
d. Add 8 to the contents of the memory location whose address is stored in BP and store the sum in CX.
e. Add the contents of BP to the contents of memory address 8 and store the sum in CX.

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16. One of the following is illegal instruction

a. MOV CL,[BX]
b. POP AL
c. MOV WORD PTR [BX],AX
d. INC [DI]
e. MOV DS,AX

17. If AL=00000100b, BL=01000001b , then after execution the instruction

CMP AL, BL

The contents of AL and zero-flag bit are:

a. AL=00000100, ZF=0
b. AL=00000100, ZF=1
c. AL=00000000, ZF=0
d. AL=00000000, ZF=1
e. AL=01000101, ZF=0

18. Variable MESSAGE is defined as follows:

MESSAGE DW 10h, 122Fh, 12Eh

How many bytes does the variable MESSAGE occupy in the memory?

a. 3
b. 4
c. 5
d. 6
e. 9

19. The arithmetic instruction D = A + B' is a

a. Subtract operation
b. Add operation
c. Add with carry
d. Subtract with borrow
e. 2's complement operation

20. Moore's Law stated that the number of _____ on a chip would double every year.

a. Logic gates
b. Flip Flops
c. Transistors
d. Capacitors
e. All the above

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21. when a processor executes a procedure call,

a. It pushes the content of IR (instruction register) onto the stack, and then changes the IR value.
b. It pushes the content of PC onto the stack, and then changes the IR value.
c. It pushes the content of PC onto the stack, and then changes the PC value.
d. It pushes the content of IR onto the stack, and then changes the PC value.
e. It pushes the content of AC onto the stack, and then changes the AC value.

22. Multiplexed Address/Data buses have the advantage of:

a. Speed of operation
b. Lower Cost
c. No need for a clock
d. Simpler Design
e. None of the above

23. Multiple-bus hierarchies have the advantage of:

a. Increased performance and lower cost
b. Simpler design and lower cost
c. Increased performance and lower cost
d. Increased performance and wider device choices
e. None of the above

24. In the 8086 processor, the register DI stands for:

a. Data Instruction
b. Destination Instruction
c. Destination Index
d. Data Index
e. None of the above

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Student ID : _____

Student Name: _____

☐ **Section 1** **Abdel Salam Sayyad**

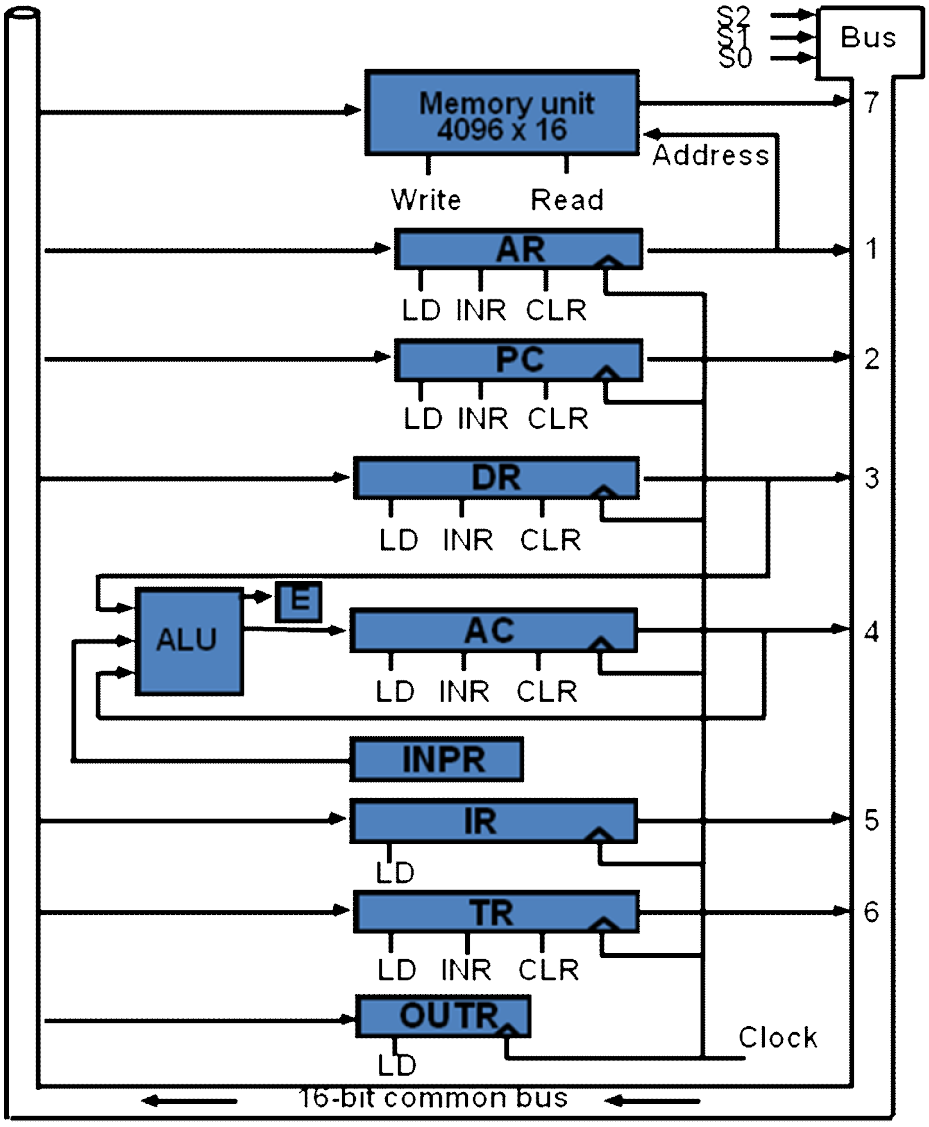
☐ **Section 2** **Mohammad Abu Ayyash**

☐ **Section 3** **Mahmoud Qasrawi**

Score	

Question 3: (20 marks)

Consider the Basic Computer shown below:



(Questions on next page…)

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What will be the register transfer executed during the next clock cycle if the following control signals are active:

a) $S_2S_1S_0$ = 111, LD of register IR, Memory Read. [4 marks]

IR ← M[AR]

b) $S_2S_1S_0$ = 100, LD of register DR, Memory Write. [4 marks]

DR ← AC
M[AR] ← AC

What is the sequence of micro-operations (and the corresponding control signals) needed to perform the following operations:

c) M[DR] = M[PC] + AC [6 marks]

AR ← PC
TR ← DR
DR ← M[AR]
AC ← AC + DR
AR ← TR (only 12 bits are transferred)
M[AR] ← AC

d) DR = DR + AC [6 marks]

DR ← AC , AC ← DR
AC ← AC + DR
DR ← AC , AC ← DR

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Question 4: (10 marks)

Consider a computer system with memory of size 4096 locations, 1 byte each. Its instruction length is 16 bits and consists of op-code portion, addressing mode bit, and address/operand portion. Suppose that the computer uses only direct-memory and immediate addressing modes.

a. What is the maximum number of instructions that can be supported by this computer? Why? [5 marks]

The opcode field is 3-bit long, ➔ max number of instructions = $2^3 = 8$

b. If the ADD instruction with immediate value is used, what is the maximum unsigned value that can be added? [5 marks]

The immediate value field is 12-bit long, ➔ max unsigned number = $2^{12} - 1 = 4095$

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Question 2: (15 marks)

a) Why is the memory system of a computer organized as a hierarchy? What are the basic elements of a memory hierarchy?

To balance the need for high performance (short access time) [1 mark] with the need for great capacity/ low cost per bit [1 mark]

Basic Elements: (1) In-board memory (CPU Registers, Cache, Main Memory) [1 mark]
(2) Out-board memory (Magnetic Disk, Optical Devices) [1 mark]
(3) Off-line storage (Magnetic Tape) [1 mark]

b) Give a precise definition of hit ratio, as applied to cache memory.

Hit Ratio: "Fraction of memory accesses involving only cache memory." [3 marks]

c) Locality of reference is an important feature of programs, in the context of memory hierarchies. Explain what locality of reference means and why is it important in view of the above 2 items.

Locality of Reference: "Memory addresses in the vicinity of a referenced word are likely to be referenced in the near future." OR: "Memory references tend to cluster." [3 marks]

Examples: Loops, subroutines, tables, records. [1 mark]

Importance: Memory locations most likely to be accessed soon can be placed closer to the top of the memory hierarchy. Thus, frequency of processor access to the memory should decrease as we move down the memory hierarchy. [3 marks]

Question 3: (20 marks)

Suppose physical addresses are 32 bits wide, in a byte-addressable multiplexed system bus. Suppose there is a cache containing 256K words of data (not including tag bits), and each cache block contains 4 words. For each of the following cache configurations, specify how the 32-bit address would be partitioned. Justify your answers.

1. direct mapped

Multiplexed bus → data lines = address lines = 32 lines

4 words per block → 2 address bits to locate words within a block [3 marks]

Byte-addressable → 2 address bits to locate bytes within a word [2 marks]

Cache size = 256 K words / 4 = 64 K lines (blocks) = 2^{16} [3 marks]

→ L = 16 [2 marks]

T = 32 – 16 – 2 – 2 = 12 [3 marks]

Tag	Line	Word	Byte
12	16	2	2

2. 2-way set associative

2 blocks per set → # sets = 64 K /2 = 32 K = 2^{15} [3 marks]

→ S = 15 [2 marks]

T = 32 – 15 – 2 – 2 = 13 [2 marks]

Tag	Set	Word	Byte
13	15	2	2

BIRZEIT UNIVERSITY

ENCS336 – 1st Exam

Dr. Emad Hamadeh

1st Semester 08/09
Date: 28/10/2008

Student ID :_____

Student Name :_____SOLUTION_____

☐ **Section 1 (1:00PM SMW)**

☐ **Section 2 (8:00AM SMW)**

Instructions:

- **You have 90 minutes, so budget your time carefully!**
- **Turn OFF your mobile.**
- **To make sure you receive credit, please write clearly and show your work.**

Question	Maximum	Your Score
1	20	
2	25	
3	15	
4	15	
5	10	
6	15	
Total	100%	

Question 1 (20 marks**) :**

a) TRUE or FALSE :

TRUE	FALSE	
○	💣	PCI Express consists of lanes such that each lane is 32-bit wide
💣	○	Performance of x machine is better than y machine if y has more execution time than x
○	💣	Extended PCI bus has 32-bit data/address lines and twice the speed of standard PCI
○	💣	Number of address lines for a 256K x 16 memory organization is 16
○	💣	Moore's Law states that the number of transistors on a chip will double every two years
○	💣	ENIAC was a binary machine programmed manually by switches
💣	○	In Booth's Algorithm, the number of Shift Arithmetic Right operations is equal to the number of bits in M or Q
💣	○	A 4-bit binary decrementer can be implemented by adding **1111b** to the desired register
○	💣	All Intel x86 family share the same basic organization in order to maintain code backwards compatibility
○	💣	AR is a special register used to store the address of next instruction to be read from memory

b) What are the main types of interrupts? And what are some of the approaches for dealing with multiple interrupts?

Main Types:

1) Hardware, 2) software, 3) special events (div by 0…)

Dealing with Multiple INTs:

1) first come first served (ignore others),

2) set priority

Question 2 (25 marks**) :**

a) An instruction encoder uses 5 bits for encoding the opcode. One of the 5-bit patterns is used as a special case, in which 3 other bits decide the actual opcode. How many unique opcodes can this computer have? (3pt)

$2^5 - 1 + 2^3 = 39$

b) A user code consists of the following four sequenced RTL lines:

T_0: **R2 ← NOT[R1]**
T_1: **R1 ← NOT[R1 + R2]**

T_2: **R2 ← ASR[R1] , R1 ← R1 U R2**
T_3: **R1 ← SHL[R1]**

Assuming 8-bit registers, with **R1 = AAh**, write out the values for R1 and R2 after the execution of each RTL line? **NOT** is bit negation operation, **SHL** is Shift Left, and **ASR** is Arithmetic Shift Right operation. **All values should be in hexadecimal**. (10pt)

After T0: R1 = ____AA_____, R2 = _____55_____

After T1: R1 = ____00_____, R2 = _____55_____

After T2: R1 = ____55_____, R2 = _____00_____

After T3: R1 = ____AA_____, R2 = _____00_____

c) Calculate the CPI and then find the CPU execution time of a computer running at 500 MHz, and the following Instruction Class distribution for a program with 100 instructions:

Class 1:	**3 CPI**	**40%**
Class 2:	**5 CPI**	**20%**
Class 3:	**3 CPI**	**30%**
Class 4:	**1 CPI**	**10%**

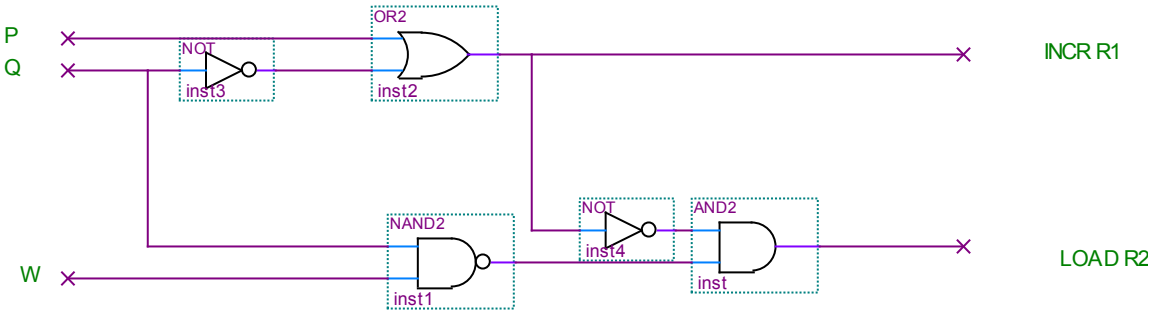
CPI = 3*0.4 + 5*0.2 + 3*0.3 + 1*0.1 = 3.2

E.T. = 100 * 3.2 / (500*10^6) = 640 ns

d) Draw the control logic (only) for the following RTL pseudo code:

If (P = 1 OR Q = 0) then R1 gets (R1 + 1)
Elseif (W = 1 NAND Q = 1) then R2 gets (R1 + R2)

Where P, Q, and W are the input signals to the control unit. (6pt)



Question 3 (15 marks):

a) Show the steps for doing **(- 8 x - 5)** using Booth's algorithm? Write final result. (10pts)

A	Q	Q_{-1}	M	Comments
00000	11011	0	11000	Initial Values

Result = AQ = 00001 01000 = 40

b) How many addition and how many subtraction operations are needed when using Booth's algorithm to multiply a number X by the multiplier **"11101001110b"**

Number of Addition Operations: _____2_____

Number of Subtraction Operations: _____3_____

Just count the pairs of "01" for addition and "10" for subtraction

Question 4: (15 marks)

a) Given the 32-bit pattern

1011	1111	1100	1000	0000	0000	0000	0000

What is the value in **decimal** if the above pattern is for:

I) Unsigned integer? 2pts

$2^{31} + (2^{30} - 2^{22}) + 2^{19} = 3{,}217{,}555{,}456$

II) Two's complement integer? 3pts
Sign bit is 1, negative

0100	0000	0011	1000	0000	0000	0000	0000

$= - (2^{30} + (2^{22} - 2^{19}) = - 1{,}077{,}411{,}840$

III) Single format floating point number? 5pts

Sign = 1, i.e. negative
Biased Exponent = $(2^7 - 2^0) = 127$
True exponent = 127 – 127 = 0
Fraction = $2^{-1} + 2^{-4} = 0.5625$

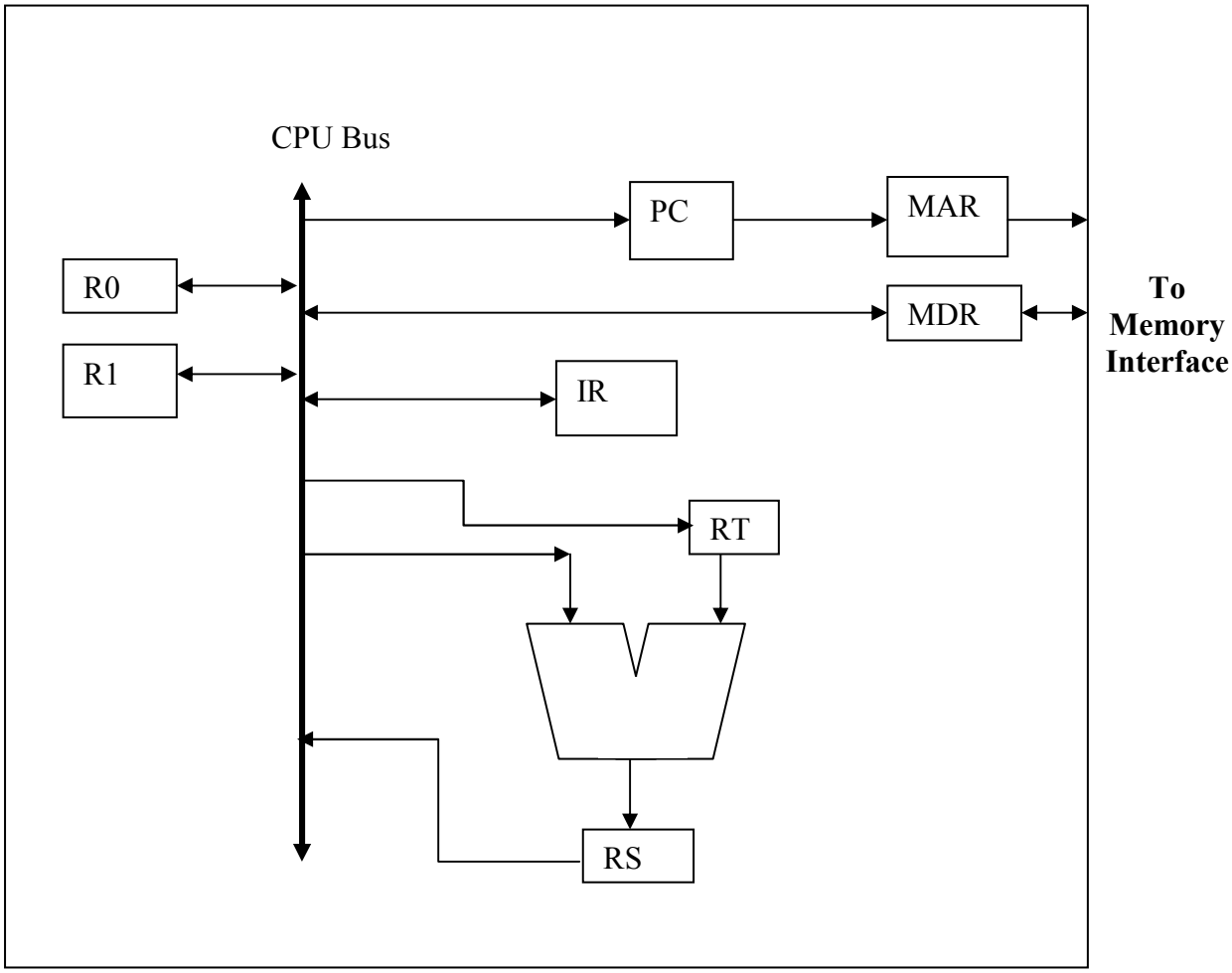
Value = - 1.5625 x 2^0 = -1.5625

b) Which is more difficult to implement; floating point addition or floating point division operations? Why?

Floating point Addition
Need alignment of exponents

Question 5: (10 marks)
Draw a block diagram of the data path for a CPU that has the following hardware components: 2 general purpose registers **(R0, R1)**, Program Counter **(PC)**, Instruction Register **(IR)**, an **ALU** that can perform logical and arithmetic functions, Memory Address Register **(MAR)**, Memory Data Register **(MDR)**, a register that temporarily holds one operand for the ALU **(RT)**, and a register to temporarily hold the result from the ALU **(RS)**.

Use a single CPU bus, drawn below, to interconnect the hardware resources.



Question 6 (15 marks):

A **4K x 16** memory, shown below, is used to store instructions set and data for a basic computer architecture based machine. The first instruction is stored at memory address location **FF0h**;

a) fill in the table below with the values for **PC**, **IR**, and **AC**? Initial values mean the values of the registers prior to fetching the first instruction from memory.

Opcode **1h** is to load AC from memory
Opcode **3h** is to store AC to memory, while
Opcode **5h** is to add to AC from memory.
(All numbers are in hex representation)

Instruction Phase	PC	IR	AC
Initial Values	FF0	--	--
After 1st Instruction Fetch	FF1	1FF3	--
After 1st Instruction Execution	FF1	1FF3	3402
After 2nd Instruction Fetch	FF2	5401	3402
After 2nd Instruction Execution	FF2	5401	8402

Memory Address	Instructions & Data
:	:
400	0 A C E
401	5 0 0 0
402	3 1 0 0
403	0 F F 1
:	:
FF0	1 F F 3
FF1	5 4 0 1
FF2	3 F F 1
FF3	3 4 0 2
:	:

b) Using the above memory organization, what is the value of the operand stored in memory if the instruction format indicated an **indirect memory access** with an **address field** value of **403h**?

5401

BIRZEIT UNIVERSITY

ENCS336 – First Exam

Summer Semester 08/09
Date: July 13, 2009

Student ID : _____

Student Name : Typical Solutions

Instructor: Abdel Salam Sayyad

Instructions:

- **You have 80 minutes to answer all questions, so budget your time carefully!**
- **Turn OFF your mobile**
- **To make sure you receive credit, please write clearly and show your work**

Question	Maximum	Your Score
1	20	
2	45	
3	10	
4	12	
5	15	
Total	102%	

Question 1: TRUE or **FALSE (**20 marks**)**

Score	

TRUE	**FALSE**	
○	○	Prior to executing an Interrupt Service Routine, the 8086 saves a copy of the instruction register (IR) to the stack.
○	○	In the FETCH phase, an instruction is transferred from memory to the Program Counter (PC).
○	○	After RESET, the 8086 will have a value of FFFF0h in the Code Segment (CS) register.
○	○	Number of address lines for a 256K x 16 memory organization is 16.
○	○	All Intel x86 family members share the same basic architecture in order to maintain code backwards compatibility.
○	○	In a typical instruction cycle, only the fetch phase requires access to main memory.
○	○	In 8086, after fetching an instruction, the Instruction Pointer (IP) is always incremented by two.
○	○	In 8086, after a PUSH instruction, the Stack Pointer (SP) is decremented by two.
○	○	After a CMP instruction, the Zero Flag will be equal to 0 if the two values are equal.
○	○	After a TEST instruction, the Zero Flag will be equal to 0 if the two values are equal.

Question 2: Multiple Choice (45 marks)

Score	

1. Reading and writing to the memory unit (RAM) takes place via:

a. the ALU and the register unit
b. the memory address and memory data registers
c. the program counter and the memory data register
d. the Program Counter and the Instruction Register
e. the write enable line

2. Given an ISA computer specifying a word size of 4 bytes, byte addressability, and an address space of 16 MB: What is the size of the PC register?

a. 8 bits b. 16 bits c. 24 bits d. 32 bits e. 16 Mbits

3. Given an ISA computer specifying a word size of 4 bytes, byte addressability, and an address space of 16 MB: What is the size of the IR?

a. 8 bits b. 16 bits c. 24 bits d. 32 bits e. 16 Mbits

4. The Program Counter register is:

a. a binary counter that keeps track of the number of instructions executed
b. a register that stores the next instruction to be executed
c. a control circuit that steps through a sequence of instructions
d. a register that stores the address of the next memory location to be written to
e. a register that stores the memory address of the next instruction

5. The purpose of the control unit is:

a. to store the list of instructions
b. to fetch the next instruction from memory & decode it
c. to control the ALU
d. to control access to memory
e. to clock the transitions between states of the whole microprocessor

6. DS=1000h ES=1200h CS=1300h SS=1400h BP=5500h BX=0300h SI=0200h DI=0300h. Consider the instruction **MOV [BX+SI], BP**

The content of BP register will be copied to:

a. Memory physical addresses 10500h,10501h
b. Memory physical addresses 10700h,10701h
c. Memory physical addresses 0500h,0501h
d. Registers BX and SI.
e. Registers DS, BX and SI.

7. The memory segment that holds the programs and procedures used by microprocessor is:

a. Code Segment
b. Data Segment
c. Extended Segment
d. Stack Segment
e. Data Segment and Extended Segment

8. If SP=FFEE BP=0000h SI=0000h DI=0000h DS=1500h ES=1100h SS=1600h CS=1400h IP=1200h , The microprocessor fetches its next instruction from the physical memory location:

a. 1200h **b.** 15200h c. 1400h d. 2600h e. 16200h

9. What is the effect of the following instruction? **MOV CX, [BP + 8]**

a. Add 8 to the contents of BP and store the sum in CX.
b. Add 8 to the contents of DS+BP and store the sum in CX.
c. Add 8 to the contents of BP, treat the sum as a memory address and store the contents at that address in CX.
d. Add 8 to the contents of the memory location whose address is stored in BP and store the sum in CX.
e. Add the contents of BP to the contents of memory address 8 and store the sum in CX.

10. One of the following is illegal instruction

a. MOVE CL,[BX]
b. POP AL
c. MOV WORD PTR [BX],AX
d. INC [DI]
e. MOV DS,AX

11. If AL=00000100b, BL=01000001b , then after executing the instruction

CMP AL, BL

The contents of AL and zero-flag bit are:

a. AL=00000100, ZF=0
b. AL=00000100, ZF=1
c. AL=00000000, ZF=0
d. AL=00000000, ZF=1
e. AL=01000101, ZF=0

12. Variable MESSAGE is defined as follows:

MESSAGE DW 10h, 122Fh, 12Eh

How many bytes does the variable MESSAGE occupy in memory?

a. 3
b. 4
c. 5
d. 6
e. 9

13. Moore's Law stated that the number of _____ on a chip would double every year.

a. Logic gates
b. Flip Flops
c. Transistors
d. Capacitors
e. All the above

14. when a processor executes a procedure call,

a. It pushes the content of IR (instruction register) onto the stack, and then changes the IR value.
b. It pushes the content of PC onto the stack, and then changes the IR value.
c. It pushes the content of PC onto the stack, and then changes the PC value.
d. It pushes the content of IR onto the stack, and then changes the PC value.
e. It pushes the content of AC onto the stack, and then changes the AC value.

15. The following instruction is assembled at physical memory address 01034H.

MOV BX, 2H

After execution, the instruction pointer (IP) had the value 0017H. Knowing that the CS register held the value 0102H, how many bytes in memory did the above instruction occupy?

a. 1 byte b. 2 bytes c. 3 bytes d. 4 bytes

Question 3: (10 marks)

Consider a computer system with memory of size 4096 locations, 1 byte each. Its instruction length is 16 bits and consists of op-code portion, addressing mode bit, and address/operand portion. Suppose that the computer uses only direct-memory and immediate addressing modes.

a. What is the maximum number of instructions that can be supported by this computer? Why?

Opcode bits = 16-12-1 = 3
Maximum number of operations = 2^3 = 8

b. If the ADD instruction with immediate value is used, what is the maximum unsigned value that can be added?

Maximum unsigned number = 2^12 -1 = 4095

Question 4: (12 marks)

Suppose that the AL register contains 95H, the CL register contains 02H, and the carry flag (CF) contains '1' just before each of the instructions below is executed (that is, don't accumulate the results of the following instructions, start fresh with 95H, 02H, and '1' each time). What will be the value in the AL register after each instruction?

```
ROL     AL, CL      ; AL = 01010110
RCR     AL, CL      ; AL = 11100101
SHR     AL, 1       ; AL = 01001010
SAR     AL, CL      ; AL = 11100101
```

Notes:

1. ROR: Logic Rotate Right
2. RCR: Rotate Right with Carry
3. SHR: Logic Shift Right
4. SAR: Arithmetic Shift Right

Question 5: (15 marks)

Table Q4 shows some current content of the main memory of an 8086 system.

Address	Hex data							
1000H	10	02	20	11	10	13	14	10
1008H	01	31	21	22	04	51	13	12
1010H	12	12	03	33	21	03	10	19
:								
2010H	10	11	12	10	14	15	17	16

Table Q4

Assume now we have DX=2006H, BX=0004H, SI=0002H and DS=0100H.

Determine which data is moved from which location to which location when the following instructions are executed.

a) MOV CX, [BX]

Source: Memory addresses 1004H and 1005H

Destination: Register CX

Data: 1310H

b) MOV BX, BYTE PTR [SI]

Source: Memory address 1002H

Destination: Register BX

Data: 20H

c) MOV [BX+SI+100CH], DX

Source: Register DX

Destination: Memory addresses 2012H and 2013H

Data: 2006H

Question (1) 16 point

- Program counter : incrementing counter that keeps track of the memory address of the instruction that is to be executed next. (True)
- Memory address register (MAR) - holds the address of a memory block to be read from or written to read from or written to. Memory data register (MDR) (True)
- Instruction register (IR) - a temporary holding for the instruction that has just been fetched from memory (True)
- Mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing. Improves process efficiency. (True)
- Data Bus width determines maximum memory capacity of system (False, Address bus)
- A system with Multiplexed buses has fewer lines but more complex control (True)
- In machine code each instruction has a unique bit pattern (True)
- Little Endian : In little endian, you store the most significant byte in the smallest address. (false, the least)

Select the correct Answer: (3 points)

1. Interrupts can be generated in response to
   a. detected program errors such as arithmetic overflow or division by zero
   b. detected hardware faults
   c. Input/Output activities
   e. b, c, and d
   f. a, b, and c

2. In order to execute a program instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How many memory access would be needed in this case to transfer a 32 bit instruction from memory to the CPU.
   a. 1 b. 2 c. 3 **d. 4**

Question (2) 6 point

Short answer questions

a) List differences between CISC and RISC computers (up to 3 differences) . **(6 points)**

1) Larger number of instructions 2) Variable length instruction format 3) More addressing modes 4) complexity in design

b) Is this true : Transistors, Resistors and Capacitors are the three principal constituents of a computer system **(2 point)**

True

c) What are the main two approaches to deal with multiple interrupts? **(4 point)**

- The First approach is to disable interrupts while an interrupt is being processed.
- The Second approach is to define priorities for interrupts and to allow an interrupt to higher priority to cause a lower-priority interrupt handler to be itself interrupted.

Question (3) 6 point

Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address.

a. What is the maximum directly addressable memory capacity (in bytes)? **(2 point)**

32-8=24 Byte
Address : 2^{24}= 16MB

b. Discuss the impact on the system speed if the microprocessor bus has **(4 point)**

1. A 32-bit local address bus and a 8-bit local data bus, or

If local address is 32 bits then the whole address will be transferred at once, however because the local data bus is 16 bit then we need 4 clock cycles. .

2. A 16-bit local address bus and a 16-bit local data bus.

16bit of address bus can't access the whole memory, so more complex memory interface control is needed to latch the first part of the address and then for the second part. So the microprocessor need 2 ccs to fetch the instruction.

Question (4) 6 point

A PC-relative mode branch instruction is stored in memory at address 620_{10}. The branch is made to location 530_{10}. The address field in the instruction is 10 bits long. What is the binary value in the instruction? **(6 point)**

(PC+1) +Relative address =Effective address
Relative address = -621+530 =-91
Converting to the twos complement representation, we have : 1110100101

Question (5) 7 point

Assume a stack-oriented processor that includes the stack operations PUSH and POP. Arithmetic operations automatically involve the top one or two stack elements. Begin with an empty stack. What stack elements remain after the following instructions are executed (fill the table)? **(7 point)**

Instruction	Stack (top on left)
PUSH 9	4
PUSH 7	7,4
PUSH 8	8,7,4
ADD	15,4
PUSH 10	10,15,4
SUB	5,4
MUL	20

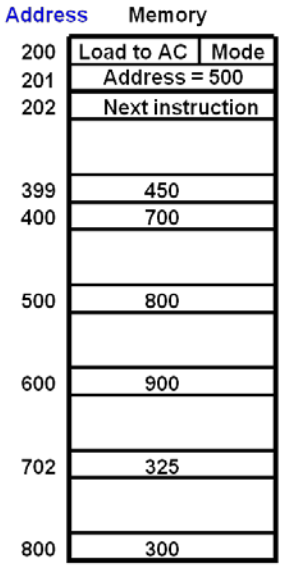
Question (6) 10 point instructions as shown in the table below

Given the following memory section, and 4 registers as shown below, fill the effective address and the content of the accumulator as shown in the table.

Addressing Mode	Effective Address		Content of th Accumulato
Direct address	500	AC ← (500)	800
Immediate operand	-	AC ← 500	500
Indirect address	800	AC ← ((500))	300
Relative address	702	AC ← (PC+500)	325
Indexed address	600	AC ← (RX+500)	900
Register	__	AC ← R1	400
Register indirect	400	AC ← (R1)	700
Autoincrement	400	AC ← (R1)+	700
Autodecrement	399	AC ← -(R)	450

PC = 200

R1 = 400

XR = 100

AC