Birzeit University

Department of Electrical and Computer Engineering

ENCS 336 – Computer Organization & Assembly Language

Midterm Exam - First Semester 2016/2017

17/11/2016

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Instructions:

1) This exam is closed-book, closed-notes, and closed-cellphone.
2) One size A4 sheet of notes is allowed.
3) Exam duration is 70 minutes.
4) Answer the questions on this exam paper.

Student name: Typical Solutions Student Number: .

Question	Full Mark	Your Mark
1	6	
2	7	
3	6	
4	8	
5	3	
Total	30	

Question 1: (6 marks)

The following statements are incorrect. Explain why.

A. Instruction Set design and memory addressing are issues of computer organization.

They are issues of computer architecture, since they are visible to the programmer.

B. Moore's law states that number of vacuum tubes in integrated circuits will double every year.

Transistors. Not vacuum tubes.

C. As the density of integrated circuits increases, power consumption increases because of the larger number of transistors.

Power consumption decreases because of the shorter paths between transistors.

D. The memory device sends an interrupt signal to the CPU whenever it is ready to send and receive data.

Interrupt signals only come from I/O devices. Not memory devices.

E. The data bus is used to transfer data between the memory and CPU, while the address bus is used to load instructions from memory to the CPU.

The address bus transfers addresses. Not instructions.

F. The instruction pointer (IP) stores the address of the current instruction being executed by the CPU.

The next instruction. Not the current instruction.

Question 2: (7 marks)

Consider a hypothetical microprocessor generating a 26-bit address and having a 32-bit data bus. This microprocessor supports 14 different operations (instructions), and the memory is byte-addressable.

A. What is the maximum memory size that the processor can access?

a. 256 MB b. 128 MB c. 64 MB d. 32 MB e. 16 MB

B. What is the minimum length required for the opcode?

a. 26 bits b. 14 bits c. 8 bits d. 5 bits e. 4 bits

C. Now suppose that the microprocessor supports the following opcodes:
(0110 = load to AC, 1001 = add to AC, 0011 = store to memory), and that each instruction includes a 26-bit memory address field. Write the machine code for the following instructions:

Instruction	Machine code
Load the contents from address 2ABCD00 to AC	1AABCD00
Add the contents from address 2ABCD04 to AC	26ABCD04
Store AC to address 6EF004	0C6EF004

Question 3: (6 marks)

Complete the following code fragment such that the program takes 10 characters from the keyboard. Each character is compared to the corresponding character in array1; if they are equal then the corresponding element of array2 is set to "Y", otherwise it is set to "N".

```
.model small

.stack 100h

.data
array1 db "ABCDEFGHIJ"
array2 db 10 dup(?)

.code
mov ax, @data
mov ds, ax

mov si, offset array1
mov di, offset array2
mov cx, 10
mov ah, 1

L1:
Int 21h
cmp bl, [si]
jne L2
mov [di], 'Y'
jmp L3
L2:
Mov [di], 'N'
L3:
inc si
inc di
loop L1

mov ah, 4ch
int 21h
end
```

Question 4: (8 marks)

In an 8086 computer system, the initial status of registers and memory locations is as follows:

AX = 2; BX = 45H; CX = 0AH; DX = 0; SI = 5200H; IP = 100H; CS = 1EE2H; DS = 1A34H

Address	Content
1F540H	F0H
1F541H	0FH
1F542H	ABH
1F543H	45H
1F544H	00H
1F545H	24H
1F546H	8CH
1F547H	88H

For each of the following questions, always begin from the status above; i.e. all registers and memory locations are reset to the above values before each execution.

A. What is the physical address of the next instruction to be executed?

   a. 100H b. 5200H c. 1EE200H d. 1FE20H e. 1EF20H

B. After the instruction **MOV BX, [SI]** is executed, the value in BX will be:

   a. 00H b. F0H c. 0FH d. 0FF0H e. F00FH

C. The command **CMP BX, AX** will result in:

   a. BX = 45H, AX = 45H, ZF (Zero Flag) = 0
   b. BX = 2, AX = 2, ZF (Zero Flag) = 0
   c. BX = 45H, AX = 45H, ZF (Zero Flag) = 1
   d. BX = 45H, AX = 2, ZF (Zero Flag) = 0
   e. BX = 45H, AX = 2, ZF (Zero Flag) = 1

D. The following code

```
L4:   ADD  AX, 20
      LOOP L4
```

   Will result in:

   a. AX = 40 b. AX = 202 c. AX = 402 d. AX = 102 e. AX = 42

Question 5: (3 marks)

Explain why the following commands will result in syntax errors:

a. mov ax, D3H

D3H is a hexadecimal number. It must be written as 0D3H.

b. xor SI, BL

SI is 16-bit long, whereas BL is 8-bit long. This is a size mismatch.

c. mov ds, @data

@data must be moved to a register like AX first, and then AX can be moved to DS.