BIRZEIT UNIVERSITY

ENCS336 – Second Exam

2nd Semester 08/09
Date: May 14th, 2009

Student ID : _____

Student Name: __typical solutions_____

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Instructions:

- **You have 80 minutes to answer all questions, so budget your time carefully!**
- **Turn OFF your mobile**
- **To make sure you receive credit, please write clearly and show your work**

Question	Maximum	Your Score
1	24	24
2	36	36
3	16	16
4	12	12
5	12	12
Total	100%	100%

Question 1: True or False (24 marks)

Score	

	True	False	
a)	O	O	DRAM is more popular than SRAM because it can be accessed faster than SRAM.
b)	O	O	To properly handle an external interrupt, the current instruction must be suspended then restarted.
c)	O	O	Larger caches have better hit rates but longer latency.
d)	O	O	Multi-level caches generally operate by checking the smallest Level 1 (L1) cache first; if it hits, the processor proceeds at high speed.
e)	O	O	Increasing the disk size will increase the average seek time.
f)	O	O	Programmable ROM types (PROM, EPROM, EEPROM, and Flash) are all written (programmed) using electricity.
g)	O	O	Both DRAM and EPROM are volatile memory.
h)	O	O	The refresh cycle in SRAM causes slow access to data.
i)	O	O	In interrupt-driven I/O the CPU has to check the status register periodically to know if the operation is accomplished.
j)	O	O	It is possible to interrupt an interrupt service routine (ISR).
k)	O	O	Cache memory is implemented using EPROM technology.
l)	O	O	SRAM consume more power than DRAM.

Question 2: Choose the right answer (36 marks)

Score	

1. A disk drive has 3 double-sided platters. The drive has 300 cylinders. How many tracks are there?

   A. 600 B. 900 C. 1800 D. 3600 E. 300

2. Cache memory refers to
   A. cheap memory that can be plugged into the mother board to expand main memory
   B. fast memory typically present on the processor chip that is used to store recently accessed data
   C. a reserved portion of main memory used to save important data
   D. a special area of memory on the chip that is used to save frequently used constants
   E. Stack memory

3. Which one has the fastest access time?
   A. Magnetic tape
   B. Magnetic disk
   C. Main memory
   D. Cache
   E. Flash disk

4. Usually, cache memory is:
   A. small SRAM
   B. Large SRAM
   C. small DRAM
   D. SDRAM
   E. DRAM

5. One of the following is not true:
   A. Both Static RAM and Dynamic RAM don't save data if the power shut down
   B. Both Static RAM and Dynamic RAM must have refreshing circuit,
   C. Static RAM is more expensive (per bit) because a latch/flip-flop takes more space than a capacitor/transistor.
   D. Static RAM is faster than dynamic RAM
   E. Typically, DRAM is used as main memory in computer system, while Static RAM is used in cache.

6. Consider a 256K x 1-bit SRAM chip. The memory module is organized as rows and columns. How many address lines are needed?
   A. 8
   B. 9
   C. 18
   D. 256
   E. 512

7. How many 256K X 8 DRAM modules are needed to implement 1M X 16 DRAM module?
   A. 2
   B. 4
   C. 8
   D. 16
   E. It is not possible , we only can implement it using 256K X 16 modules

8. A system uses memory-isolated I/O addressing mode, if there are 8 address lines, then the system can support up to:
   A. 8 memory locations , and 8 I/O locations
   B. Total 512 memory and I/O locations
   C. Total 256 memory and I/O locations
   D. 512 memory locations , and 512 I/O locations
   E. 256 memory locations , and 256 I/O locations

9. The _____ of a disk is the time needed to position the read/write head over the correct track.
   A. Rotationally delay
   B. transfer speed
   C. frequency
   D. Access time
   E. Seek time

10. A disk with spindle speed =7500 rpm. Average seek time = 4.5ms, 512-byte sectors. What is the maximum rotational delay?
   A. 8ms
   B. 4ms
   C. 4.5ms
   D. 0.13ms
   E. 0.26ms

11. One of the following is not true:
   A. The direct mapped cache is the simplest form of cache and the easiest to check for a hit
   B. The fully associative cache has the best hit ratio
   C. The fully associative cache suffers from problem of involving searching the cache
   D. In N-way set associative cache, Hit ratio increase as N Increases
   E. Direct mapped, fully associative and set associative caches need block replacement algorithms

12. A system uses direct-mapped cache. Imagine the processor needs 3 different addresses (call them X, Y and Z) in the following sequence (X, Y, X, Y, Z, X, Y, Y, Y, Z). Suppose both X and Y map to the cache line 0, Z maps to cache line 3. The hit ratio is:
   A. 0.30 B. 0.70 C. 0.50 D. 0.20 E. 0.90

Score	

Question 3: (16 marks)

Consider a **Seagate Barracuda** hard disk with the following parameters:

- Number of sectors per track = 600 sectors
- Number of bytes per sector = 512 bytes
- Number of tracks per one platter = 29851 tracks
- Number of platters = 2 single-sided platters
- Spindle speed = 7200 rpm
- Average seek time = 9.5 ms

1. What is the number of cylinders in this hard disk? **[2 marks]**

# of cylinders = # of tracks = 29851 cylinders

2. What is the number of tracks per one cylinder? **[2 marks]**

Number of tracks per one cylinder = number of platters = 2

3. What is the total capacity of the hard disk? **[4 marks]**

Capacity = # of platters * # of tracks/platter * # of sectors/ track * # of bytes/sector
= 2 * 29851 * 600 * 512
= 18340454400 bytes

4. What is the average rotational delay? **[4 marks]**

Average rotational delay = 1/ 2r = 1 / 2 (7200/60) = 4.17 ms

5. What is the total time needed to read data of 10 Kbytes stored on 20 adjacent sectors? **[4 marks]**

= seek time + Rotational delay + transfer time
= 9.5 ms + 4.17 ms + b/rN
= 9.5 ms + 4.17 ms + (10 * 1024)/ (7200/60) * (600 * 512)
= 9.5 ms + 4.17 ms + 0.3 ms
= 13.97 ms

No partial marks.

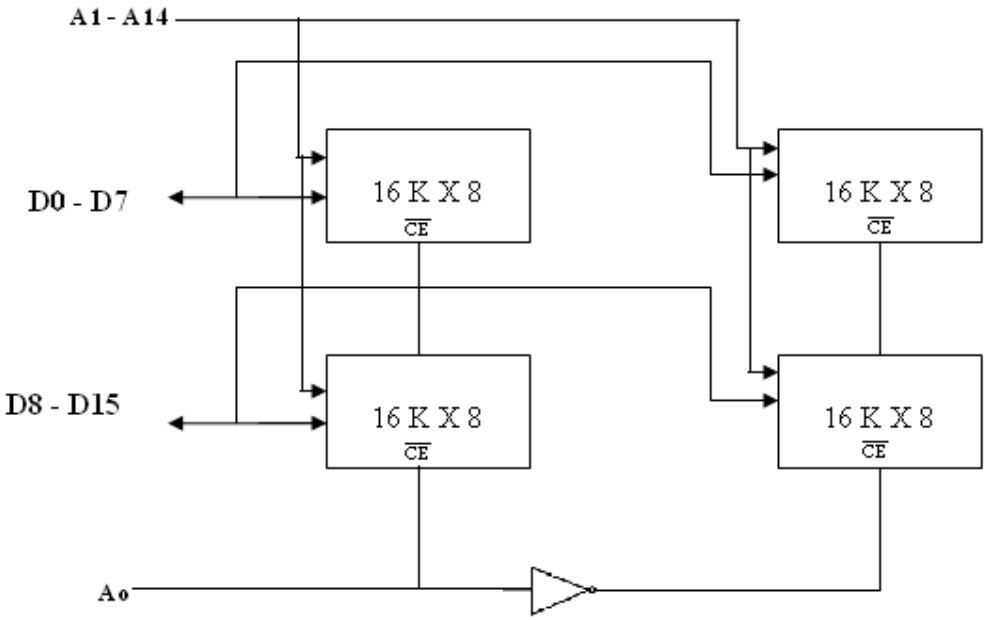
Score	

Question 4: (12 marks)

Consider a 16-bit processor that requires 64 Kbytes main memory. Design a memory module for the processor using only 16-Kbyte memory chips organized as 16K X 8 bit.

Solution:

- **Memory locations = 32 K locations, 15 address lines are needed (A0 – A15)**
- **Available chips 16 Kbytes (16K X 8), we need 4 chips, each needs 14 address lines**



- 2 marks for # chips = 4
- 4 marks for connecting 14 address lines to all chips
- 4 marks for connecting the data lines correctly
- 2 marks for decoding one address bit to drive chip selects.

- No partial marks.

Score	

Question 5: (12 marks)

Consider a computer system with the following characteristics:

1. 16-Mbyte main memory,
2. 256-Kbyte cache memory,
3. Byte Addressable,
4. 8 bytes per cache line.

Suppose that the cache memory is to be mapped as 4-way set associative.

a. How many lines are there in the cache memory?

Lines = (256 KBytes) / (8 Bytes/line) = 32 K lines [3 marks]
= 32 * 1024 lines
= 32768 lines

b. How many sets are there in the cache memory?

Sets = (32 * 1024 lines) / (4 lines/set) = 8 * 1024 = 8192 sets [3 marks]

c. How many blocks are there in main memory?

Blocks = (16 MBytes) / (8 Bytes/block) = 2 M blocks [3 marks]

d. How long (in bits) is the Tag field?

Total memory address bits = $\log_2$ (16M) = 24 bits
Set bits = $\log_2$ (8192) = 13 bits
Word bits = $\log_2$ (8) = 3 bits

Tag bits = total bits – set bits – word bits = 24 – 13 – 3 = 8 bits [3 marks]

No partial marks.

key

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Computer Systems Engineering Department
Computer Organization – ENCS238
Second Exam

Name: key **ID:** **Section: 1 2 3**

Question 1: [30] (Multiple choice; 2 pts each)

1. CPU checks for an interrupt signal during
   (A) Starting of last Machine cycle
   (B) During execution cycle
   (C) Operand Fetch cycle
   (D) Instruction fetch cycle

2. In 8086 the Overflow flag is set when
   (A) the sum is more than 16 bits
   (B) Signed numbers go out of their range after an arithmetic operation
   (C) Carry and sign flags are set
   (D) During subtraction

3. Which of the following is an illegal instruction
   (A) MOV AX, 25000 (B) DEC AL
   (C) AND BX, CX (D) MOV DS, 7000H

4. In a 16-bit floating point format with 6 bits exponent, and 9-bits mantissa, the value of the exponent for the binary number 101.100×2^3
   (A) 34 (B) 5
   (C) 36 (D) 67

5. Which of the following variables uses the most amount of RAM:
   (A) x db 255 **(B)** y db 80 dup('Z')
   (C) z dw 50 dup(0) **(D)** small dd 40 dup(0)

6. The result of mov al, 65 is to store
   (A) 0100 0010 in al **(B)** ASCII code of 'A' in al
   (C) store 42H in al **(D)** store 1000 0001 in al

7. The effect of the following instructions

```
push ax
add ax, 4
pop bx
mov cx, ax
push bx
pop ax
```

on the ax register is

(A) leave it with its original value **(B)** add 4 to it
(C) clear it **(D)** double it

8. To copy the hexadecimal number A to the bh register you write

(A) mov 0bh, ah **(B)** mov bh, 0ah
(C) mov bh, ah **(D)** mov bh, [ah]

9. Given that al contains the ASCII code of an uppercase letter, it can be converted to lowercase by

(A) add al,32 **(B)** sub al, 32
(C) or al, 1101 1111 **(D)** and al, 0010 0000

10. The word size of an 8086 processor is

(A) 8 bits (B) 16 bits
(C) 32 bits (D) 64 bits

11. One of the following instruction is illegal:

(A) mov al,[bx] (B) mov [bx],[2000]
(C) inc [bx] (D) add cx,[200]

12. A computer system has 64MB of memory (Byte addressable), the minimum size of MAR

(A) 24 bit (B) 8 bit
(C) 26 bit (D) 16 bit

13. Which register will be affected by the instruction **MUL BX**

(A) BX (B) AX
(C) DX (D) Both AX and DX

14. The bp register is typically used for accessing

(A) strings (B) memory
(C) stack (D) data segment

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	B	D	C	D	B	A	B	A	B	B	C	D	C	X

Question 2: [15]

Consider a 16-bit floating-point format given in Figure below:

Sign (1 bit)	Exponent (7 bit)	Significant (8 bit)

a) What is the absolute maximum and absolute minimum normalized numbers that can be represented in this floating-point format? C5PTS3

Bias = $2^6 - 1 = 63$

max. exponent = 126, max significant = FFH

abs. Max = $\pm 1.11111111 \times 2^{63}$

min. exp = 1 $\Rightarrow 1 - 63 = -62$

min. sig. = 00H

So, abs. min = $\pm 1.00000000 \times 2^{-62}$

b) Let A= $(BD70)_H$ and B = $(42C8)_H$ are two floating-point numbers, expressed in hexadecimal. Let C = A + B, find the representation of C in 16-bit format given in figure above (show how the floating point calculations are performed step by step)[10] Bias = 63

A = 1 011 1101 | 0111 0000
exp. sig.

exp. = 61 − 63 = −2

$A = -1.0111 \times 2^{-2}$

$A = -0.00010111 \times 2^{3}$

B = 0 | 1000010 | 11001000
exp. sig.

exp = 66 − 63 = 3

$B = +1.11001 \times 2^{3}$

1.1100 1000 00
− 0.0001 0111 1
+1.1011 1001

$C = +1.10111001 \times 2^{3}$

sign = 0

exp. = 3 + 63 = 66 = $(1000010)_2$

sig. = 10111110

in 16-bit Floating-point

C = 0 | 1000010 | 10111100

4 2 B E

$C = (42BE)_H$

or Rounded to

0/1000010/10111101

42BDH

Question 3:[15]

a) What is interrupt? [2pts]

Mechanism by which other Modules (e.g I/O) may interrupt normal sequence of processing to improve process efficiency.

b) Mention three sources that cause an interrupt? [3 pts]

1) I/O (external signals such as from printer)
2) Program (overflow, divide by zero)
3) Timer ⓦ HW failure.

c) Consider a system with five I/O devices: D1, D2, D3, D4 and D5. Interrupts from D1 and D2 has the same priority = 2, D3 has priority = 4, and D4 has priority = 7, and D5 has priority = 5. A user program begins at time t = 0:

- at t = 10 D2 interrupt occurs and it needs 20 sec to be handled
- at t = 15 D4 interrupt occurs and it needs 15 sec to be handled
- at t = 20 D1 interrupt occurs and it needs 10 sec to be handled
- at t = 25 D3 interrupt occurs and it needs 25 sec to be handled
- at t = 30 D5 interrupt occurs and it needs 10 sec to be handled

$0 \rightarrow 10$ main prog.
$10 \rightarrow 15$ D2
$15 \rightarrow 30$ D4
$30 \rightarrow 40$ D5
$40 \rightarrow 65$ D3
$65 \rightarrow 80$ D2
$80 \rightarrow 90$ D1

Using nested multiple interrupts, complete the table below: [10pts]

Device	Interrupt handling start time	Interrupt handling complete
D1	t = 80	t = 90
D2	t = 10	t = 80
D3	t = 40	t = 65
D4	t = 15	t = 30
D5	t = 30	t = 40

Question 4: [20]

a) Identify the operand addressing mode used in each of these instructions: [5 pts]

1) AND DX,AX ___Register Addressing Mode. (AM)___

2) JMP TABLE[BX] ___Based A.M. (mem. Reg. Indirect).___

3) ADD DX,15 ___Immediate A.M.___

4) CMP WORD PTR [BX+DI],10 ___Based-Indexed A.M. (mem. Reg. Indirect)___

5) MOV IVAL[DI+4],CX ___Indexed with displacement A.M. (mem. Reg. Indirect)___

b) Assume (all values are in hex) [15 pts]

AX=0000 **BX**=00050 **CX**=0003 **DX**=0000 **SI**=0050 **DI**=0000
CS=2000 **SS**=4000 **DS**=5000 **ES**=2000 **SP**=3000 **BP**=00050
IP=100

```
        mov cx,7
L:      Inc DI
        Loop L ; if cx !=0 then dec cx and goto L
        or AX,[BX+2]
        Lea DX,[SI]
        POP SI
```

get 16-bit then Inc SP by two.

42FFF	12
43000	34
43001	56
43002	78
...	....
5004F	AA
50050	BB
50051	CC
50052	DD
...	...

i) What is the physical address of the next instruction to be executed? [2pts]

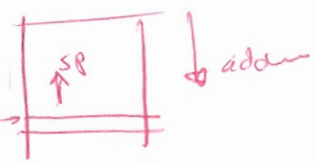
$CS*10h+IP = 20100_H$

20000
+ 100
20100

ii) What is the lowest possible address of the stack segment? [2pts]

Lowest address when SP = FFFFH

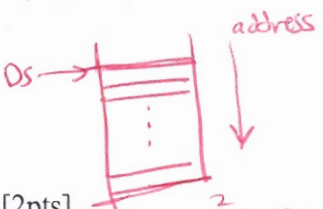
So, lowest physical address = SS*10h + FFFFH = 4FFFFH



iii) What is the highest possible address of data segment? [2pts]

Highest address when offset = FFFFH.

Highest physical address = DS*10h + FFFF = 5FFFFH



iv) What is the SP and SS after the two instructions push AX push BX: [2pts]

SP = SP - 4 ⇒ SP = 2FFCH

SP = 2FFCH SS = 4000H

2 15 15 16
3000
- 0004
2FFC

v) What is the physical address of the source operand of the fourth instruction? [2pts]

DS*10h + BX+1 = 50000 + 0050 + 1 = 50051H

vi) What is the new value of the affected registers after executing these instructions? [5pts]

CX = 0000H
DX = 0050H
DI = 0008H
SI = 3412H
AX = DDCCH

Question 5: [20]

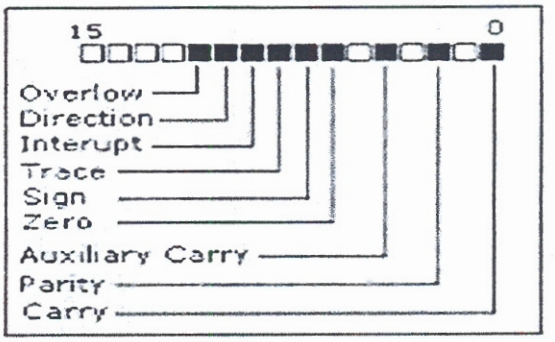
a) Show how the AL and Flags are affected by

```
Mov AL, 0BBH
ADD AL, 0CCH
```

AL= 87H CF= 1 OF= 0 ZF= 0 SF= 1

b) Given the Flags register in the following figure, write a set of instructions for setting the direction flag (DF) without changing the other flags and without using the instruction **STD.**

```
pushf
popAx
OR AX, 0400H
push AX
popf
```



c) What will be the value in AX after executing the following instructions? Give the answer in both hexadecimal and binary.

```
mov al, 15
mov ah, 15
xor al, al
mov cl, 3
shr ax, cl
add al, 90h
adc ah, 0
```

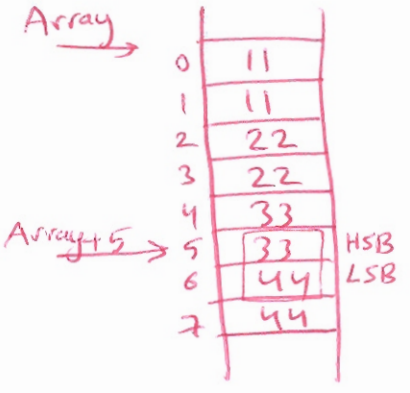
AX= (0270)(H) AX=(0000001001110000)B

d) What will be the value in AX after executing the following instructions? Assume that DS and ES are set up appropriately to access the variable 'Array'. Give the answer in hexadecimal:

```
Byte                1 0  3 2  5 4  7 6
Array   dw          11 11h, 22 22h, 33 33h, 44 44h

mov bx, 1
mov si, 6
mov ax, Array[bx][si-2]
```

AX = (3344)H



Birzeit University

Computer Systems Engineering Department

Computer Organization- ENCS 238

First Exam, May, 6, 2010

2nd semester, 2009/2010

(2 hours)

Section 1: Abdalkarim Awad **Section 2: Mohammad Abu- Ayyash**

Section 3: Aziz Qaroush

Name: **ID:**

Part One (True or False) (20Marks):

1	Given Ax=FFEE BX=7777 the instructions *cmp AX, BX* followed by *JGE L1* will change the IP to the value associated with L1 (i.e go to L1)	**F**
2	Hit ratio measures the expected probability of data being found in main memory.	**F**
3	Write-through cache reduces the number of write operations to main memory	**F**
4	Direct mapped, fully associative and set associative caches need block replacement algorithms	**F**
5	In the LRU (Least Recently Used) replacement algorithm, the data that has been in cache memory the longest time is replaced.	**F**
6	The access method used in EPROM is the Random Access	**T**
7	add *AL, [2000]* is illegal 8086 instruction	**F**
8	The instruction *mul Al, 20H* is illegal 8086 instruction	**T**
9	Both DRAM and SRAM need refresh	**F**
10	The instruction *Mov AX,[DX]* is a legal 8086 instruction	**F***

* DX, AX and CX can't be used as pointers to the data segment. We can us BX (i.e. Mov Ax,[BX] is legal)

Part Two (Assembly): (35 Marks)

1. Assembly languages are difficult for many reasons such as difficult to read, very difficult to debug, …. But still it has many advantages over high level languages. Give three of these advantages. (5 Marks)

   1 Assembly program size is smaller than high level languages
   2 Programs in assembly language will be executed faster than program in high level languages
   3 It access the hardware more efficient.

2. Write a complete assembly program that reads a key from the keyboard and if this key is a number then print on the screen the messages "A number has been pressed" else it print the messages "a non-number has been pressed". You may need the following information (10Marks)

```
.model small
.stack 100
.data
m1 db " A number has been pressed$"
m2 db " A non- number has been pressed$"
.code
mov ax,@data
mov ds,ax

mov ah,1
int 21h

cmp al,"0"
jb notnumber
cmp al,"9"
ja notnumber

lea dx,m1
mov ah,9
int 21h
jmp exit1

notnumber:
lea dx,m2
mov ah,9
int 21h

exit1:
mov ah,4ch
int 21h
end
```

   - ASCII codes for digits 0-9 are 30H-39H
   - For display use service 6H (i.e., AH=6H) of Int 21h (DOS interrupt), where the value to be displayed is placed in DL. Or service 2H (i.e., AH=2H) where the value to be displayed is placed in DL. And service 1H to read from the keyboard where the ASCII value of the inserted key will be in AL.

3. Assume(all values are in hex) (10 Marks)

AX=0000 BX=00050 CX=0003 DX=0000 SI=0050 DI=0000
CS=2000 SS=4000 DS=5000 ES=2000 SP=3000 BP=00050
IP=100

42FFF	12
43000	34
43001	56
43002	78
…	….

5004F	AA
50050	BB
50051	CC
50052	DD
…	…

```
Mov cx,7
L:
Inc DI
Loop L
or AX,[BX]      ;
Lea DX,[SI]     ;
POP SI
```

a. What is the physical address of the next instruction to be executed?

CS*10+IP
20000 +100=20100

b. What is the physical address of the source operand of the fourth instruction?

DS*10+BX
50000+50=50050

c. What is the new value of the affected registers after executing these instructions?

AX: CCBB CX:0000 DX:0050 SI:5634 DI:0007 SP:3002 IP:N/A

d. What is the physical address of the sources operand in the instruction mov DX,[BP+5]

SS*10+BP+5
40000+50+5=40055

Note that **SP & BP are two pointers associated with SS**. SP points to the top of stack, and BP points to any location we required in stack segment.

e. What is the SP and SS after the two instructions push AX push BX

SS:4000 SP 2FFE

4. Show how the AL and Flags are affected by (5 Marks)

```
Mov AL, 0BBH
ADD AL,0CCH
```

AL= 87 CF=1 OF=0 ZF=0 SF=1

5. Conditional jump (i.e JZ , JNZ…) allow relative range of only +127/-128 bytes form their current location. Knowing that unconditional jump does not have this limitation, show how to implement JZ L1 where L1 is located out side the +127/-128 range? (5 Marks)

```
JNZ skip
Jmp L1
```

Skip:

Part Three (Cache & Internal Memory): (45 Marks)

1. What is the performance advantage of using a write-back cache over a write-through cache? (4Marks)

2. Assume that we have 32-bit processor and it is byte-addressed (i.e. addresses specify bytes). Suppose that it has two way set-associative 512-byte cache, (16 bytes) cache lines (blocks), and uses LRU replacement.

   a. Split the 32-bit address into "tag", "set", and "word" pieces. Which address bits comprise each piece? (6 Marks)

# of words in each line = 16, need 4 bits to represent the word

# of lines = 512/16 = 32 lines

# of sets = # of lines/2 = 16, needs 4 bits to represent the set

The remaining bits of 32 bits used to represent Tag which is 32-4-4 = 24 bits

TAG: 24 bits	SET: 4 bits	W: 4 bits

   b. How many sets does this cache have? Explain. (3Marks)

   c. Below is a series of memory read references set to the cache from part (a). Assume that the cache is initially empty and classify each memory references as a hit or a miss. *Hint: start by splitting the address into components.* (12 Marks)

Address	Set Number	Hit/Miss?
0x007	*S0 / B0*	*M*
0x017	*S1 / B1*	*M*
0x104	*S0 / B1*	*M*
0x023	*S2 / B0*	*M*
0x203	*S0 / B0 LRU*	*M*
0x10F	*S0 /B1*	*H*

Address 007= 0 0 0 0 0 0 0 0 0 1 1 1

This means set 0 ⟹ 0 mod 16 = 0, (miss) we place this block in block 0 of the set 0 in the cache.

0X10F is hit, because this address and 0X104 address are found in the same block (same Tag "1").

d. Calculate the miss rate and hit rate. (5Marks)

Miss rate = 5/6

Hit rate= 1/6

3. Consider a system with cache, main memory and disk (or secondary memory) with the following parameters. It takes 10 ns to access cache, 100ns to access RAM and 10μs to access disk. The cache miss rate is 3% while miss rate in RAM is 20%. Estimate the average access time. (5Marks)

Ta = 0.97 * 10ns + 0.03(0.89 * 100ns + 0.11 * 10μs) =

97% of data is found in the cache.

3% of data is found out of the cache: 89% of this 3% data is in RAM, 11% in disk

(Note that access time is the "total time" to get the valid data. For example, RAM access time is the total time to get data from RAM including checking the cache)

4. Consider 8-bit processor that requires 64 Kbytes main memory. Design memory module for the processor using only 8 Kbytes memory chips organized as 16K X 4 bit. Draw your design. (10 Marks)

Solution:

- **Memory locations = 64 K locations, 16 address lines are needed (A0 – A15)**
- **Available chips 8 Kbytes (16K X4), we need 8 chips, each needs 14 (A2 –A15) address lines.**
- **The memory modules organized as four groups (banks) each contains two chips.**
- **A0 & A1 used to select one of the four groups. Use 2-to-4 decoder**

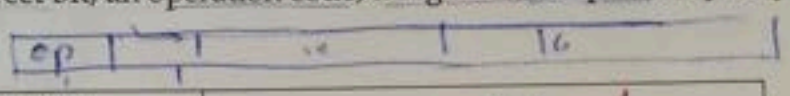
Question 2 (10 points)

What is the 8-bit results after performing each of the following shift operations.

Arithmetic Shift Left of (11110010)	(11100100)
Circular shift left of (11110010)	11100101
Logical shift left of (11110010)	11100100
Arithmetic shift right of (11110010)	11111001
Logical shift right of (11110010)	01111001

Question 3 (10 points)

A computer uses a memory unit with 1K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 16 registers, and an address part.



How many bits are there in the register code part	4
How many bits are there in the address part	12
How many bits are there in the data inputs of the memory	2^{16}
How many bits are there in the operation code part	2
How many bits are there in the address inputs of the memory	10

Question 4 (10 points)

A digital computer has a common bus system for 32 registers of 64 bits each. The bus is constructed with multiplexers.

How many multiplexers are there in the bus	64
How many selection inputs are there in each multiplexer	5
How many 3-state buffers are needed to reconstruct the bus using decoders and 3-state buffers	32X64
How many decoders are needed to reconstruct the bus using decoders and 3-state buffers	1
What the size of decoder(s) needed to select one destination register (for writing bus into a register)	5X32