BIRZEIT UNIVERSITY

Computer Organization and architecture (ENCS238)
First Exam

Fall Semester 2013/2014 **Date**: 21/10/2014
Instructor: Abualsoud Hanani **Time allowed**: 75 minutes

Name: _____ **ID:** _____.

Instructions:

- **You have 75 minutes, budget your time carefully!**
- **Turn OFF your mobile.**
- **To make sure you receive credit, please write clearly and show your work.**

Question	Maximum	Mark	Course Outcome
1	30		
2	10		
3	10		
4	10		
5	10		
6	10		
7	10		
Total	90		

Question 1 (30 marks, 2 pts each)

1. Virtually all computer designs are based on the von Neumann architecture. A high level view of this architecture has the following three components:
   (A) Buses, memory, input/output controllers (B) Hard disks, floppy disks, and the CPU
   (C) Memory, the CPU, and printers (D) memory, input/output modules, and the CPU

2. Any computer must at least consists of
   (A) Data bus (B) Address bus
   (C) Control (D) All of the above

3. Word 20 contains 40 Word 30 contains 50
   Word 40 contains 60, Word 50 contains 70

   Which of the following instructions **does not** load 60 into the Accumulator

   (A) Load immediate 60 **(B)** Load direct 30

   (C) Load indirect 20 **(D)** both (A) & (C)

4. Computers use addressing mode techniques for _____.
   (A) Giving programming versatility to the user by providing facilities as pointers to memory counters for loop control

   (B) Reducing number of bits in the field of instruction

   (C) Specifying rules for modifying or interpreting address field of the instruction

   (D) All the above

5. _____ Register keeps track of the instructions stored in program stored in memory.
   (A) AR (Address Register) **(B)** XR (Index Register)

   (C) PC (Program Counter) **(D)** AC (Accumulator)

6. A Stack-organised Computer uses instruction of
   (A) Indirect addressing **(B)** Two-addressing

   (C) Zero addressing **(D)** Index addressing

7. The minimum number of bits in operation code (opcode) required for implementing **N** different operations is:
   (A) 2^N (B) 2N
   (C) log2(N) (D) log10(N)

8. The operation executed on data stored in registers is called
   (A) Macro-operation **(B)** Micro-operation

   (C) Bit-operation **(D)** Byte-operation

9. The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called
   (A) Data transfer instructions. **(B)** Program control instructions.

   (C) Input-output instructions. **(D)** Logical instructions.

10. A computer's memory is composed of 8K words of 32 bits each. How many bits are required for memory address if smallest addressable unit is one word?
    (A) 13 (B) 8
    (C) 10 (D) 5

11. A computer's memory is composed of 4K words of 32 bits each. How many total bits in memory?
    (A) 12800 (B) 1280000
    (C) 1310720 (D) 131072

12. A "word" is the natural unit of organization of memory. Different computer types may have different word length (in bits).
    (A) True (B) False

13. Register contains data and instructions needed by the CPU.
    (A) True (B) False

14. In computers, subtraction is generally carried out by
    (A) 9's complement (B) 10's complement
    (C) 1's complement (D) 2's complement

15. A computer system has seven 8-bit registers. We need to implement a shared 8-bit data bus. We need:
    A) Eight 8x1 multiplexers B) Eight 4x1 multiplexers
    C) Seven 8x1 multiplexers D) Eight 2x4 decoders
    E) Seven 2x4 decoders

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Question 2 (10 points)

What is the 8-bit results after performing each of the following shift operations?

Arithmetic Shift Left of (11110010)	
Circular shift left of (11110010)	
Logical shift left of (11110010)	
Arithmetic shift right of (11110010)	
Logical shift right of (11110010)	

Question 3 (10 points)

A computer uses a memory unit with 2M words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 18 registers, and an address part by which the memory unit can be accessed directly.

How many bits are there in the register code part	
How many bits are there in the address part	
How many bits are there in the data inputs of the memory	
What is the maximum number of different operations that can be implemented by this machine	
What is the maximum size of memory that can be accessed indirectly	

Question 4 (10 points)

Draw a digital circuit of computer which has a common bus system for 4 registers of 4 bits each. Your draw should show clearly data transfer from and to the registers.

Question 5 (10 points)

Consider a computer that has a number of registers such that the three registers R0 = 1000, R1 = 1008, and R2 = 1002. Part of the memory is shown in the diagram below. Identify the addressing mode and show the effective address of memory and the registers' contents in each of the following instructions (assume that all numbers are decimal).

(1) **ADD R0, (1010)**

(2) **SUB R1, ((R2))**

(3) **MOV R2, (4+((R1-2)))**

Address	Memory
1000	1003
1001	1004
1002	1005
1003	1006
1004	1007
1005	2
1006	1000
1007	1002
1008	1001
1009	1002
1010	3
1011	4

Question 6 (10 points):

Write the Register Transfer Language (RTL) of the following pseudo code, then **Draw** the circuit that represents it using minimum logic gates.

If ((P = 1 AND Q = 1) OR (P=0 AND Q=0)) Then

R1 gets (R2)

Else

R1 gets (R3)

Where P, Q are the input signals to the control unit, and R1, R2 and R3 are general 4-bit registers.

Question 7 (10 points):

a) Draw a state machine for the instruction cycle.[4pts]

b) (i) Describe benefit of 1's complement number compared to signed magnitude representation. [6pts]

(ii) Describe benefit of 2's complement number compared to 1's complement representation.

(iii) Use the minimum number of bits to represent (-24) using the following signed number representations:

(1) Sign magnitude:

(2) Bias representation:

(3) 1's complement:

(4) 2's complement: