



Computer Organization and Assembly Language – ENCS336

Midterm – Summer 2022

Name (Arabic):

Solution

ID:

| Question | Maximum | Mark |
|--------------|-----------|------|
| 1 | 15 | |
| 2 | 10 | |
| 3 | 15 | |
| Total | 40 | |

Question 1:[15 marks]_Multiple choice

- Which of the following is the correct definition of Computer?
(A) Computer is a machine or device that can be programmed to perform arithmetical or logic operation sequences automatically
(B) Computer understands only binary language, which is written in the form of 0s & 1s
(C) Computer is a programmable electronic device that stores, retrieves, and processes the data
(D) All of the mentioned
- Which of the following programming languages has an instruction set closest to the machine language of a computer?
A) BASIC B) Java (C) Assembly Language D) C/C++
- Which of the following unit is responsible for converting the data received from the user into a computer understandable format?
a) Output Unit (b) Input Unit
c) Memory Unit d) Arithmetic & Logic Unit
- Which of the following is the brain of the computer?
(A) CPU (B) Memory (C) Logical gates (D) Transistor
- The Stack machine uses instruction of
(A) Two-addressing (B) One-addressing (C) Zero addressing (D) Index addressing

6. The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called

- (A) Data transfer instructions. (B) Program control instructions.
(C) Input-output instructions. (D) Logical instructions

7. A computer's memory is composed of 8K cells of 32 bits each. How many bits are required for memory address if the smallest addressable memory unit is one cell?

- (A) 13 B) 8 C) 10 D) 6

8. If a register containing data $(11001100)_2$ is subjected to arithmetic shift right operation, then the content of the register after shift shall be

- (A) 01100110 (B) 11100110
(C) 10011001 (D) 10011000

9. If an 8-bit register contains a value of -12 (using 2's complement), the register value after applying rotate right 2 bits becomes:

- (A) -61 (B) +61 (C) -4 (D) +4

10. The addressing mode in which the address of an instruction's operand is stored into a register

- A. Register direct B. Register indirect C. Direct D. Indirect

11. There can be multiple computer organizations for the same computer architecture

- A. True B. False

12. Which of the following computer memory is fastest?

- (A) Register B) Hard disk C) RAM D) None of the above

13. Computer address bus is

- A) Multidirectional B) Bidirectional (C) Unidirectional D) None of the above

14. Where is the decoded instruction stored?

- A) MAR B) MDR C) PC (D) IR

15. In order to reset (make zero) the least significant bit of a 8-bit register R without changing the other bits, we use:

- A) XOR R, R, 0x1 B) AND R, R, 0x1 C) OR R, R, 0x1 (D) AND R, R, 0xFE

Question 1 answers:

| | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| D | C | B | A | C | A | A | B | B | B | A | A | C | D | D |

Question 2: [15 marks]

A computer has the following instruction and integer format. The instruction consists of 3 bits opcode, 1 bit (M) that indicate the addressing mode, and the remaining bits are used either for immediate or address. When M=0 => immediate, when M=1 => memory direct. The memory is 2-bytes addressable, i.e., each memory location is 16 bits. Assume that the programs (instructions) should be stored in the memory starting from address 0, while data should be stored starting from address 80H. Unless otherwise stated, assume that the initial content of all registers and memory is 0. All numbers are in hexadecimal.

| | | | | | | |
|--------------------|--|---------------------|----------------------------|--|--------------------|---------|
| Opcode (3bits) | | M (1bit) | Immediate/Address (12bits) | | Main Memory | |
| Instruction format | | | | | Address | Content |
| Sign 1 bit | | Magnitude (15 bits) | | | 0 | 0x8064 |
| Integer | | | | | 1 | 0x7080 |
| | | | | | 2 | 0x5082 |
| | | | | | 3 | 0xA000 |
| | | | | | ... | ... |
| | | | | | 0x80 | 0x0046 |
| | | | | | 0x81 | 0x0064 |
| | | | | | 0x82 | 0x0000 |
| | | | | | | |

The computer supports the following operations:

- 011: Add immediate /from memory to AC
- 100: Load immediate/from memory to AC
- 001: Subtract immediate /from memory from AC
- 010: Store AC to Memory
- 101: Jump to Memory address

1. Starting with zero's initial values in all registers, fill in the following table by executing four instructions. [5pts]

| Instruction | PC | AC | IR | MAR | MBR |
|------------------------------------|----|-----|------|-----|------|
| Initial values | 0 | 0 | 0 | 0 | 0 |
| After executing first instruction | 1 | 064 | 8064 | 0 | 8064 |
| After executing second instruction | 2 | 0AA | 7080 | 80 | 0046 |
| After executing third instruction | 3 | 0AA | 5082 | 82 | 00AA |
| After executing fourth instruction | 0 | 0AA | A000 | 3 | A000 |

(Hex)

Write assembly code to add memory location 0x80 to memory location 0x81 and store the result in memory location 0x82. [3pts]

Load [80]
ADD [81]
Store [82]

3. Write the machine code for the instruction that jumps to the instruction at address 8. [4pts]

101 0 0000 0000 1000 => 0xA008

4. What is the range of the signed integer values that can be stored in one memory cell? [3pts]

$-2^{15}-1 \rightarrow +2^{15}-1$

Question 2: [20 marks]

A) What is interrupt? Mention three sources that make interrupt? [4pts]

A mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing to improve processor efficiency.

Source & int.

- ① SW program e.g. divide by zero.*
- ② Timer.*
- ③ HW I/O*
- ④ HW Failure.*

B) Assume we have four devices D1, D2, D3 and D4. Device D4 has the highest priority, then device D2 followed by device D1 and then D3 has the lowest priority. A user program begins at time $t = 0$ sec.

- at $t = 10$ sec D2 interrupt occurs and it needs 20 sec to be handled
- at $t = 15$ sec D4 interrupt occurs and it needs 15 sec to be handled
- at $t = 20$ sec D1 interrupt occurs and it needs 10 sec to be handled
- at $t = 25$ sec D3 interrupt occurs and it needs 25 sec to be handled

1. Assume using sequential multiple interrupts, complete the table below: (8 pts)

| Device | Interrupt handling start time | Interrupt handling end time |
|--------|-------------------------------|-----------------------------|
| D1 | 45 | 55 |
| D2 | 10 | 30 |
| D3 | 55 | 80 |
| D4 | 30 | 45 |

2. Now Assume using nested multiple interrupts, complete the table below: (8 pts)

| Device | Interrupt handling start time | Interrupt handling end time |
|--------|-------------------------------|-----------------------------|
| D1 | 45 | 55 |
| D2 | 10 | 45 |
| D3 | 55 | 80 |
| D4 | 15 | 30 |