BIRZEIT UNIVERSITY

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ENEE2103

Report For Exp#8

“The Field-Effect Transistor”

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Abstract:

This experiment leads to identify new electronic devices which are FET transistor and how to use them in the circuit, it has three heads gate, source, and drain. There is a lot of application that FET transistor enters in it and one of this application was shown in this experiment which is an amplifier. Many devices used in this part to study the characteristic of it like DMM to use the RMS voltage and current, an oscilloscope to measure peak to peak voltage.

The method used

- ✓ Digital Multimeter to measure DC values and rms values of voltages and currents.
- ✓ Resistors, capacitorsand FETs.
- ✓ DC power supply ,and an AC power generator
- ✓ board to place elements and wires to connect them.
- ✓ Oscillators to see the phase shifts.

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Theory

The **field-effect transistor (FET)** is a type of transistor that uses an electric field to control the flow of current. FETs are devices with three terminals: *source*, *gate*, and *drain*. FETs control the flow of current by the application of a voltage to the gate, which in turn alters the conductivity between the drain and source.

FETs are also known as unipolar transistors since they involve single-carrier-type operation. That is, FETs use either electrons or holes as charge carriers in their operation, but not both. Many different types of field effect transistors exist. Field effect transistors generally display very high input impedance at low frequencies. The most widely used field-effect transistor is the MOSFET (metal-oxide-semiconductor field-effect transistor).

❖ CHARACTERESTICS OF AN N-CHANNEL JFET

A JFET is a three terminal semiconductor device in which current conduction is by one type of carrier i.e. electrons or holes. The current conduction is controlled by means of an electric field between the gate and the conducting channel of the device. The JFET has high input impedance and low noise level.

The big point is that, an N-Channel JFET turns on by having a positive voltage applied to the drain terminal of the transistor and ideally no voltage applied to the gate terminal.
The transistor is in its fully conductive state and is in maximum operation when the voltage at the gate terminal is 0 V . [1]

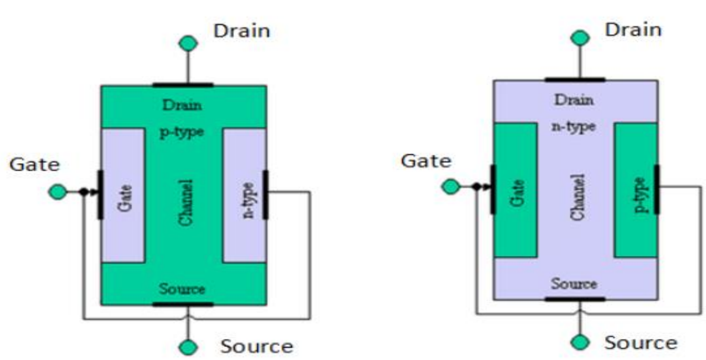


Figure 1:A JFET consists of a p-type or n-type

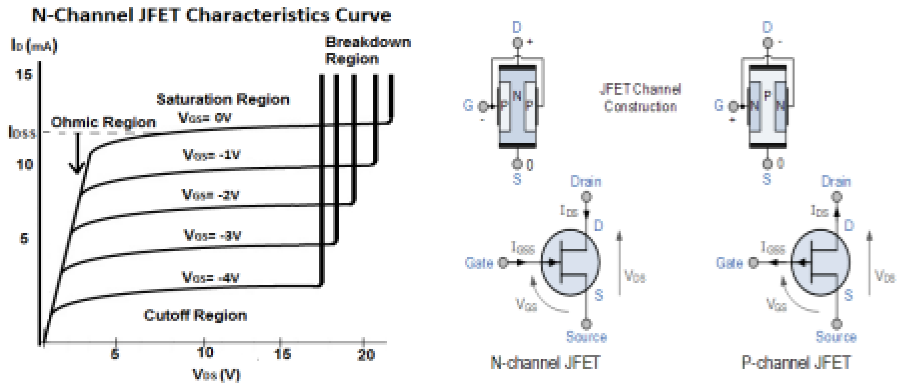


Figure 2:N-channel JEFT characteristics curve

$IDS = IDSS(1 - \left(\frac{VGS}{VP}\right))$……….(1) This equation used to measure the current between drain and source.

$AV = \frac{VOUT}{VIN}$ ……………………………(2) This equation to compute the voltage gain

❖ A JFET AMPLIFIER.

Common Source JFET Amplifier uses junction field effect transistors as its main active device offering high input impedance characteristics. Transistor amplifier circuits such as the common emitter amplifier are made using Bipolar Transistors, but small signal amplifiers can also be made using Field Effect Transistors.[2]

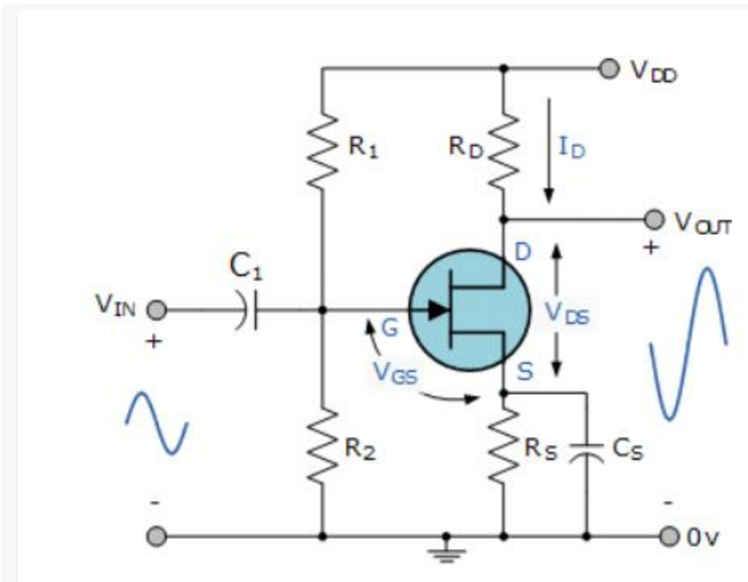


Figure 3:JFET amplifier

❖ COMMON DRAIN AMPLIFIER.

In electronics, a common-drain amplifier, also known as a source follower, is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit (NMOS) the gate terminal of the transistor serves as the input, the source is the output, and the drain is *common* to both (input and output), hence its name. The analogous bipolar junction transistor circuit is the common-collector amplifier. This circuit is also commonly called a "stabilizer."

In addition, this circuit is used to transform impedances. For example, the Thévenin resistance of a combination of a voltage follower driven by a voltage source with high Thévenin resistance is reduced to only the output resistance of the voltage follower (a small resistance). That resistance reduction makes the combination a more ideal voltage source. Conversely, a voltage follower inserted between a driving stage and a high load (i.e. a low resistance) presents an infinite resistance (low load) to the driving stage—an advantage in coupling a voltage signal to a large load.[3]

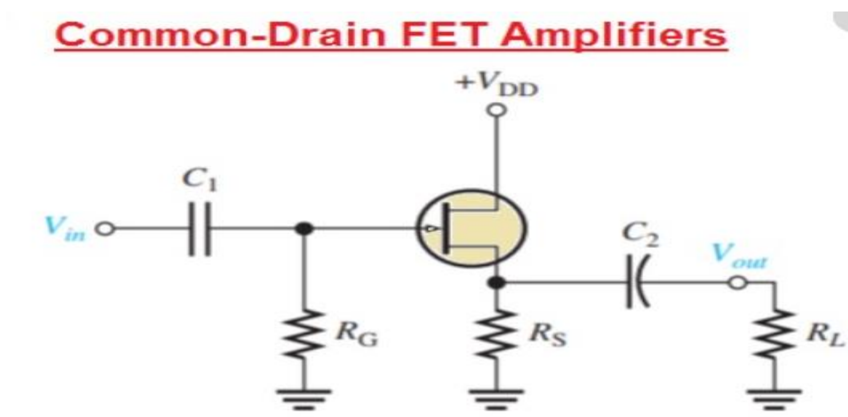


Figure 4:example of drain amplifiers

❖ CONSTANT CURRENT SOURCE.

A constant current source is a power source which provides a constant current to a load, even despite changes and variance in load resistance.

In other words, the current which a constant current source provides is steady, even if the resistance of the load varies.

A constant current source is, thus, a very valuable component because it can supply steady current even if there are changes in resistance, even a wide variance in the resistance. This comes in use when a circuit needs a steady current supply, without fluctuations.

Procedure:

I. CHARACTERESTICS OF AN N-CHANNEL JFET.

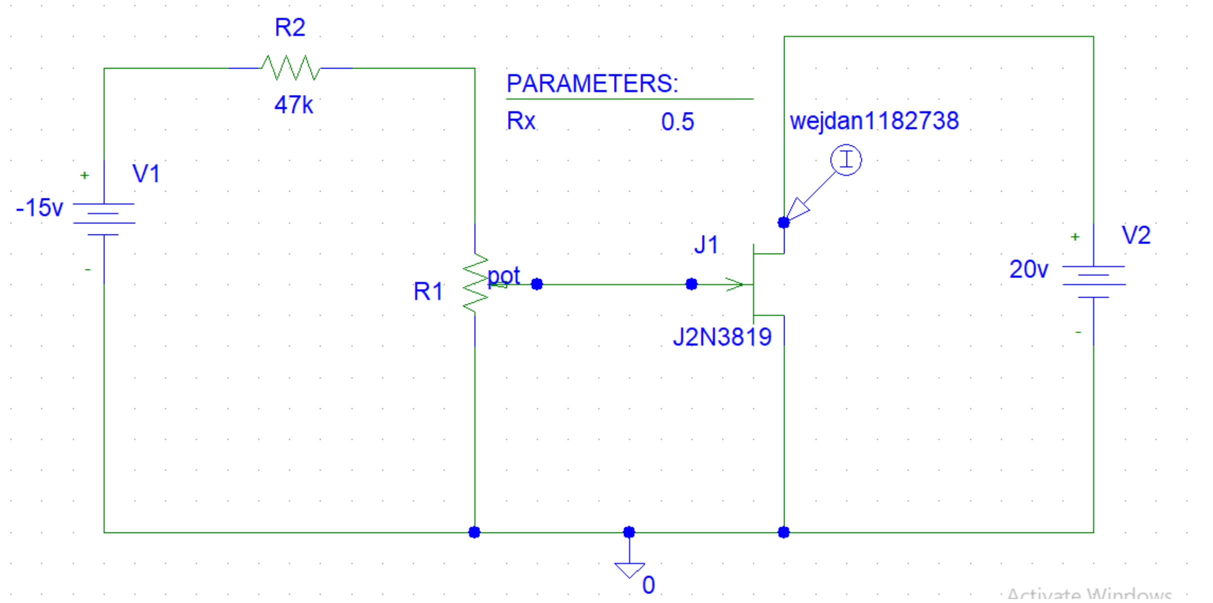


Figure 5: CHARACTERESTICS OF AN N-CHANNEL JFET

The circuit in figure 5 was connected. The values of potentiometer and variable DC source were changed repeatedly to get different values of VDS and VGS and ID was measured each time. The values are shown table1.

Table 1:

Vgs(V)	ID(mA) fpr Vds=(V)						
	0	0.5	1	2	5	10	15
0	0.142	3.267	6.16	9.33	11.5	12	12.8
-0.5	57.4M	1.96	5.16	7.4	8.8	10.5	14.7
-1.0	0.134	2.38	3.64	5.12	5.9	8.72	15.8
-1.5	0.12	1.76	3	3.9	4.46	7.9	16.2
-2.0	0.1	1.17	1.85	2.24	5.56	6.51	16.4
-2.5	0.09	0.69	0.93	1.104	1.34	5.45	16.4

By analyzing the figure “ID vs. VD” that produced from these values we got that Vgs work as control voltage as shown in figure 6.

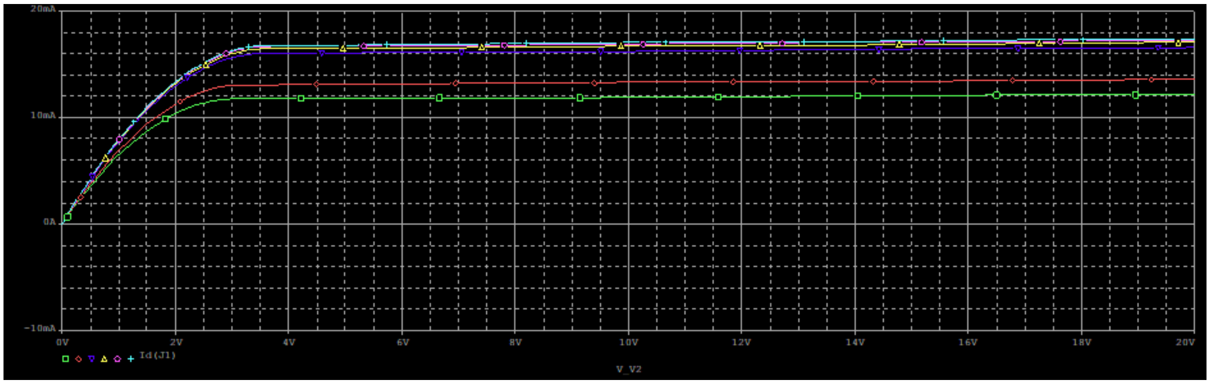


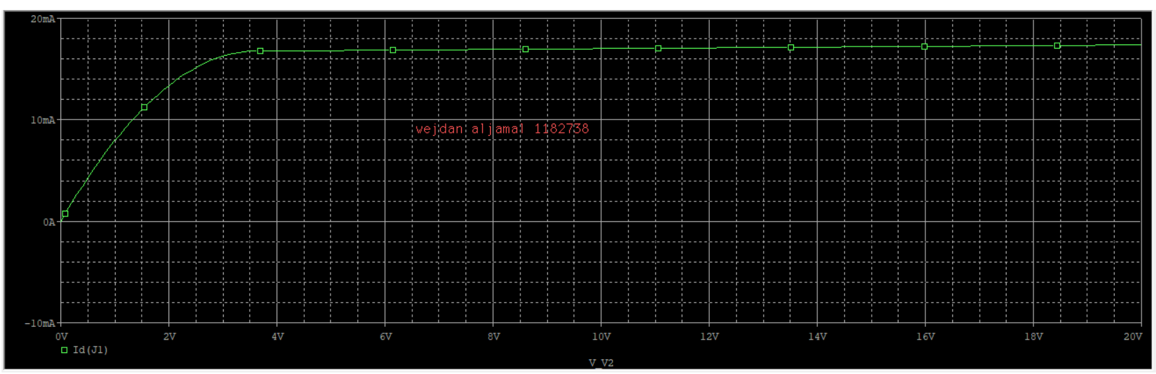
Figure 6:Id vs Vd simulation

When VDS is set to 10 V and VGS is set to-1.0 V, then IG = 0

- **Questions**

  1- From your graph, above which values of VDS is ID almost unaffected by VDS when VGS=0?

  (Vds,Ids)= (4.5691,16.811m) in Prelab



and when VGS= 0, ID is almost unaffected byVDS when VDS ≥ 5 volts.

2- For a given value of VDS changing VGS does not result in equal changes

3- Can you measure IG or is it too small?
It's too small, so it's very hard to measure it

4- Estimate the change in id for 0.5 change in vgs (vds=10v,vgs=-1v) ,then find gm

VDS=10V, at VGS=-1V -> IDS=8.73 and at VGS=-1.5V -> IDS=7.9V

gm = $change\ in\ ID\ /change\ in\ VGS$ =8.73-7.9/0.5 =1.6

II. A JFET AMPLIFIER.

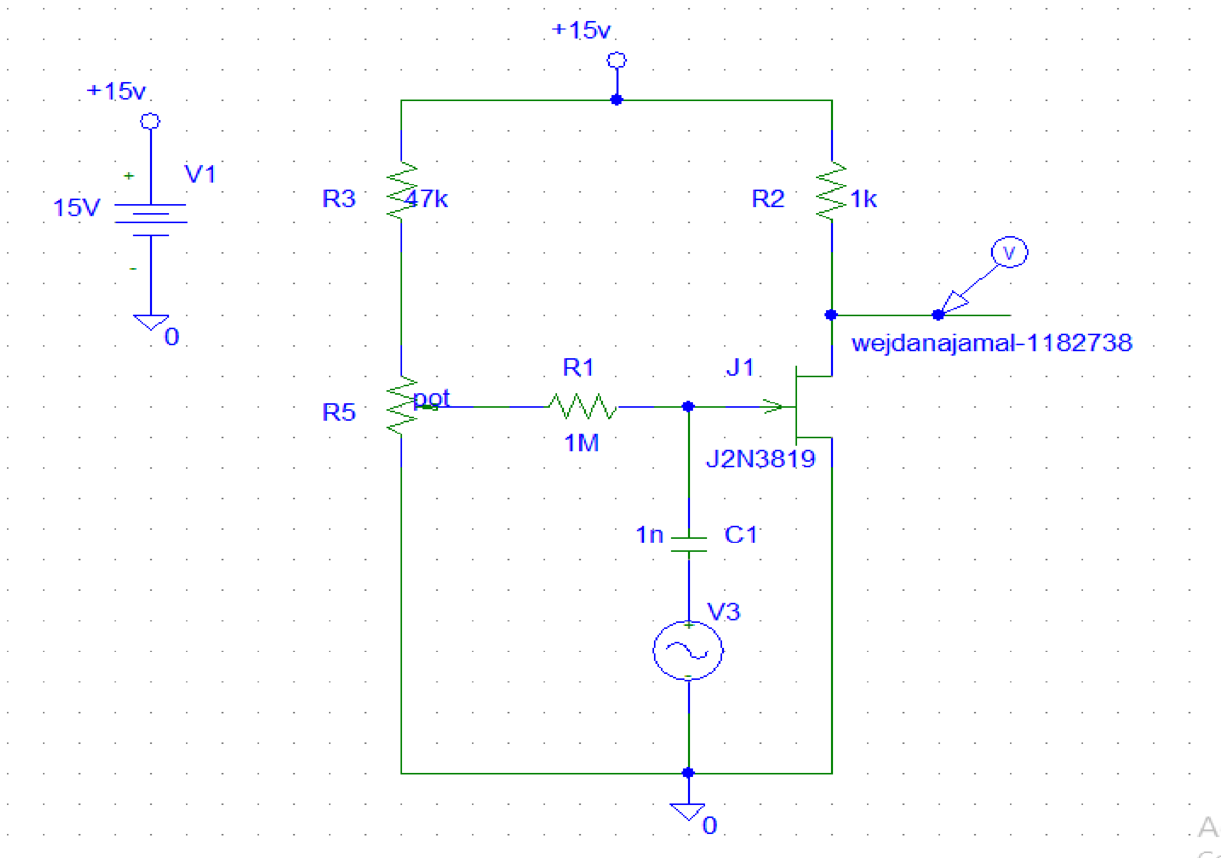


Figure 7:a jfet amplifier

First, the resistances were checked using a Multi-meter Then, the circuit was connected as in fig(7) with a generator which is an Ac source with 1khz and zero amplitude at the first. Then, Vds was set to equal 10 v by controlling the potentiometer value. After that, the Oscilloscope was linked to the circuit via connecting channel one to the input source and the other channel to the output so the below fig(8) was produced, this figure is shown peak to peak values of input and output. After that, the amplitude of the generator was changed until got peak to peak in channel 2 equals two volts and by getting the output voltage so the voltage gain can be measured according to this equation $av = vout/vin$, For measuring the input impedance "Zin" , current and voltage values were measured by DMM and apply the following equation $zin = vin/ii$

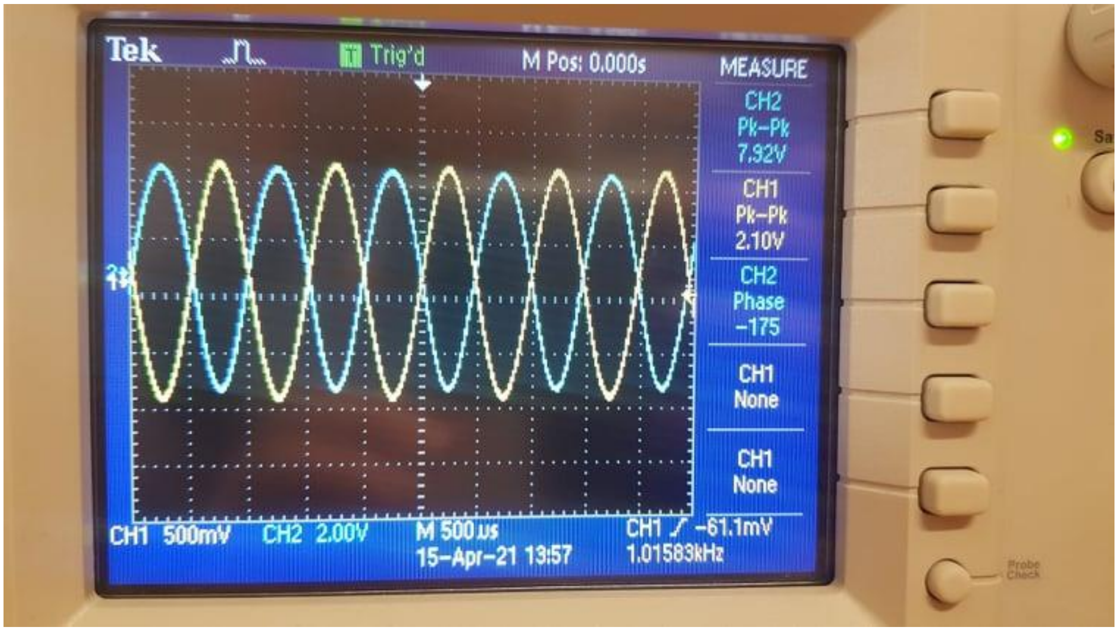


Figure 8: AC sweep of input and output

- The peak to peak output was measured and the value :

$$vp - p = 7.92v$$

- and the voltage gain :

$$vgain = \frac{vo}{vi} = \frac{7.92}{2} = 3.96v$$

- input current using DMM :

$$Ii = 5.22ma$$

- $Zin = \frac{Vin}{Iin} = \frac{1.414}{5.22} = 0.271$

III. COMMON DRAIN AMPLIFIER.

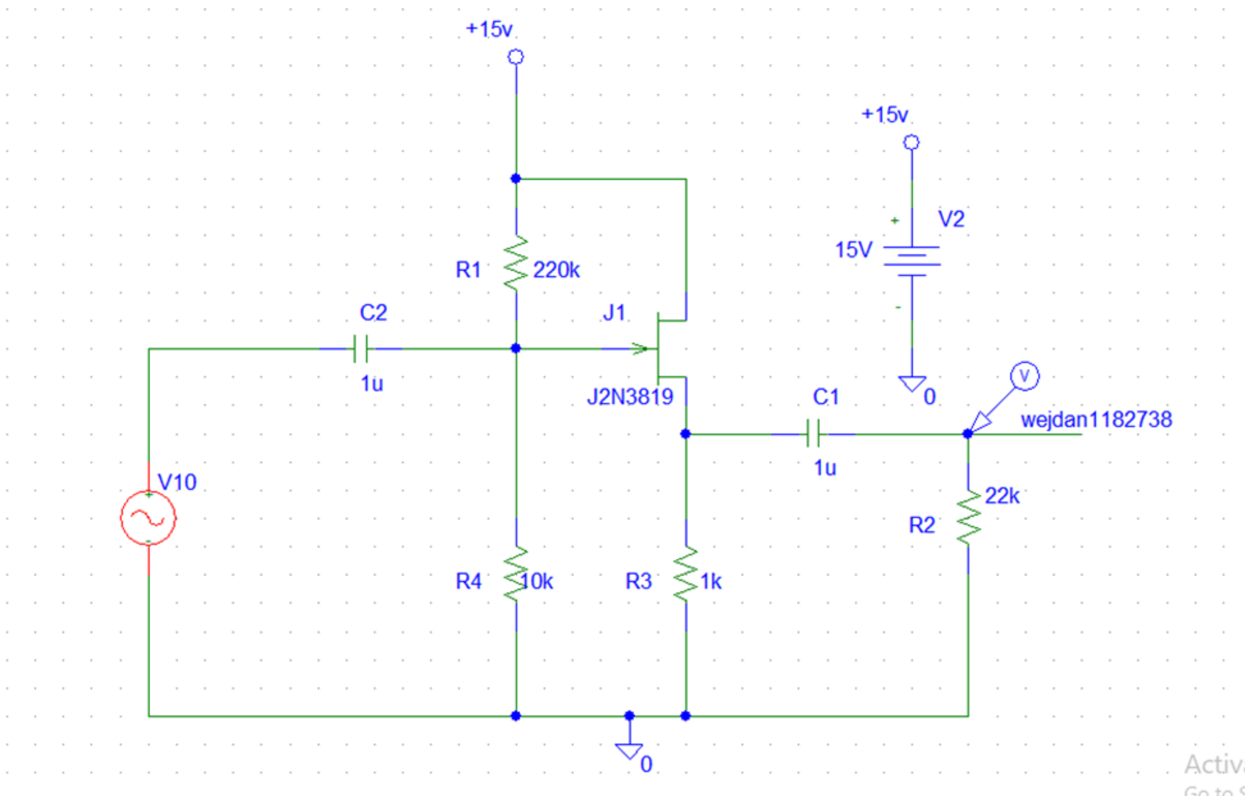


Figure 9:common drain amplifier

First, the resistances were checked using a Multi-meter Then, the circuit was connected as in fig(9) with a generator which is an Ac source with 1khz and zero amplitude at the first to measure Vg and Vs. Then, changing the amplitude of generator to get 0.4 peak to peak input voltage in Oscilloscope as appeared in fig(10) then the voltage gain can be measured by the following equation $av = vout/vin$, also phase difference between two waves equals zero which means that waves are in phase. After that, to compute the input and output impedances DMM was used by getting the current and voltage and using the following equations $zin = vin/ii$ To measure the output impedance, the location of the input source was transferred to the output part and repeat measuring current and voltage $zout = vout/iout$

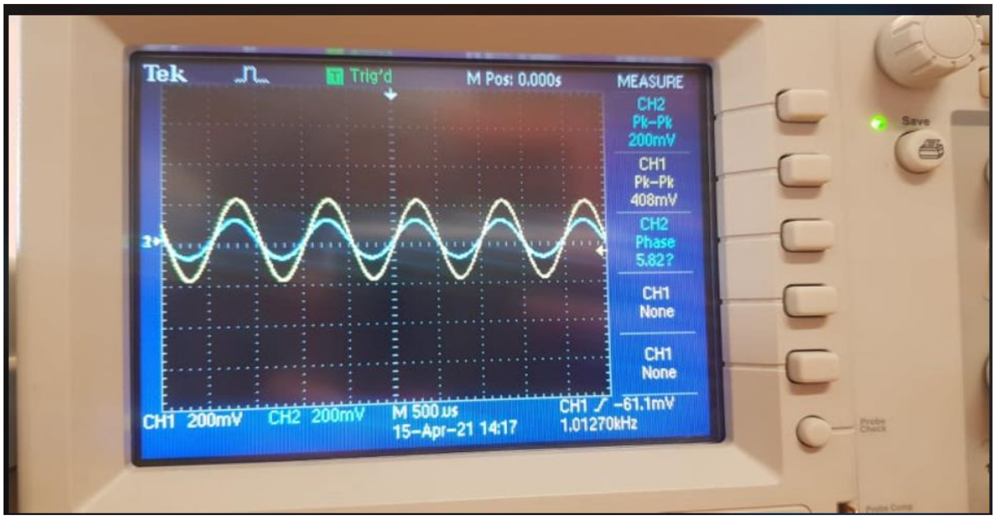


Figure 10: AC sweep of input and output

By analyzing the above figure the phase difference equals zero because two waves are in phase together and voltage gain by dividing Vout(channel1) over Vin(channel2)

- Vo and Vin was calculated and the result is :

$$vo = 200mv \;\; \& \; vin = 408mv$$

- Voltage gain :

$$v\ gain = \frac{vo}{vin} = \frac{200}{408} = 0.49mv$$

- The phase shift equal zero

- To calculate Zin and Z out , need the input and output current, in addition to input and output voltage

$$Ii = 13.32ma \;\; , Io = 8.6\ ma$$

$$Zin = \frac{Vi}{Ii} = \frac{408}{13.32} = 30.63\ \Omega$$

$$Zout = \frac{Vo}{Io} = \frac{200}{8.6} = 23.255\ \Omega$$

- By using DMM some values were measured as Vg=0.656 v, Vs=2.979 v which are very near to the theoretical values so they acceptable.

- **Question:**

Compare the voltage gain of step 5 with the theoretical gain value

$$Av\ theory = \frac{gm * regu}{1 + gm * regu}$$

$$gm = \frac{\Delta Id}{\Delta Vgs}$$

IV. CONSTANT CURRENT SOURCE

The circuit was connected as figure 11 with variable resistors, JFET transistor and power supply. VRL and ID was measured by change the resister between 0.1-3kΩ as shown in table2.

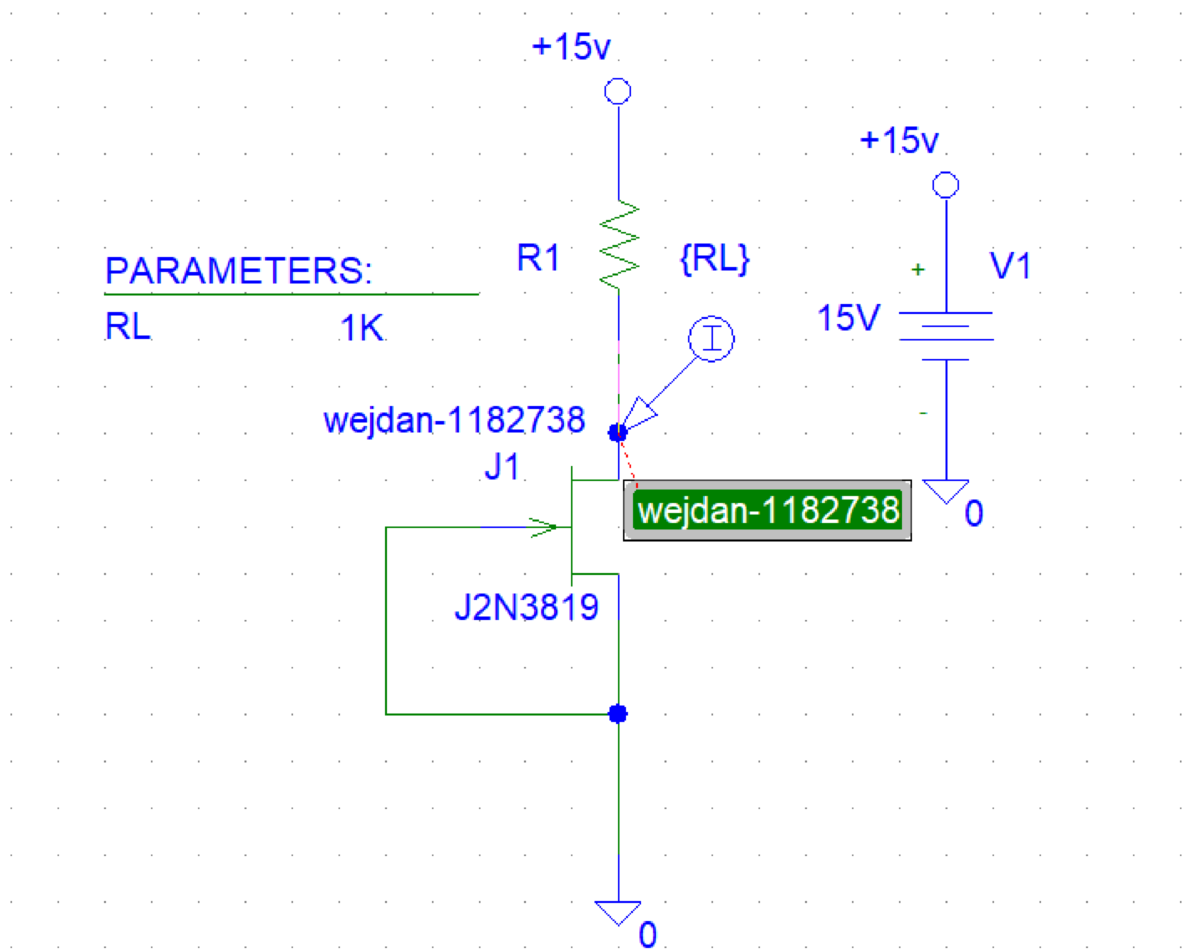


Figure 11: constant current source circuit

Table 2:

RL(KΩ**)**	**Vl(V)**	**ID(mA)**
0.1	1.13	11.3
0.22	2.46	11.18
0.33	3.67	11.12
0.47	5.21	11.08
0.56	6.2	11.07
1	10.67	10.67
1.5	13.04	8.69
2	13.72	6.56
3	14.23	4.74

After analyzing the above table constant value around 11.07 v was fixed until the value of R=1kΩ " in pinch off region" but after that when the resistor was increased the drain current decreased.

- To measure the maximum theatrical value of resistance provides a constant current , the below equation will apply, $Vds = Vdd - Id * Rl$ .From this equation

$RL = \frac{Vds-vdd}{id} = 10/11.07 \approx 903\Omega$ which is near to 1kΩ.

Conclusion

In this experiment, the JFET transistor was displayed, and how to connect it in the circuit some measurements were taken to understand the characteristic of the transistor more by using many devices like DMM, multi-meter, and oscilloscope. Talk one of the most important used applications of JFET which is an amplifier, there are many causes of errors like fault in elements themselves, wire and devices.

References

1. http://www.learningaboutelectronics.com/Articles/N-channel-JFET#:~:text=The%20big%20point%20is%20that,applied%20to%20the%20gate%20terminal.&text=The%20transistor%20is%20in%20its,the%20gate%20terminal%20is%200V.

2. https://www.electronics-tutorials.ws/amplifier/amp_3.html

3. https://en.wikipedia.org/wiki/Common_drain