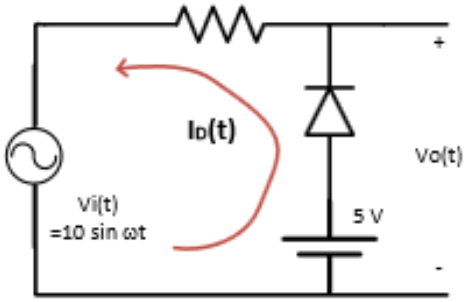
# ENEE2103- Circuits and Electronics lab

# Electronics Theoretical Background Summary

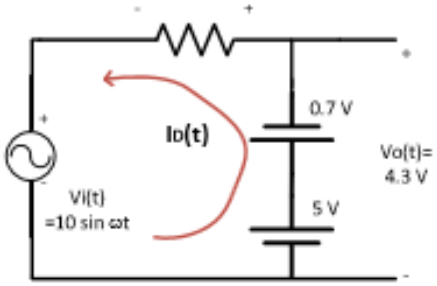
## 1. Diode Applications

### ⇨ Clipper-Limiter

Example: Calculate and sketch Vo(t) using simplified diode model

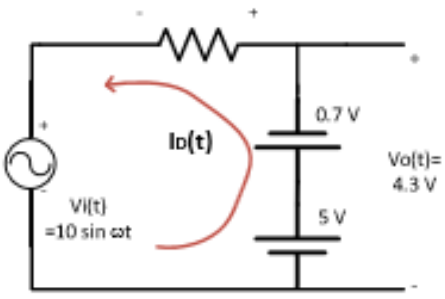



1) Assume diode is ON, so we replace it by 0.7 V and $i_D(t)$ must be > 0




$$5V - 0.7V - i_D(t).R - Vi(t) = 0$$
$$i_D(t).R = 4.3V - Vi(t)$$

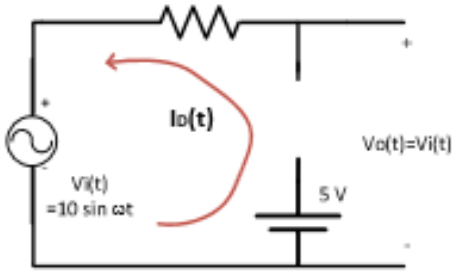
$$i_D(t) = \frac{4.3V - Vi(t)}{R} > 0$$




$$\therefore \quad 4.3V - Vi(t) > 0$$
$$\Rightarrow Vi(t) < 4.3V$$

when $Vi(t) < 4.3$ V diode is ON ar
$Vo(t) = 4.3V$

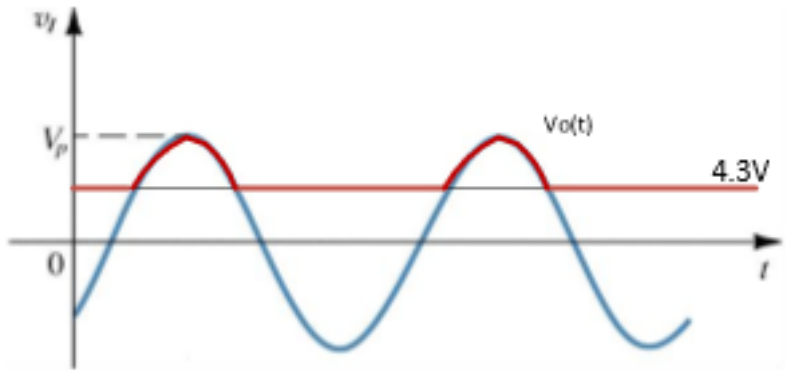
2) Otherwise, When Vi(t) is > 4.3 V, Diode will be off and it is replaced by open circuit




$$\Rightarrow Vi(t) > 4.3V$$
$$Vo(t) = Vi(t)$$

when $Vi(t) < 4.3V$ , diode is ON & $Vo(t) = 4.3V$

when $Vi(t) > 4.3V$ , diode is off & $Vo(t) = Vi(t)$

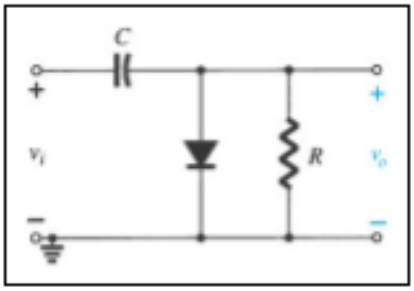


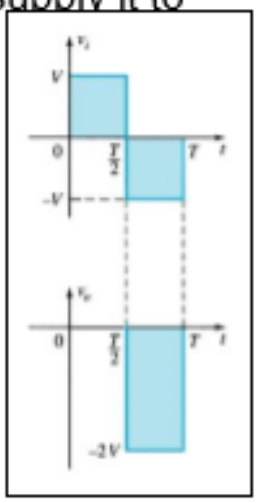

⇨ **Diode Clamper**

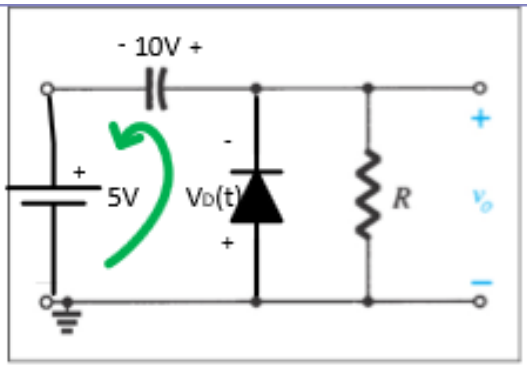
# Clampers

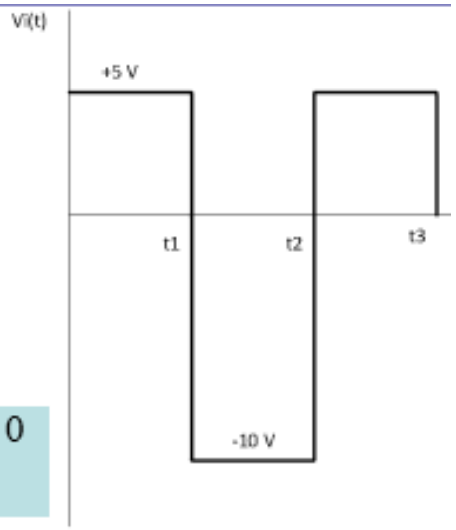
**Function:** A Clamper shifts the input waveform up or down (adds a dc offset) while keeping its shape and peak to peak value unchanged.

It consists of a diode and capacitor (and maybe a series dc source ) that can be combined to "clamp" an AC signal to a specific DC level and supply it to the load R



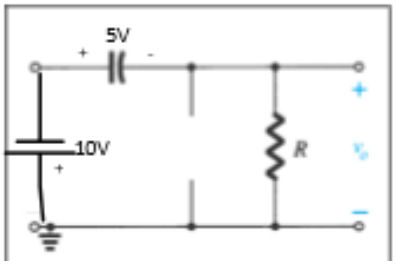





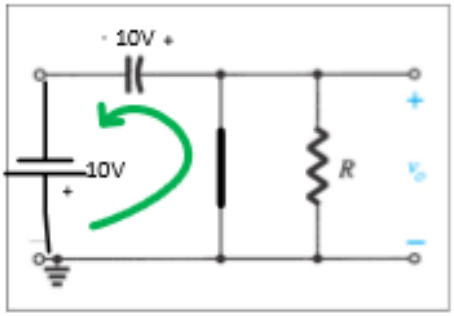

KVL around the loop : $10 + 5 + V_D(t) = 0$

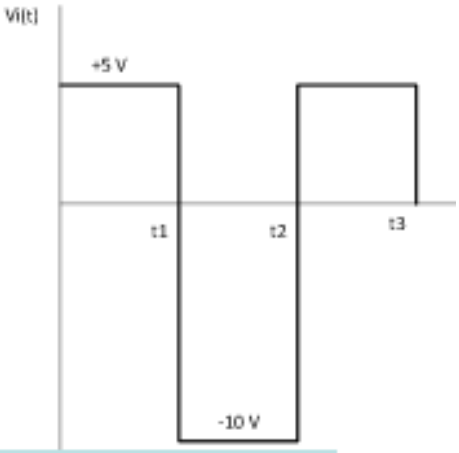
$\Rightarrow V_D(t) = -15\ V < 0$ ,∴ diode is OFF




$Vo(t) = -V_D(t) = 15\ V$

Cap is charged to 10V with shown polarity due to diode forward current $Vo(t) = 0\ V$

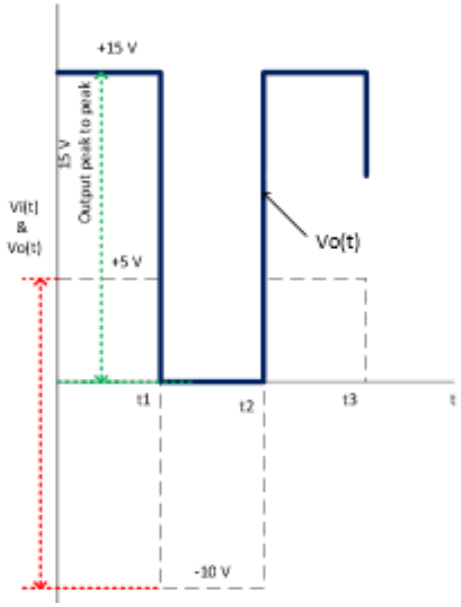



2) for $t_2 < t < t_3$ voltage source reverses polarity, $Vi(t) = +5V$ while Cap keeps its charge $Vc = 10V$

Afterwords for any value of the given Vi(t) diode remains OFF and $Vo(t) = Vi(t) + 10$

∴ the clamper charges a cap and uses this charge to add up to the input to shift it up or down (i.e. add dc offset)




Important Note

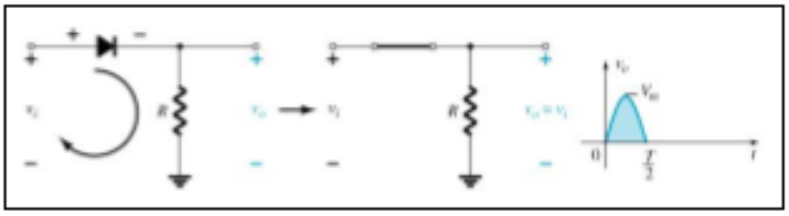
For Proper Clamping action , $\tau_{discharge}$ must be large enough ( at least 10 times the period of the input waveform)

$$\tau_{discharge} = R.C > 10\,(t_1 + t_2)$$

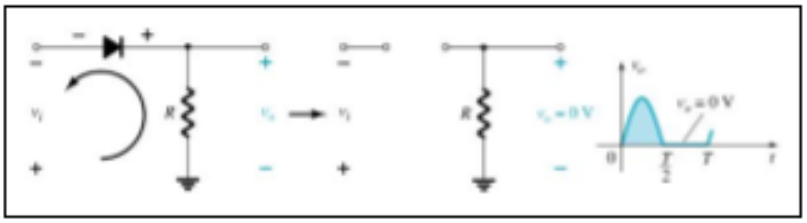
⇨ **Diode Rectifier**

## Half Wave Rectifier

1)When $Vi(t) > 0$, Diode is ON
$Vo = Vi$



2)When $Vi(t) < 0$, Diode is OFF
$Vo = 0$



The diode conducts only when it is forward biased, therefore only half of the AC cycle passes through the diode to the output.

$$V_{AVG} = \frac{1}{T}\int_0^T V_m Sin(\omega t)dt$$

# Half Wave Rectifier

$$V_{AVG} = \frac{1}{T}\int_0^T V_m Sin(\omega t)dt$$

$$= \frac{1}{2\pi}\int_0^{\pi} V_m Sin(\theta)d\theta$$

$$= \frac{1}{2\pi}\left[-V_m Cos(\theta)\right]_0^{\pi} = \frac{V_m}{2\pi}\left[-Cos(\pi) - (-Cos(0))\right]$$

$$V_{AVG} = \frac{V_m}{2\pi}\left[-(-1) - (-1)\right]$$

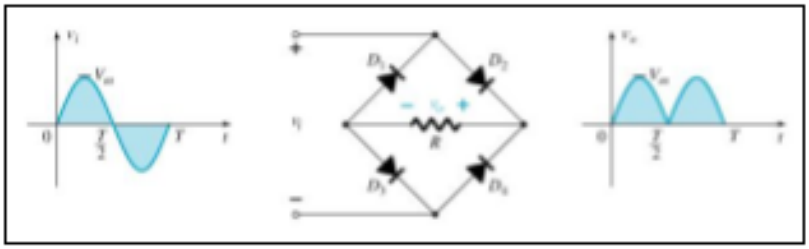
$$= \frac{2V_m}{2\pi} = \frac{V_m}{\pi} \cong 0.318V_m$$

$T = T_o$ and $f = f_o$

(period and frequency of the rectified waveform is the same as ac input)

# Bridge Full-Wave Rectifier

A full-wave rectifier with four diodes that are connected in a bridge configuration

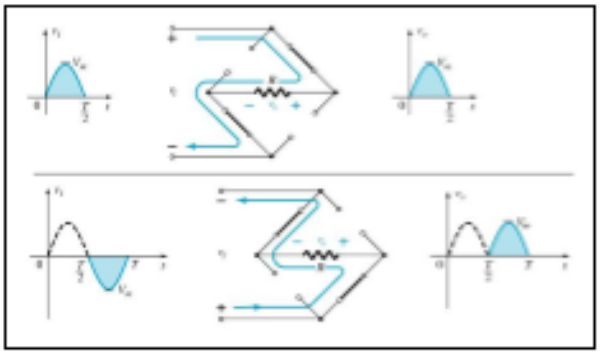


1)When Vi(t) > 0,
D2, D3 are ON
D1, D4 are OFF

$\Rightarrow Vo(t) = Vi(t)$

2)When Vi(t) < 0,
D2, D3 are OFF
D1, D4 are ON

$\Rightarrow Vo(t) = -Vi(t)$



$$V_{AVG} = \frac{2V_m}{\pi} \cong 0.636V_m$$

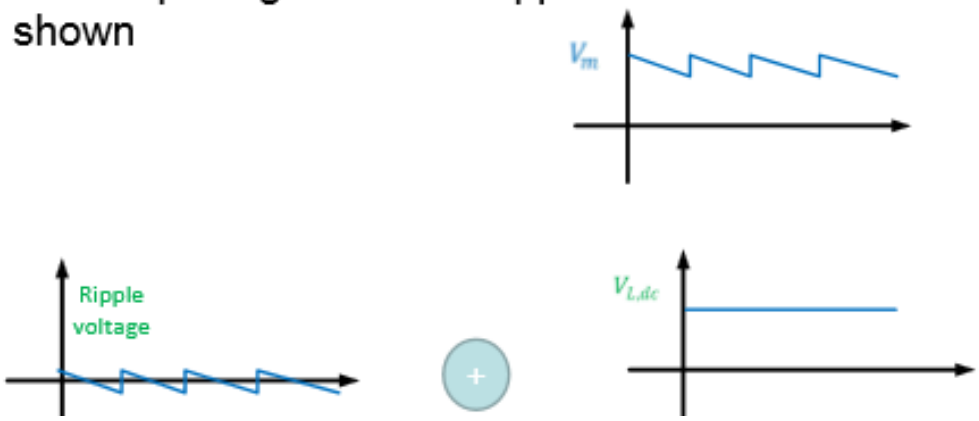
$$T = \frac{T_o}{2} \text{ and } f = 2f_o$$

(period and frequency of the rectified waveform is not the same as ac input)

- Ripple factor is an indicator for the effectiveness of the filter

$$r = \frac{RMS(ripple\ voltage)}{Average\ value\ of\ the\ output\ signal} \times 100\%$$

- The output signal can be approximated as shown




- Also for a triangular signal,

$$\text{RMS Value} = \frac{\text{Peak Value}}{\sqrt{3}}$$

OR

$$\text{RMS Value} = \frac{\text{Peak to peak Value}}{2\sqrt{3}} = \frac{V_{Lr,p-p}}{2\sqrt{3}}$$

$$V_{L,dc} = V_m - \frac{1}{2}V_{Lr,p-p}$$

a) For Half Wave Rectifier

$$t_2 - t_1 \cong T_o = \frac{1}{f_o}$$

$$V_{Lr,p\text{-}p} = V_m\left(\frac{T_o}{RC}\right) = V_m\left(\frac{1}{f_o RC}\right)$$

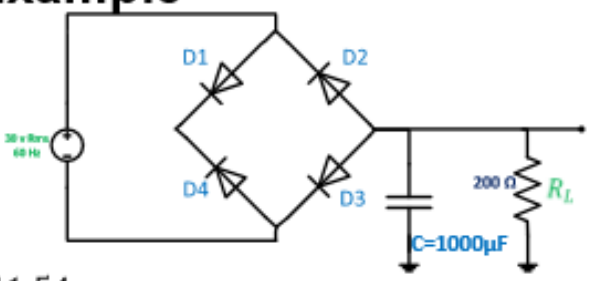
b) For Full Wave Rectifier

$$t_2 - t_1 \cong \frac{1}{2}T_o = \frac{1}{2f_o}$$

$$V_{Lr,p\text{-}p} = V_m\left(\frac{T_o}{2RC}\right) = V_m\left(\frac{1}{2f_o RC}\right)$$

## Example

- Find the ripple factor r




- $V_{L,dc} = V_m - \frac{1}{2}\frac{V_m}{2f_o R_{Lc}} = 41.54\ v$

  $V_{Lr,p-p} = \frac{V_m}{2f_o R_{Lc}} = 1.7677 v$

- RMS (ripple voltage) $= \frac{V_{Lr,p-p}}{2\sqrt{3}} = 0.51 v\ rms$

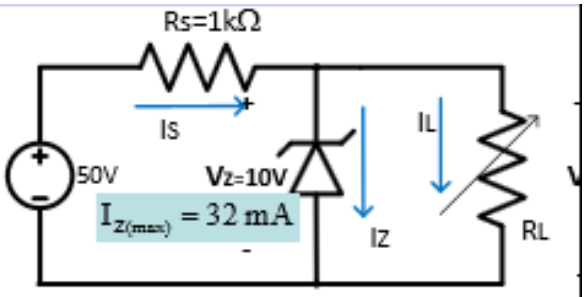
  $\therefore r = \frac{0.51}{41.54} \times 100\%$

  $r = 1.2277\ \%$

## ⇨ Zener Diode VR

# Example

1) Determine Range of $R_L$ & $I_L$ that will result in $V_L$ being maintained at 10V
2) Determine the power rating of the zener diode




*SOLUTION*

1) To find $R_{L(min)}$ that will turn the zener diode ON :

$$V_L = V_Z = \frac{R_L}{R_L + R_s} V_i \Rightarrow$$

$$R_L = \frac{R_s}{V_i - V_Z} V_Z$$

$$R_{L(min)} = \frac{1\,k\Omega}{50-10} 10 = 250\,\Omega$$

$$250\,\Omega \le R_L \le 1.25\,k\Omega$$

2) To find $R_{L(max)} \Rightarrow$ we need $I_{L(min)}$

$$I_{L(min)} = I_s - I_{Z(max)}$$

$$I_s = \frac{V_i - V_Z}{R_s} = \frac{50-10}{1\,k\Omega} = 40\,mA$$

$$I_{L(min)} = 40 - 32 = 8\,mA$$

$$\Downarrow$$

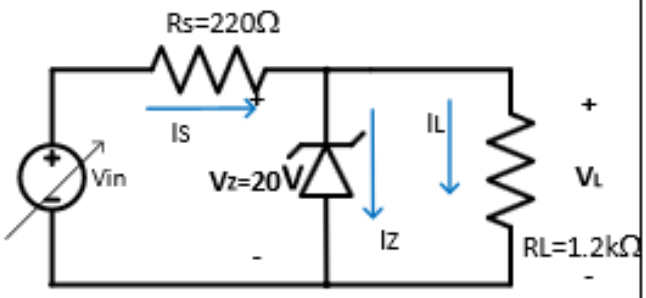
$$R_{L(max)} = \frac{V_L}{I_{L(min)}} = \frac{10\,V}{8\,mA} = 1.25\,k\Omega$$

3) $P_{Z(max)} = V_Z . I_{Z(max)} = 10\,V \;.\; 32\,mA = 320\,mW$

The zener diode is chosen with power rating $\ge P_{Z(max)}$

# Example

*Find the range of values of Vi that will maintain the zener in the ON (regulation ) State*




$$V_{in(min)} = \frac{R_L + R_s}{R_L} V_Z$$

$$= \frac{1200 + 220}{1200} 20 = 23.07\,V$$

$$I_s = I_Z + I_L$$

$$I_{S(max)} = I_{z(max)} + I_L$$

$$I_L = \frac{V_L}{R_L} = \frac{20\,V}{1200\,\Omega} = 16.67\,mA$$

$$I_{S(max)} = 60\,mA + 16.67\,mA = 76.67\,mA$$

$$V_{i(max)} = (76.67\,mA).(220\,\Omega) + 20\,V = 36.87\,V$$

$I_{Z(max)} = 60$ mA

$$\therefore\; 23.07\,V \le V_{in} \le 36.87\,V$$

## 2. BJT dc analysis

### Transistor biasing:

✓In order to operate properly as an amplifier, it's necessary to correctly bias the two pn-junctions with external voltages.

✓Depending upon external bias voltage polarities used; the transistor works in one of **four regions** (modes).

✓ For transistor to be used as an Active device **(Amplifier);** the emitter-base junction must be forward bias, while the collector-base junction must be reverse biased.

npn transistor modes of operation

| Junction/ Mode | BE | BC | Remarks |
|---|---|---|---|
| **Saturation Mode** | Forward | Forward | Equivalent to short circuit<br>Ic=Ic(sat)<br>Vce=Vce(sat)=~ 0.2V |
| **Active Mode (Linear Region)** | Forward | Reverse | Ic proportional to Ib<br>Vce defined by circuit |
| **Cut-off Mode** | Reverse | Reverse | Equivalent to open circuit<br>Ic=Ib=0<br>Vce defind by circuit |
| Inverse Mode | Reverse | Forward | Rarely used and will not be discussed in this course |

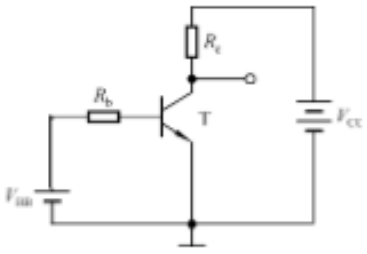
# Basic BJT Amplifiers Circuits

**BJT in Active Mode** $I_E=I_B+I_C$

$$\alpha \approx \frac{I_C}{I_E}$$

$$\beta \approx \frac{I_C}{I_B}$$ ---common-emitter current gain

$$\beta = \frac{\alpha}{1-\alpha}$$




**BJT DC Analysis**

- Make sure the BJT current equations and region of operation match

  $V_{BE} > 0$,
  $V_{BC} < 0$, → $V_E < V_B < V_C$

- Utilize the relationships ($\beta$ and $\alpha$) between collector, base, and emitter currents to solve for all currents

$$\begin{cases} I_E = I_C + I_B = (1+\beta) I_B \\ I_C = \beta I_B \\ I_C = \alpha I_E \end{cases}$$

1. In the cutoff region :

$I_B = I_C = I_E = 0$

2. In the active region :

$I_C = \alpha I_E$

$I_C = \beta I_B$

$I_E = (\beta+1) I_B$

3. In the saturation region :

$V_{CE} = V_{CE,sat}$

$V_{BE} = 0.7\,v$ , Si , npn

$V_{BE} = -0.7\,v$ , Si , pnp

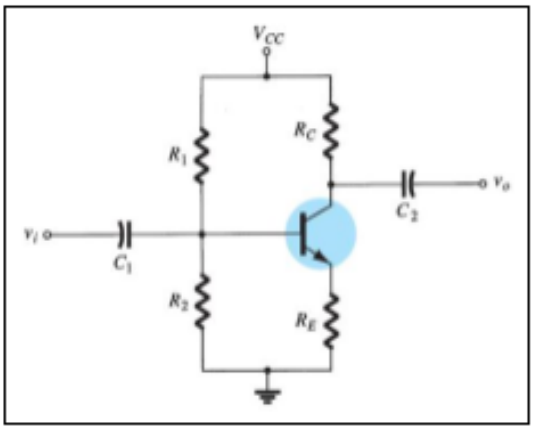
$V_{CE} > V_{CE,sat} = 0.2\,v$ , Si , npn

$V_{CE} < V_{CE,sat} = -0.2\,v$ , Si , pnp

# 4) Voltage Divider Bias

***This is a very stable bias circuit.***

The currents and voltages are nearly independent of any variations in β if the circuit is designed properly



## Exact Analysis

**We must try to make $I_B$ as close as possible to zero**

**Thevenin Equivalent circuit for the circuit left of the base is done**

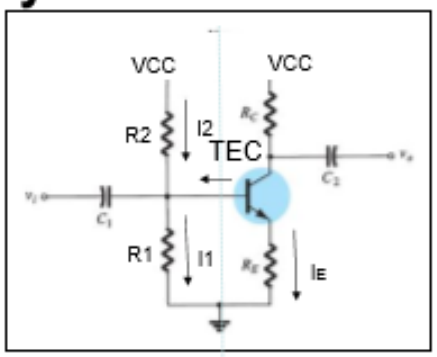
$$V_{th} = \frac{R_1 V_{CC}}{R_1 + R_2}$$

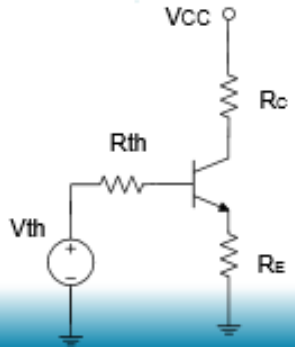
$$R_{th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

$$\text{but } I_B = \frac{I_E}{\beta + 1}$$

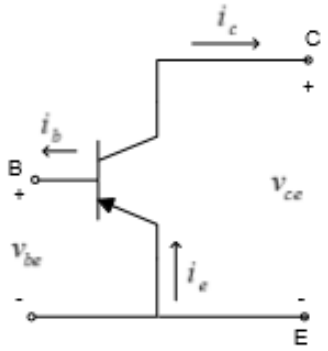
$$\therefore I_{E(exact)} = \frac{V_{th} - V_{BE}}{\frac{Rth}{\beta + 1} + R_E}$$

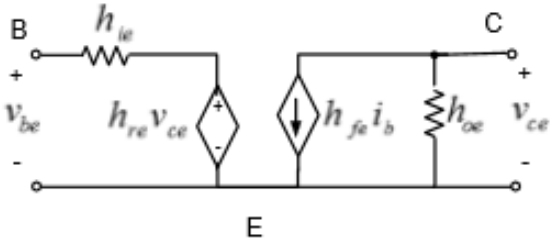


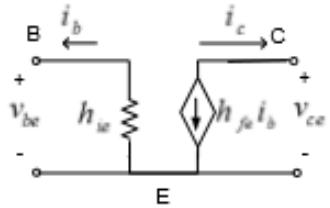




## 3. BJT amplifier ac analysis (Common Emitter, Common Collector, Common Base)

## Common Emitter and Common Collector Configuration



# Value of hie

Base Emitter is a pn junction similar to a diode
hie is the dynamic resistance of the pn junction

In a diode:

$$r_d = \frac{V_T}{I_{DQ}} \Rightarrow$$

$$h_{ie} = \frac{V_T}{I_{BQ}} = \frac{V_T}{\frac{I_{CQ}}{h_{fe}}} = \frac{h_{fe} V_T}{I_{CQ}}$$

$I_{BQ}$ dc value of base current

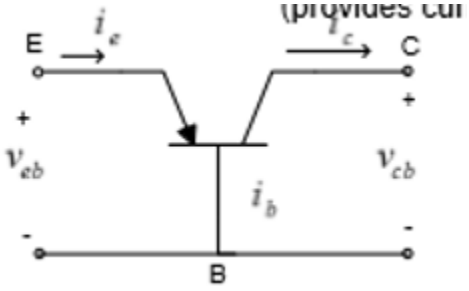
$I_{CQ}$ dc value of collector current

$$h_{fe} = \beta$$

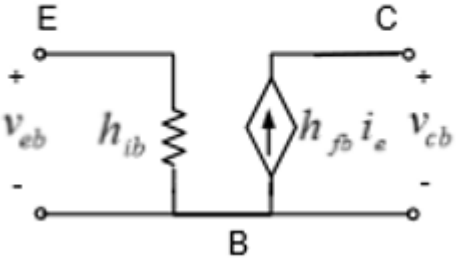
$$V_T = 25.69 \text{ mV } @ 25\,^{\circ}\text{C}$$

# Common-Base Configuration

(provides current gain and some voltage gain)




Simplified Equivalent Circuit




$$h_{ib} = \frac{V_T}{I_{EQ}}$$

$$h_{fb} = \alpha$$

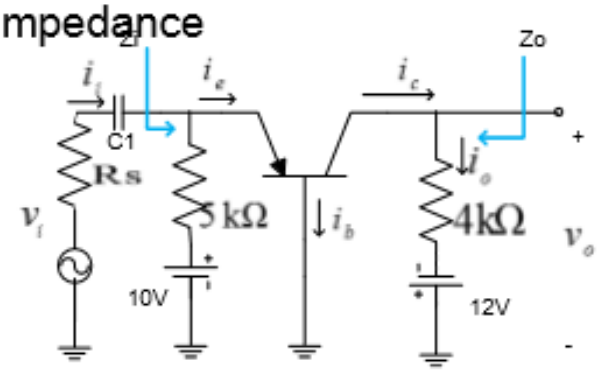
$$V_T = 25.69 \text{ mV } @ 25\,^{\circ}\text{C}$$

$$h_{ie} > h_{ib}$$

# BJT Amplifier Analysis

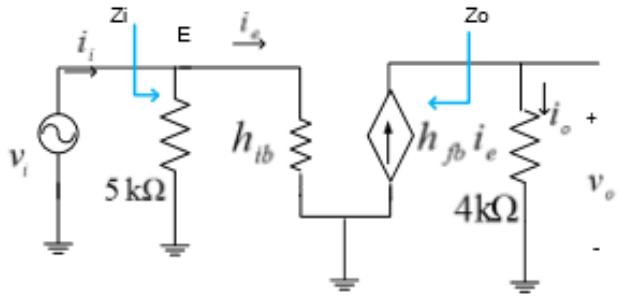
When Analyzing Amplifier Circuits, we usually want to find some or all of the following quantities:

1) Av=Vo/Vi, small signal voltage gain
2) Ai=io/ii, small signal current gain
3) Zi Input Impedance
4) Zo Output Impedance




# BJT Amplifier Analysis

Solution: (with Rs=0)
We draw the ac small signal equivalent circuit
Capacitors ==> replaced by short circuit
DC sources are killed ,



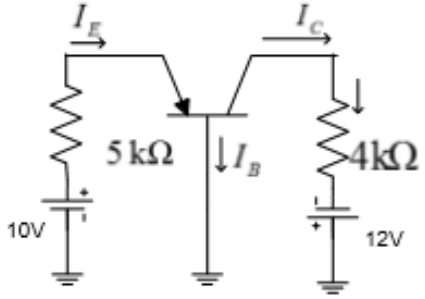

$$h_{ib} = \frac{V_T}{I_{EQ}}$$

$$h_{fb} = \alpha \cong 1$$

$I_{EQ}$ must be calculated from DC analysis

# DC Analysis

DC Equivalent Circuit:
-Cap ==> open
-Kill ac sources ==>




$$10 = 5\,\text{k}\Omega\,.\,\text{I}_{\text{EQ}} + \text{V}_{\text{EB}}$$

$$\text{I}_{\text{EQ}} = \frac{10 - 0.7}{5\,\text{k}\Omega} = 1.86\,\text{mA}$$

$$\text{h}_{\text{ib}} = \frac{\text{V}_\text{T}}{\text{I}_{\text{EQ}}} = \frac{25.69\,\text{mV}}{1.86\,\text{mA}} = 13.98\,\Omega$$

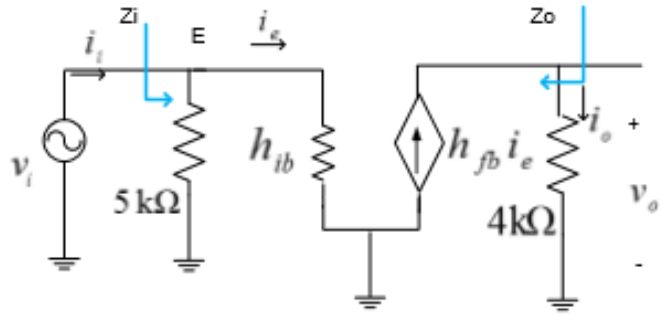
# Ac ss equivalent circuit

$$1)\ \text{A}_\text{V} = \frac{v_o}{v_i}$$

$$v_o = i_o\,.\,4\,\text{k}\Omega$$

$$i_o = h_{fb}\,.\,i_e$$

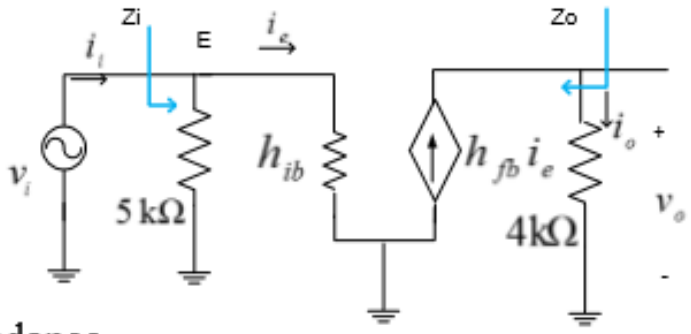
$$i_e = \frac{v_i}{h_{ib}}$$




$$\text{A}_\text{V} = \frac{v_o}{v_i} = \frac{v_o}{i_o}\,.\,\frac{i_o}{i_e}\,.\,\frac{i_e}{v_i} \quad \Rightarrow \quad \text{A}_\text{V} = (4\,\text{k}\Omega)\,.\,(h_{fb})\left(\frac{1}{h_{ib}}\right)$$

$$= (4\,\text{k}\Omega)\,.\,(1)\left(\frac{1}{13.98}\right) = 286 > 1$$

# Zi & Zo




3) Input Impedance

$$Z_i = (h_{ib} // 5\,\text{k}\Omega) = \left( \frac{h_{ib}.5\,\text{k}\Omega}{5\,\text{k}\Omega + h_{ib}} \right)$$

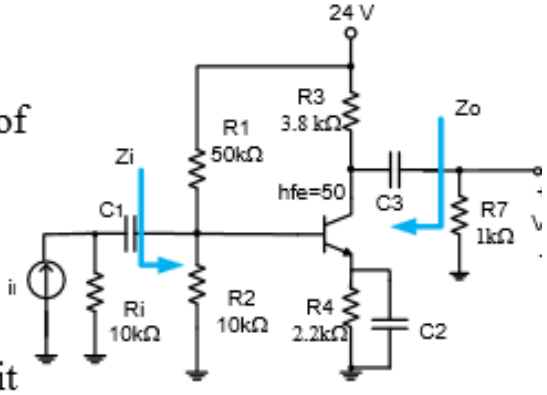
4) Output Impedance

$$Z_o\Big|_{\text{all independant sources killed (i.e. Vi=0 or short)}} = 4\,\text{k}\Omega$$

# Example: Common Emitter (CE)

1) From DC Analysis,
we find Q - point and value of

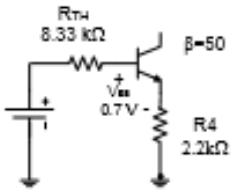
$$h_{ie} = \frac{V_T}{I_{BQ}}$$




Thevenin's equivalent circuit
as seen from the base

$$V_{TH} = \frac{10\,\text{k}\Omega}{10\,\text{k}\Omega + 50\,\text{k}\Omega}.24\,\text{V} = 4\,\text{V}$$

$$R_{TH} = 10\,\text{k}\Omega\Omega // 5\text{k}\Omega = 8.33\,\text{k}\Omega$$

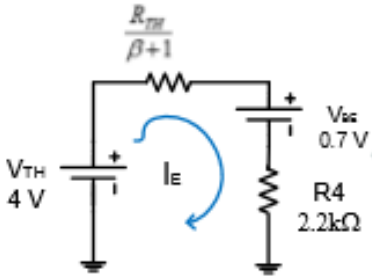



$$4 = 8.33\,\text{k}\Omega \cdot I_B + V_{BE} + 2.2\,\text{k}\Omega \cdot I_E$$

But, $I_E = (1+\beta) I_B$

$$\text{Solve for } I_E = \frac{4 - 0.7}{\frac{8.33\,\text{k}\Omega}{(1+50)} + 2.2\,\text{k}\Omega} = 1.4\,\text{mA}$$

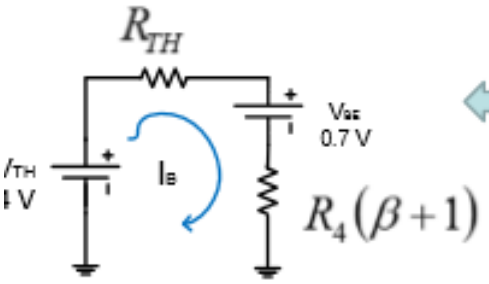
$$h_{ie} = \frac{V_T}{I_{B\Omega}} = \frac{25.69\,\text{mV}}{\frac{1.4\,\text{mA}}{51}} = 928\,\Omega$$




Here we have base reflected to emitter

$$I_B \Rightarrow I_E = (\beta+1) I_B$$

$$R_B \Rightarrow \frac{R_B}{\beta+1}$$

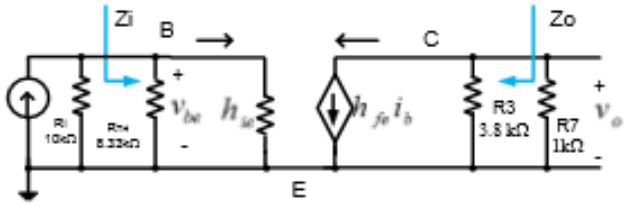



Here we have emitter reflected to base

$$I_E \Rightarrow I_B = \frac{I_E}{(\beta+1)}$$

$$R_E \Rightarrow R_E(\beta+1)$$

# AC small signal Equivalent Circuit




1) $A_V = \frac{v_o}{v_i}$

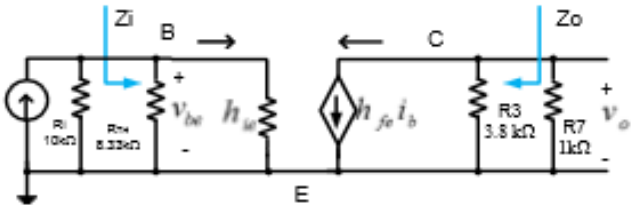
$$A_V = \frac{v_o}{v_i} = \frac{v_o}{i_b}.\frac{i_b}{v_i}$$

$v_o = -h_{fe} i_b . (R_3 // R_7)$ ⇒ $= -h_{fe} . (R_3 // R_7)\left(\frac{1}{h_{ie}}\right)$

$i_b = \frac{v_i}{h_{ie}}$

$$= -50.(3.8\,k\Omega // 1\,k\Omega)\left(\frac{1}{928\,\Omega}\right) = -42.7$$

# AC small signal Equivalent Circuit




2) $Z_I = R_{TH} // h_{ie}$

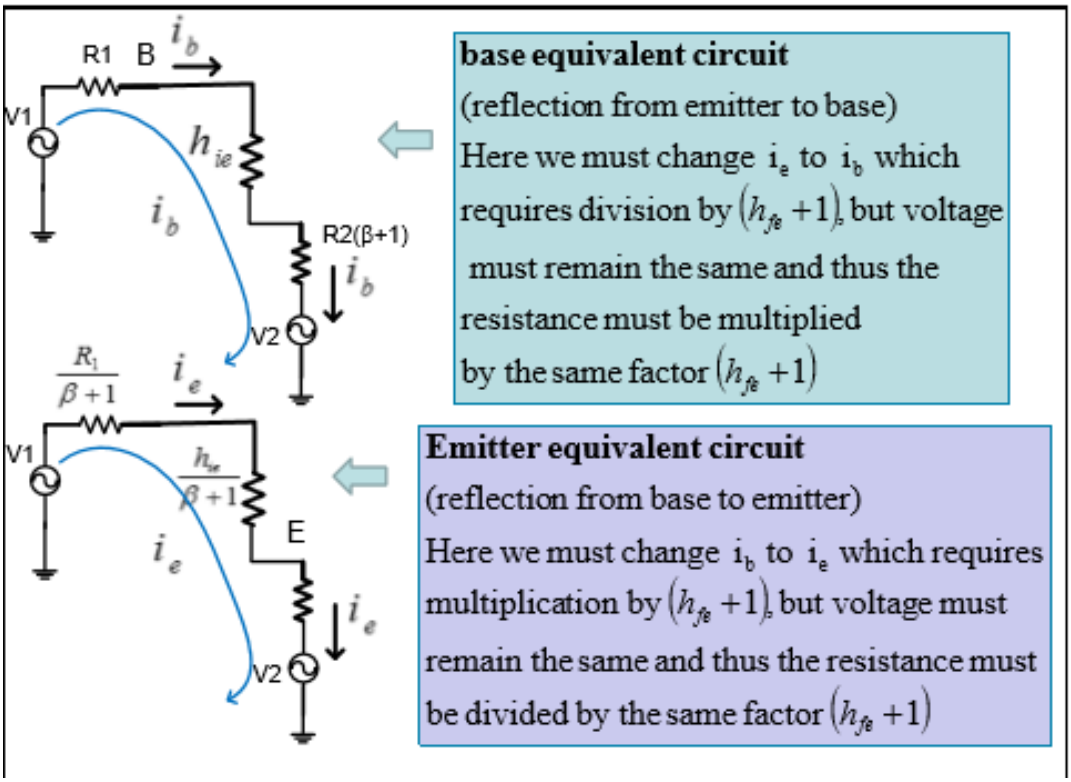
$= 8.33\,k\Omega // 928\,\Omega$

only elements to the right of arrow are considered

according to the given direction of the arrow

3) $Z_o\big|_{\text{all independant sources killed (i.e. Vi=0 or short)}} = 3.8\,k\Omega$

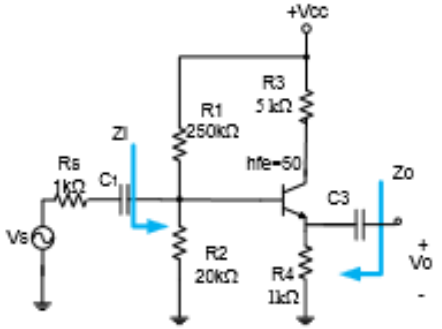
here $h_{fe}.i_b = 0$ since $i_b = 0$ (vi = 0 - killed)




**base equivalent circuit**
(reflection from emitter to base)
Here we must change $i_e$ to $i_b$ which requires division by $(h_{fe}+1)$, but voltage must remain the same and thus the resistance must be multiplied by the same factor $(h_{fe}+1)$

**Emitter equivalent circuit**
(reflection from base to emitter)
Here we must change $i_b$ to $i_e$ which requires multiplication by $(h_{fe}+1)$, but voltage must remain the same and thus the resistance must be divided by the same factor $(h_{fe}+1)$

# Common Collector Amplifier



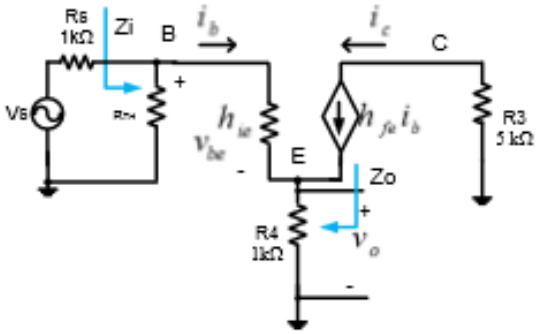

*Given*

$h_{ie} = 1\text{k}\Omega$

$h_{fe} = \beta = 50$

Find Av, Ai, Zi, Zo

**AC small signal Equivalent Circuit**

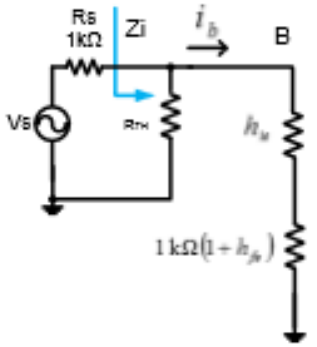



$$1)\ A_V = \frac{v_o}{v_s}$$

$$v_o = 1\text{k}\Omega \cdot i_e$$

$$i_e = i_b(h_{fe}+1)$$

$i_b$ can be found from base equivalent circuit




$$R_{TH} = 20\,k\Omega // 250\,k\Omega$$

$$i_b = i_i \frac{R_{TH}}{(R_{TH}) + (h_{ie} + 1\,k\Omega(h_{fe}+1))}$$

$$i_i = \frac{V_S}{R_S + (R_{TH} // (h_{ie} + 1\,k\Omega(h_{fe}+1)))}$$

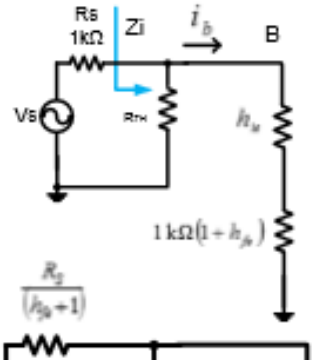
$$\therefore A_V = \frac{v_o}{v_S} = \frac{v_o}{i_e}.\frac{i_e}{i_b}.\frac{i_b}{i_i}.\frac{i_i}{v_S}$$

$$= (1k\Omega).(h_{fe}+1)\left(\frac{R_{TH}}{(R_{TH}) + (h_{ie} + 1\,k\Omega(h_{fe}+1))}\right)\left(\frac{1}{R_S + (R_{TH} // (h_{ie} + 1\,k\Omega(h_{fe}+1)))}\right)$$

$$= 0.915 < 1$$

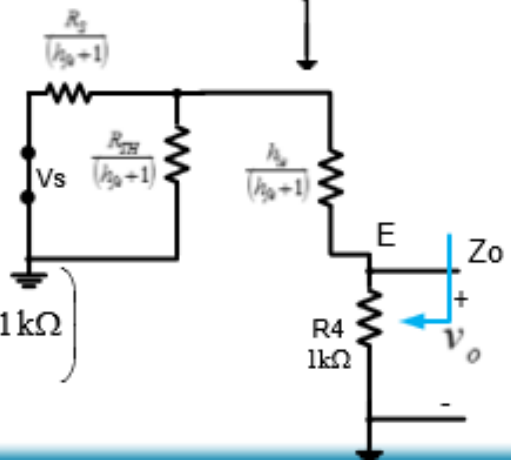
3) $Z_I = (R_{TH} // (h_{ie} + 1\,k\Omega(h_{fe}+1)))$

$= 13.66\,k\Omega$ (high)




Emitter Equivalent Circuit

& $V_S = 0$




$$Z_o\big|_{V_S=0} = \left(\frac{(R_S // R_{TH}) + h_{ie}}{(h_{fe}+1)} // 1\,k\Omega\right)$$

$$= \left(\left(\left(\frac{R_S}{(h_{fe}+1)} // \frac{R_{TH}}{(h_{fe}+1)}\right) + \frac{h_{ie}}{(h_{fe}+1)}\right) // 1\,k\Omega\right)$$

$= 36.8\,\Omega$ (low)

# 4. FET dc analysis

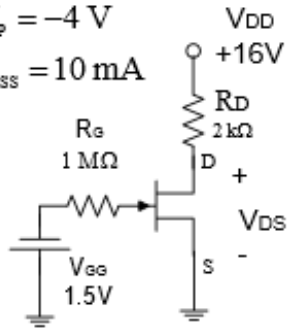
## Example

$V_{GS} = V_G - V_S = -1.5 - 0 = -1.5\ \text{V}$

Assuming JFET is in pinch off region

$V_P = -4\ \text{V}$

$I_{DSS} = 10\ \text{mA}$




1) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 10\ \text{mA}\left(1 - \frac{-1.5}{-4}\right)^2$

$= 3.9\ \text{mA}$

2) $V_{DS} = V_{DD} - I_D R_D$

$= 16 - ((2\text{k})(3.9\ \text{mA}))$

$= 8.2\ \text{V}$

3) check for $|V_{DS}| > |V_p| - |V_{GS}|$ ?

$|8.2| > |-4| - |-1.5|$

assumption is true

19

## Example

$V_S$ must be more positive than $V_G$

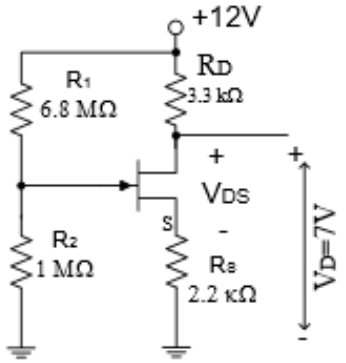
to keep the gate – source junction reverse biased

$V_S = I_D R_S$

$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - I_D R_S$




$V_D = V_{DD} - I_D R_D = 7\ \text{V}$

$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12 - 7}{3300} = 1.52\ \text{mA}$

28

# Example

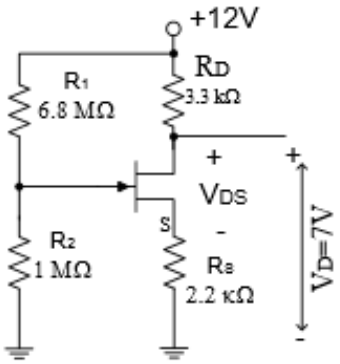
$$V_S = I_D R_S = (1.52\text{mA})\,(2.2\text{k}\Omega) = 3.34\text{ V}$$

$$V_G = \frac{1\text{M}}{1\text{M}+6\text{M}}15 = 1.54\text{ V}$$

$$V_{GS} = 1.54 - 3.34 = -1.8\text{ V} < 0 \quad \Leftarrow \text{OK}$$

also

$$\text{I}_\text{D} = \frac{\text{V}_\text{S}}{\text{R}_\text{S}} = \frac{3.34}{2200} = 1.52\text{ mA}$$




# Example

Suppose that the DMOSFET is in the pinch off region

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{.....1}$$

$$V_{GS} = V_G - V_S = V_G$$

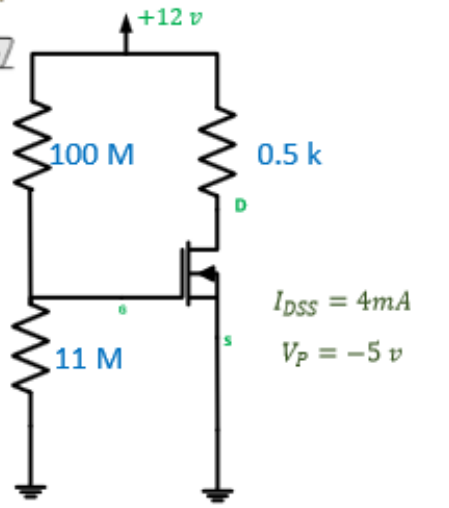
$$V_G = \frac{11M}{11M+100M}(12) = 1.19\text{ v} \quad \text{.....2}$$

sub 2 into 1 , we obtain

$I_{DS}$= 6.13mA > $I_{DSS}$ !! **THIS IS POSSIBLE AND DMOSFET WILL OPERATE IN ENHANCEMENT MODE**

$V_{DS} = V_{DD}$ - 0.5K $I_{DS}$ = 8.93 v

$V_{DS} >^{?} V_{GS} - V_P$ = 6.19 v



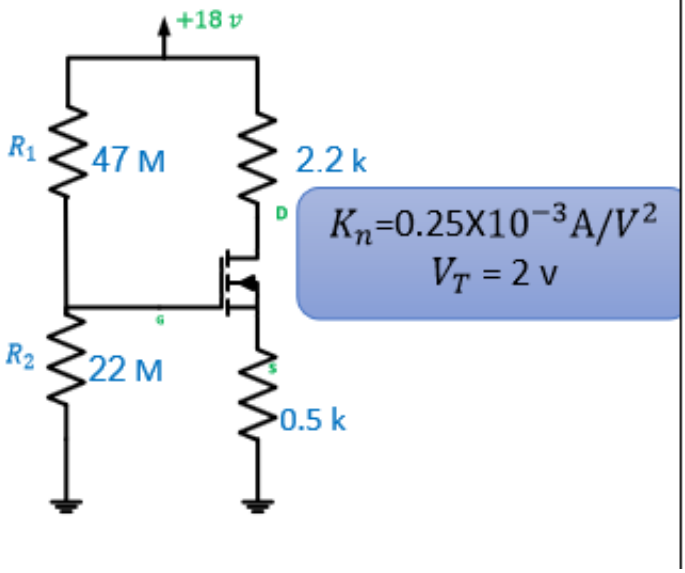

$I_{DSS}$= 4mA $V_P$= - 5 v

# Example

$I_{DS}= K_n(V_{GS} - V_T)^2$ .....1

$V_{GS}= V_G - V_S$

$V_G= \frac{22M}{22M+47M}(18) = 5.74v$

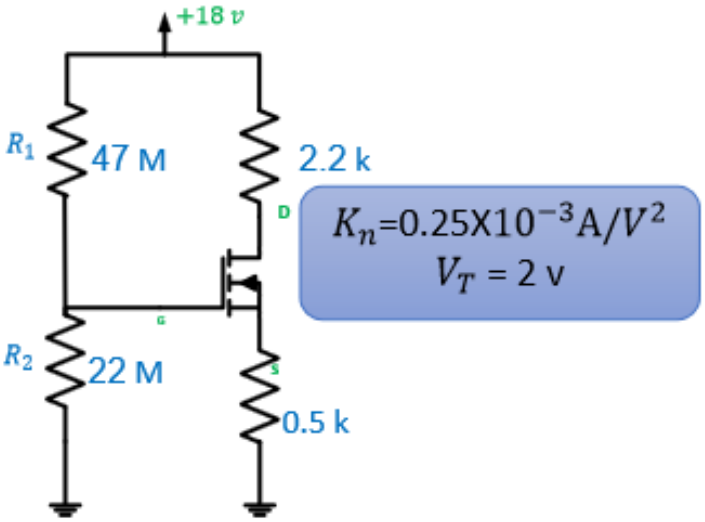



$V_S= (0.5K)\ I_{DS}$

$V_{GS}= 5.74 - (0.5K)\ I_{DS}$.....2

solving for $V_{GS}$:

$V_{GS}$= 4.78v √
= -8.78v X




$I_{DS}$=1.92m A

$V_{DS}$= 12.82> | $V_{GS} - V_T$|

## 5. FET amplifier ac analysis

### Definition: Transconductance $g_m$

For JFETs and DMOSFETs

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \qquad g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

For EMOSFET

$$I_D = K(V_{GS} - V_{GS(TH)})^2 \Rightarrow g_m = \frac{\partial I_D}{\partial V_{GS}} = 2K(V_{GS} - V_{GS(TH)})$$

$$K = \frac{I_D}{(V_{GS} - V_{GS(TH)})^2}$$

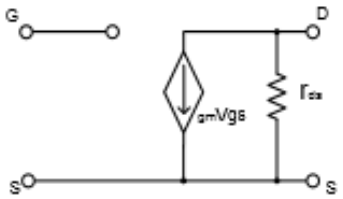
$$(V_{GS} - V_{GS(TH)}) = \sqrt{\frac{I_D}{K}}$$

$$\therefore g_m = 2K\sqrt{\frac{I_D}{K}} = 2\sqrt{\frac{I_D K^2}{K}} = 2\sqrt{I_D K}$$

### AC Small Signal Equivalent Circuit (MODEL Valid for all FET Types)

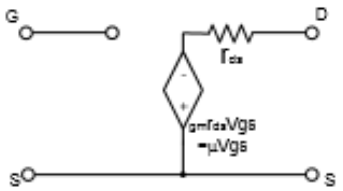
- In ac

$$g_m = \frac{i_d}{v_{gs}} \Rightarrow i_d = g_m v_{gs}$$




- Or

$\mu = g_m r_{ds}$ - amplification factor



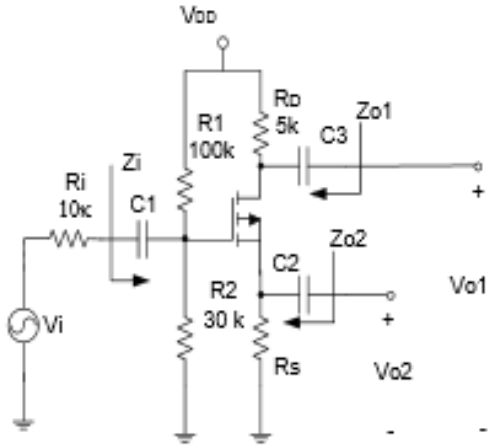
# Example: Phase Splitting circuit

- Two outputs:
  - Vo1 from drain
  - Vo2 from source

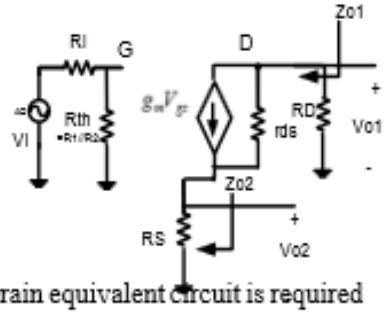
Find $A_V, A_I, Z_{O1}, Z_{O2}$ and $Z_I$

$r_{ds} = 100\,k\Omega$

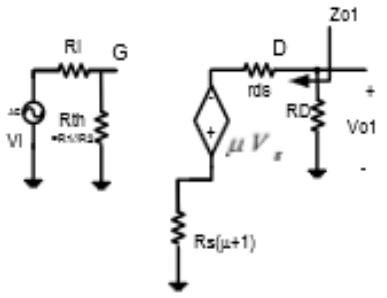
$g_m = 1\,mS$




# Solution: ac ss equivalent circuit




1) To Find $Z_{O1}, V_{O1}$ Drain equivalent circuit is required since both of these quantities are seen from the drain

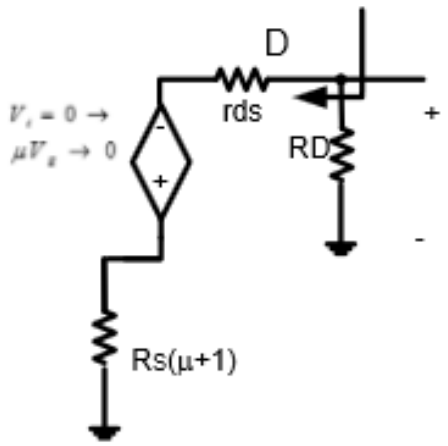


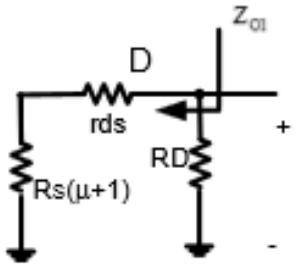

$$V_{o1} = \frac{R_D}{R_D + r_{ds} + R_S(\mu+1)}\left(-\mu V_g\right)$$

$$V_g = V_i \frac{R_{ik}}{R_{ik} + R_i}$$

$$Av = \frac{V_{o1}}{V_i} = (-\mu)\frac{R_D}{R_D + r_{ds} + R_S(\mu+1)} \cdot \frac{R_{ik}}{R_{ik} + R_i}$$

2) To Find $Z_{O1}\big|_{\substack{Vi=0\\Vg=0}}$

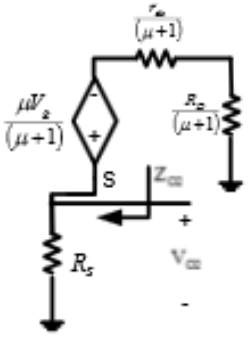



$$Z_{O1}\big|_{\substack{Vi=0\\Vg=0}} = R_D \,//\left[r_{ds} + R_s(\mu+1)\right]$$

# Solution: continued

3) To Find $Z_{O2}$, $V_{O2}$ Source equivalent circuit is required since both of these quantities are seen from the source

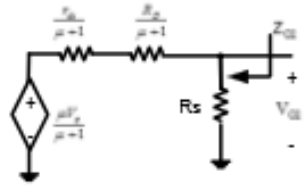



Reflection Drain to Source

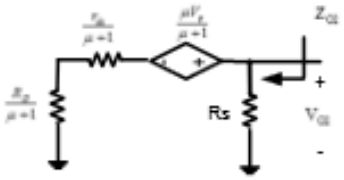
$$\mu V_{gs} \Rightarrow \frac{\mu V_g}{(\mu+1)}$$

$$R_D \Rightarrow \frac{R_D}{(\mu+1)}$$

$$r_{ds} \Rightarrow \frac{r_{ds}}{(\mu+1)}$$




$$V_{o2} = \frac{R_S}{\dfrac{R_D + r_{ds}}{(\mu+1)} + R_S}\left(\frac{\mu V_g}{(\mu+1)}\right)$$

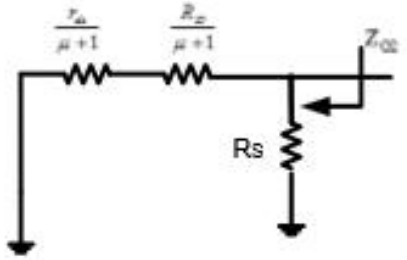



$$V_g = V_i \frac{R_{ik}}{R_{ik} + R_i}$$

$$A_{v2} = \frac{V_{o2}}{V_i} = \frac{\mu}{(\mu+1)} \frac{R_S}{\dfrac{R_D + r_{ds}}{(\mu+1)} + R_S} \cdot \frac{R_{ik}}{R_{ik} + R_i}$$

# Solution: continued

4) To Find $Z_{O2}\big|_{\substack{Vi=0\\Vg=0}}$




$$Z_{O2}\Big|_{\substack{Vi=0\\Vg=0}} = R_S \,//\left[\frac{r_{ds}+R_D}{(\mu+1)}\right]$$

$$Z_{O2}\Big|_{\substack{Vi=0\\Vg=0}}\Big|_{r_{ds}\to\infty} = R_S \,//\,\frac{1}{g_m}$$

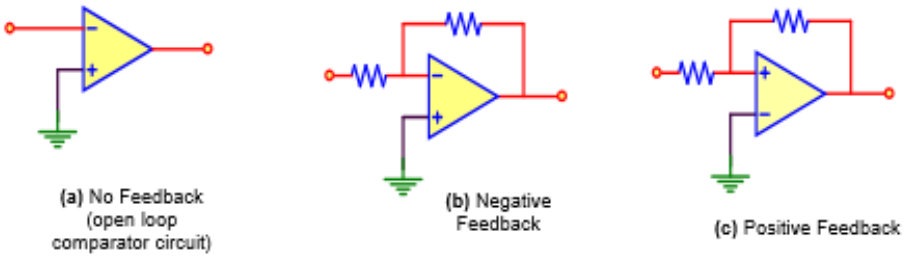
since $\lim_{r_{ds}\to\infty} \frac{r_{ds}+R_D}{\mu+1} = \lim \frac{\frac{r_{ds}}{r_{ds}}+\frac{R_D}{r_{ds}}}{\frac{g_m r_{ds}}{r_{ds}}+\frac{1}{r_{ds}}}$

$= \lim_{r_{ds}\to\infty} \frac{1+\frac{R_D}{r_{ds}}}{g_m+\frac{1}{r_{ds}}} = \frac{1}{g_m}$

$$Z_i = R_{th} = R_1 \,//\, R_2$$

# 6. Op-amp circuits

## OP-AMP CONFIGURATIONS

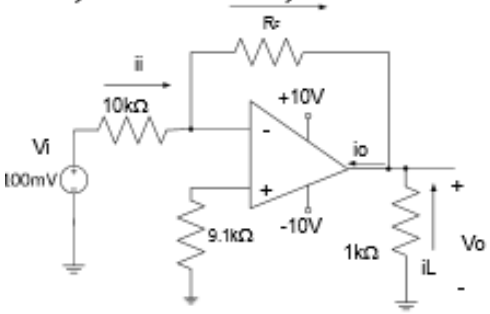



- No feedback : Open loop (used in comparators)
- Negative feedback : Feedback to the inverting input (Used in amplifiers)
- Positive feedback : Feedback to the non inverting input (Used in oscillators) and Schmitt triggers ( comparators with hysterisis)

**Example**

**Find the value of Vo and Io and verify if the opamp is in linear or saturation mode for two values of feedback resistor; assume Io(max)=20 mA:**

**1) $R_F$=100kΩ 2)if$R_F$=2MΩ**




$$V_p = V(+) = 0V$$

$$i_1 = \frac{V_1}{R_1}$$

$$i_i = i_f = \frac{V_i}{10k} = \frac{100\,mV}{10\,k\Omega} = 10\,\mu A$$

$$1)\ V_o = -\frac{R_F}{10\,k\Omega} V_i = -10\,V_i = -1V$$

$$V_o > -V_{sat}$$

Linear mode

**Important**

**Io(max) is few mA for most opamps which limits the values of resistors to be used to kohm range**

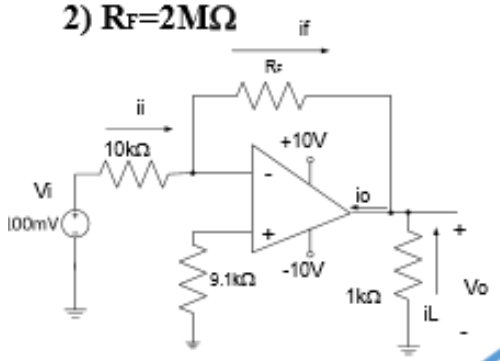
$$i_o = i_f + i_L$$

$$i_L = \frac{1V}{1k} = 1mA$$

$$i_o = 10\mu A + 1mA = 1.01mA < Io(max)$$

**Example continued**

**2) $R_F$=2MΩ**




$$i_i = i_f = \frac{V_i}{10k} = \frac{100mV}{10k} = 10\ \mu A$$

$$2) V_o = -\frac{R_F}{10k} V_i = -200V_i = -20V$$

$$V_o < -V_{sat}$$

Saturation mode $\Rightarrow V_o$ is limited to $-V_{sat}$

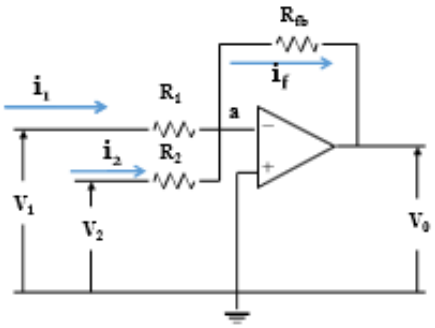
$$\therefore V_o = -V_{sat} = -8V$$

$$i_L = \frac{8V}{1k} = 8mA$$

$$i_o = 10\,\mu A + 8mA = 8.01mA < Io(max)$$

## Inverting Adder or Summing Amplifier

**Summing Amplifier: This is an application of inverting amplifier**




$$V_p = V_{(+)} = 0V$$

$$i_1 = \frac{V_1}{R_1} \qquad i_2 = \frac{V_2}{R_2}$$

$$V_o = -R_f i_f$$

$$i_f = i_1 + i_2$$

$$V_0 = -\left[\left(\frac{R_{fb}}{R_1}\right)V_1 + \left(\frac{R_{fb}}{R_2}\right)V_2\right] \qquad V_o = -R_f\left[i_1 + i_2\right]$$

**If $R_1 = R_2 = R_{fb}$ then,**

$$V_0 = -\left[V_1 + V_2\right]$$

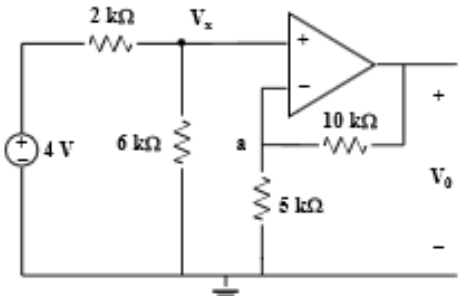
**Therefore, we can add signals with an op amp**

## Example: Non-inverting Amplifiers

**Example: Find $V_0$ for the following op amp configuration.**

$$V_x = \frac{6k}{6k + 2k}4V$$

$$V_x = 3V$$




$$V_o = \left(1 + \frac{R_F}{R_i}\right)V_x$$

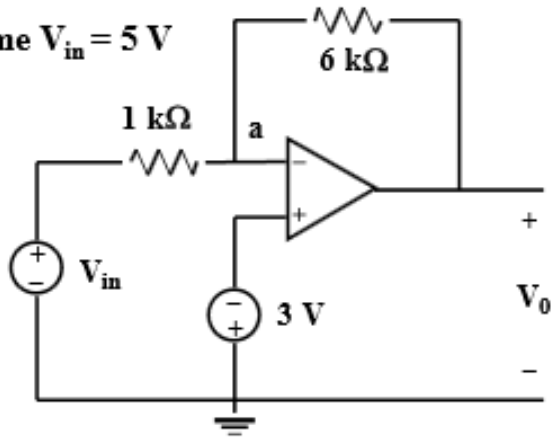
$$V_o = \left(1 + \frac{10k}{5k}\right)3V$$

$$V_o = 9V$$

Make sure that : $-V_{sat} < V_o < +V_{sat}$

**Example** Consider the op amp configuration below.

**Assume $V_{in} = 5$ V**




$$V_0 = (1+\frac{6k}{1k})(-3)-(\frac{6k}{1k})(5)$$
$$= -21-30 = -51V$$

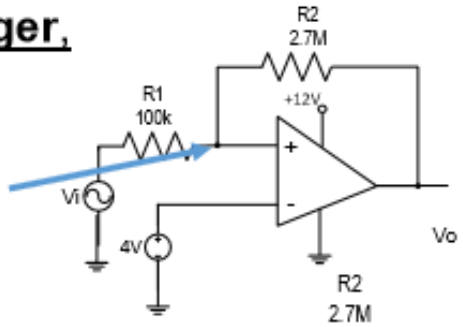
**Since $V_0 = -51$ V** **(op amp will saturate and Vo will be limited to -Vsat)**

## Schmitt trigger,

**Example: Find and sketch Vo(t) and the plot of Vo=f(Vi)**

**Solution: this is a Schmitt trigger and**

$$Vo = \pm \text{Vsat}$$




1) let $V_o = +Vsat$

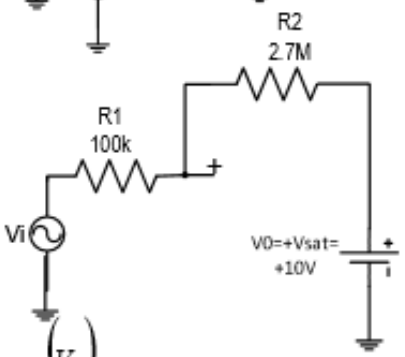
in order for Vo to be + Vsat

Vd > 0

Vd = V(+) – V(–) > 0

V(+) > V(–)

V(–) = 4V




$$V(+) = \frac{100k}{(2700+100)k}(+Vsat)+\frac{2700k}{(2700+100)k}(V_i)$$

$$\frac{100k}{(2700+100)k}(+Vsat)+\frac{2700k}{(2700+100)k}(V_i) > 4V$$

$$\frac{100k}{(2700+100)k}(10V)+\frac{2700k}{(2700+100)k}(V_i)>4V$$

$$(V_i)>\left[4V-\left(\frac{100k}{(2700+100)k}(10V)\right)\right]\left[\frac{(2700+100)k}{2700k}\right] \Longrightarrow V_i>3.777V$$

when $V_i > 3.777 \Rightarrow$ Vo $= +Vsat$; But when $V_i < 3.777 \Rightarrow$ Vo switches to $-Vsat$

2) let $V_o = -Vsat = (0+2) = 2V$

in order for Vo to be - Vsat ==> Vd < 0 ; ∴ V(+) < V(−)

$$V(+)=\frac{100k}{(2700+100)k}(-Vsat)+\frac{2700k}{(2700+100)k}(V_i)$$

$$\frac{100k}{(2700+100)k}(-Vsat)+\frac{2700k}{(2700+100)k}(V_i)<4V$$

$$(V_i)<\left[4V-\left(\frac{100k}{(2700+100)k}(2V)\right)\right]\left[\frac{(2700+100)k}{2700k}\right] \Longrightarrow V_i<4.074V$$

when $V_i < 4.074V \Rightarrow$ Vo $= -Vsat$; But when $V_i > 4.074 \Rightarrow$ Vo switches to $+Vsat$

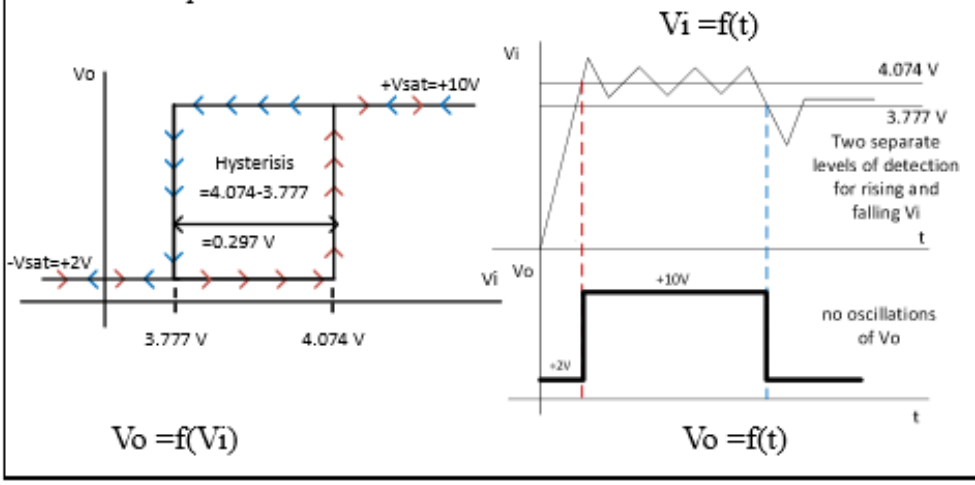
*Conclusion*

1) when Vi is decreasing , as long as Vi is $>3.777$V $\Rightarrow$ Vo $= +Vsat$;

but when $V_i$ becomes $< 3.777 \Rightarrow$ Vo switches to $-Vsat$

2) when Vi is increasing , as long as Vi is $<3.777$V $\Rightarrow$ Vo $= -Vsat$;

but when $V_i$ becomes $> 3.777 \Rightarrow$ Vo switches to $+Vsat$



## Integrator

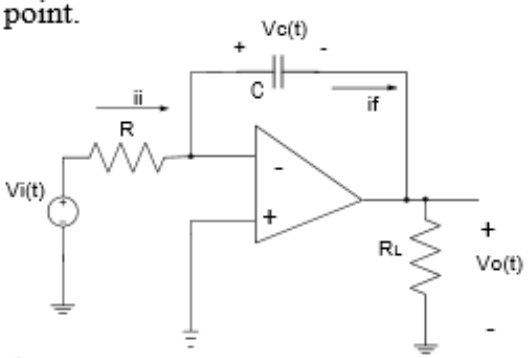
- So far, the input and feedback components have been resistors. If the feedback component used is a capacitor,, the resulting connection is called an *integrator*.
- Recall that virtual ground means that we can consider the voltage at the junction of $R$ and $X_C$ to be ground (since $V_C = 0$ V) but that no current goes into ground at that point.

$$i_i = i_f = \frac{V_i}{R}$$

$$Vc(t) = \frac{1}{C}\int_0^t i_f(t)dt$$

$$V_o = -Vc(t)$$

$$Vo = -\frac{1}{C}\int_0^t \frac{V_i(t)}{R_i}dt = -\frac{1}{RC}\int_0^t V_i(t)dt$$




## Differentiator

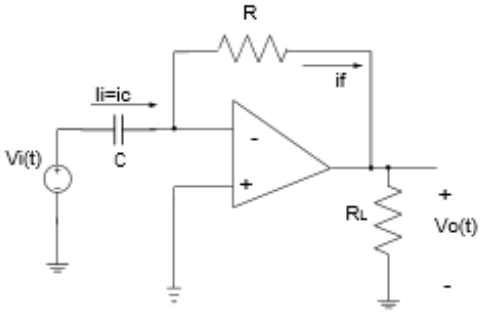
A differentiator ,while not as useful as the circuit forms covered above, the differentiator does provide a useful operation, the resulting relation for the circuit being

$$i_i = i_f = i_C = C\frac{dV_i(t)}{dt}$$

$$Vc(t) = \frac{1}{C}\int_0^t i_f(t)dt$$

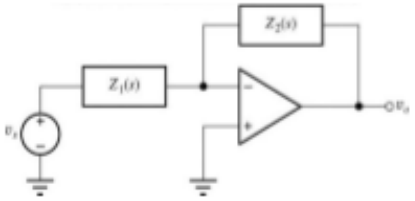
$$V_o = -i_f(t)R$$

$$Vo = -\left(C\frac{dV_i(t)}{dt}\right)(R) = -RC\frac{dV_i(t)}{dt}$$



## The Active Low-pass Filter

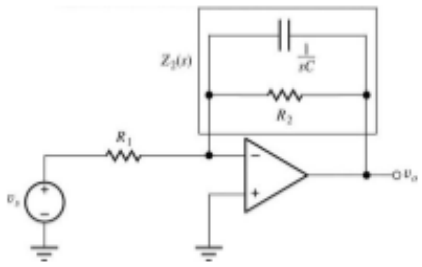
The gain analysis of this inverting amplifier. Note s = jω.



$$A_v = \frac{\tilde{v}_o(j\omega)}{\tilde{v}_s(j\omega)} = -\frac{Z_2(j\omega)}{Z_1(j\omega)} \qquad Z_1(j\omega) = R_1$$

$$Z_2(j\omega) = \frac{R_2 \frac{1}{j\omega C}}{R_2 + \frac{1}{j\omega C}} = \frac{R_2}{j\omega C R_2 + 1}$$

$$A_v = -\frac{R_2}{R_1}\frac{1}{(1 + j\omega C R_2)}$$



$$= \frac{-K}{\left(1 + \frac{j\omega}{\omega_c}\right)}$$

$$K = \frac{R_2}{R_1}$$

& cut-off frequency: $\omega_c = 2\pi f_c = \frac{1}{R_2 C} \quad \therefore f_c = \frac{1}{2\pi R_2 C}$

## Active Low-pass Filter: Example

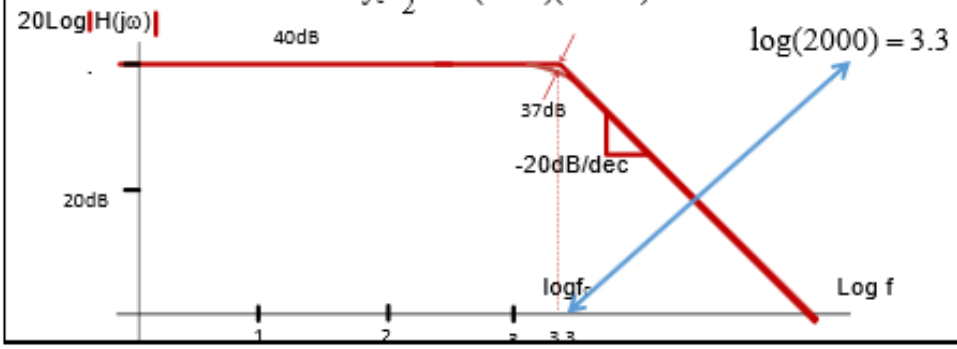
- **Problem**: Design an active low-pass filter
- **Given Data**: $A_v$= 40 dB, $R_{in}$= 5 kΩ, $f_c$ = 2 kHz
- **Assumptions:** Ideal op amp, specified gain represents the desired low-frequency gain.
- **Analysis**: $|A_v| = 10^{40\text{dB}/20\text{dB}} = 100$

  Input resistance is controlled by $R_1$ and voltage gain is set by $R_2$ / $R_1$.

  The cutoff frequency is then set by C.

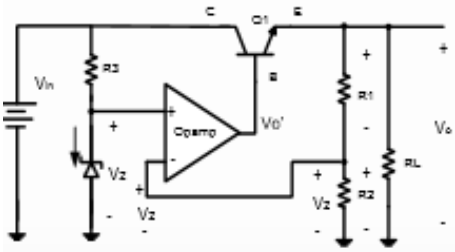
$$R_1 = R_{in} = 5\text{k}\Omega \quad \text{and} \quad |A_v| = \frac{R_2}{R_1} \Rightarrow R_2 = 100R_1 = 500\text{k}\Omega$$

$$C = \frac{1}{2\pi f_c R_2} = \frac{1}{2\pi(2\text{kHz})(500\text{k}\Omega)} = 159\text{pF}$$



# 7. Voltage regulator circuits

## Opamp Series VR




Resistors $R_1, R_2$ are for sampling of Vo (the current through these resistors must be small)

$$V_o = V_{R1} + V_{R2}$$

$$I_{R1} = I_{R2} = I$$

$$V_{R2} = V_Z$$

$$I = \frac{V_Z}{R_2}$$

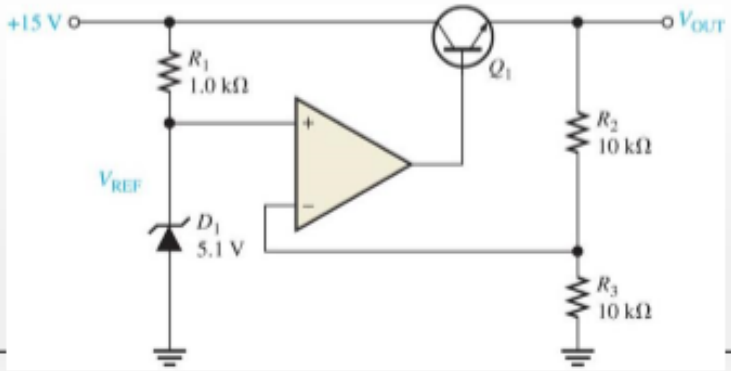
$$V_Z = V_o \frac{R_2}{R_1 + R_2}$$

$$V_o = V_Z\left(1 + \frac{R_1}{R_2}\right)$$

## Example

- Determine the output voltage for the regulator below.

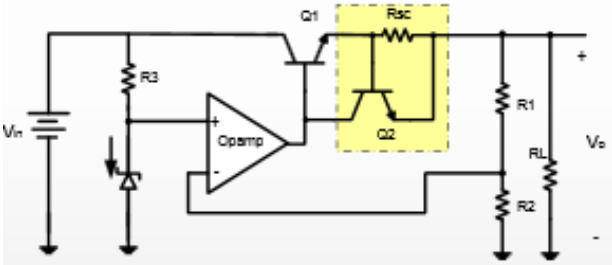
$$V_o = \left(1 + \frac{R_2}{R_3}\right)V_Z \quad \Rightarrow \quad V_o = \left(1 + \frac{10\text{k}}{10\text{k}}\right)5.1 = 10.2\ \text{V}$$



## Opamp Series VR with current limit

Current Limiting Circuit

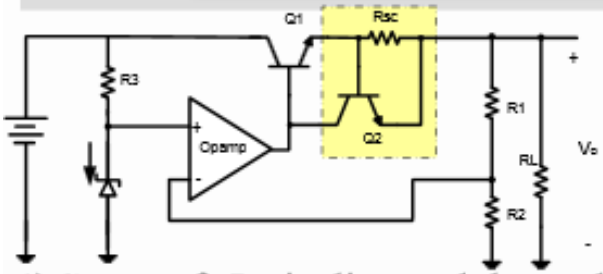
In order to protect the transistor from damage when a very high current passes through it due to a short circuit or excessive current demand at the load




1) In normal operation Q2 is off since $V_{be2} = V_{Rsc} < 0.7\ V$

2) $R_{SC} = \frac{V_{be}}{I_{L(Max)}} = \frac{0.7\ V}{I_{L(Max)}}$

## Opamp Series with current limit




3) When $I > I_{L(Max)}$, Q2 conducts since $V_{be2} = V_{Rsc} \cong 0.7\ V$

4) Some of $I_{B1}$ is diverted through Q2 ($I_{C2}$)

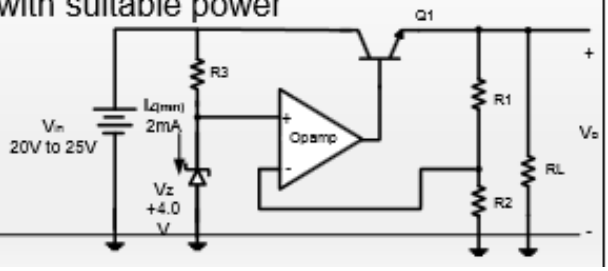
$I_{B1}$ is reduced so that $I_L$ is limited to a maximum value calculated as : $I_{L(Max)} = \frac{V_{be}}{R_{SC}} = \frac{0.7\ V}{R_{SC}}$

5)Since $V_{be2}$ cannot exceed 0.7 V , $V_{R_{sc}}$ is limited

6) This is constant current limiting

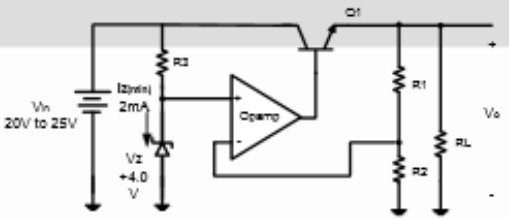
# Voltage Regulators example

- Given the following series voltage regulator
- 1) Complete the design of the following voltage regulator (Find of R1, R2 and R3) assuming that the voltage across the load resistor $R_L$ is equal to 12V. Assume Iz(min) = 2mA.
- 2)Show how to modify the circuit to limit the load current to 1A.
- 3)Find the output voltage for the modified circuit of part 2) when the load resistor $R_L$ =100Ω and when $R_L$ =8Ω.
- 4) Choose a transistor with suitable power rating




# Example Continued

- **SOLUTION**




$$1)\ R_3 \le \frac{V_{IN(Min)} - V_Z}{I_{Z(Min)}}$$

$$R_3 \le \frac{20 - 4}{2\ \text{mA}} = 8\ \text{k}\Omega \text{ in order to make sure } I_Z > I_{Z(Min)}$$

If $I_{Z(max)}$ was known , then lower limit for R3 can also be found

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z = 12\ \text{V}$$

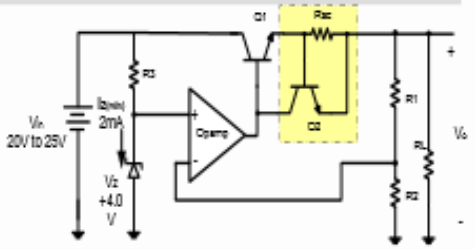
$$\therefore \frac{R1}{R2} = \frac{V_o}{V_Z} - 1 = \frac{12}{4} - 1 = 2$$

$$\Rightarrow \quad \text{choose } R_1 = 20\ \text{k}\Omega$$

$$\therefore R_2 = 10\ \text{k}\Omega$$

# Voltage Regulators

- **SOLUTION**

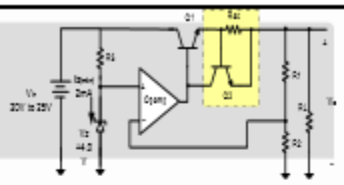



2) — The change for current limit is done by adding Q2 and Rsc as shown

$$\& \quad R_{SC} = \frac{V_{be}}{I_{L(Max)}} = \frac{0.7\ V}{1A} = 0.7\Omega$$

# Ex. Continued

- **SOLUTION**



For $R_L = 100$ ohm, $Vo = 12V$, then $I_L = \frac{12V}{100\Omega} = 0.12A$

which is smaller than $I_{L(max)}$,

$\therefore V_o = 12$ V and is not affected by the current limit circuit

For $R_L = 8$ ohm, $Vo = 12V$, then $I_L = \frac{12V}{8\,\Omega} = 1.5A$

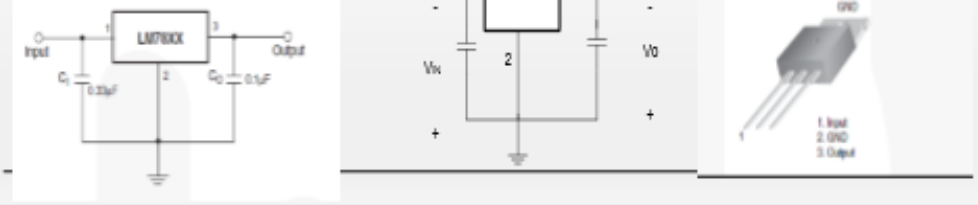
which is bigger than $I_{L(max)}$, and the current limit circuit limits the current to the maximum allowable value which is 1 A

$\therefore V_o = I_{L(Max)} * R_L = 1A * 8\Omega = 8$ V

# 3 Terminal IC Voltage Regulators

- Fixed output voltage type
- Two families exist:
- Fixed positive output (78xx ) , where xx defines the value of output voltage such as 5, 6, 8,9,12 …etc
- Fixed negative output (79xx ) , where xx defines the value of output voltage such as -5, -6, -8,-9,-12 …etc

**LM78XX / LM78XXA**
**3-Terminal 1 A Positive Voltage Regulator**




## Fixed Voltage Regulator

**Positive-Voltage** Regulators in the 78XX Series

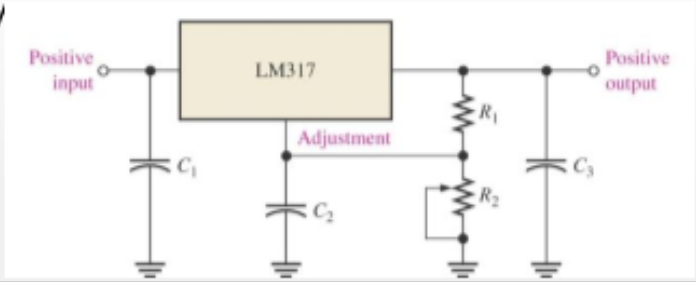
| IC Part | Output Voltage (V) | Minimum $V_i$ (V) |
|---|---|---|
| 7805 | +5 | +7.3 |
| 7806 | +6 | +8.3 |
| 7808 | +8 | +10.5 |
| 7810 | +10 | +12.5 |
| 7812 | +12 | +14.5 |
| 7815 | +15 | +17.7 |
| 7818 | +18 | +21.0 |
| 7824 | +24 | +27.1 |

**Vin must be higher than Vo by at least 2V for proper operation of the voltage regulator**

# Adjustable-Voltage Regulator

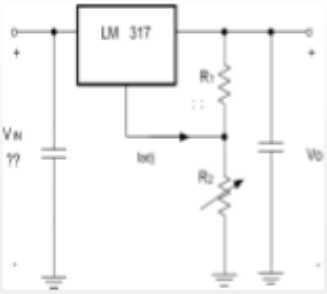
## Adjustable-Voltage Regulator

- Voltage regulators are also available in circuit configurations that allow to set the output voltage to a desired regulated value.
- The LM317 is an example of an adjustable-voltage regulator, can be operated over the range of voltage from 1.25 to 35 V



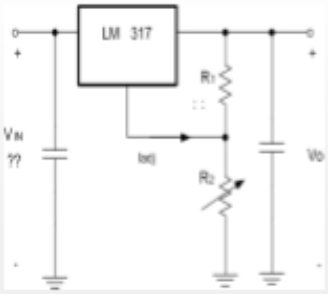

# Voltage Regulators

- Iadj=~ 50 uA (constant From data sheet)
- $V_{REF}$=1.25 (always true for the 317 family)
- Vo=~ 1.25 – 35V
- Vo is defined by proper choice of R1 & R2
- $Vo=V_{R1}+V_{R2}$
- $V_{R1}=V_{REF}=I_{R1}*R1$
- $I_{R1}=I_{REF}=V_{REF}/R1$
- $V_{R2}=(I_{REF}+I_{ADJ})*R2$
- $Vo=I_{REF}*(R1+R2)+Iadj*R2$



## Example

- Given R1=220 Ω ; R2=5kΩ potentiometer
- Iadj=~ 50 uA (constant From data sheet)
- Find Vo(min) and Vo(max)
- Find range of Vin ?




## Voltage Regulators

$$I_{REF} = \frac{V_{REF}}{R_1} = \frac{1.25}{220\,\Omega}$$

$$V_O = I_{REF}(R_1 + R_2) + I_{adj}(R_2)$$

$$V_{O(MAX)\,|R2=5k\Omega} = (26.66 + 0.25) = 29.91\,V$$

$$V_{O(MIN)\,|R2=0k\Omega} = V_{REF} = 1.25\,V$$

The input voltage must be higher than the output by at least 2 V

$$V_{IN(MIN)} \cong 1.25 + 2 = 3.25\,V$$

$$V_{IN(MAX)} \cong 29.91 + 2 = 31.91\,V$$