**Prelab for Experiment 4 ENEE2103**

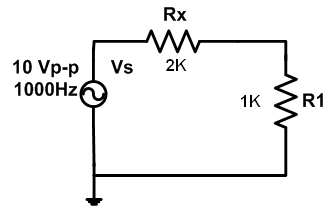
**Sinusoidal Steady State Circuit Analysis**

***Note: Transient analysis is required in all circuits***

# Impedance:

# Connect the circuit of Fig (4.1) in Pspice

1. Measure the total impedance of the circuit by measuring the total voltage and current. Find the phase shift between total voltage and current using probe.
2. Repeat the step (2) with the signal frequencies: 500 Hz , 1500 Hz
3. Connect the circuit of Fig (4.2)in Pspice and repeat step (2)
4. Repeat the steps (2) with the signal frequencies: 500Hz , 1500 Hz
5. Connect the circuit of Fig (4.3)In Pspice and repeat step (2)
6. Repeat step (2) with the signal frequencies: 500Hz , 1500 Hz

  
Fig (4.1)

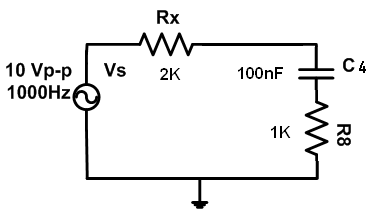


Fig (4.2)

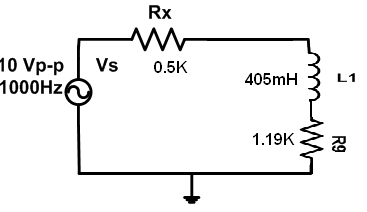


Fig (4.3)

# Capacitive and inductive behvior:

1. Connect the circuit in Fig (4.4) in Pspice
2. Measure the phase shift between the total current and the source voltage.
3. Calculate the resonance frequency (fo) and adjust the source to this frequency and repeat step (2)
4. Change source frequency to 2fo and repeat step 2.
5. Based on the results obtained in previous steps, observe the circuit behavior whether it is capacitive, inductive and resistive in each case.
6. Set the generator frequency to the resonance frequency found in 4.
7. Double the value of the capacitor (i.e. connect an additional 100nF in parallel with old one).
8. Explain the behavior of the circuit according to the circuit response and phase shift.
9. Disconnect the new capacitor.
10. Double the value of the inductor by adjusting the inductance decade box setting.
11. Explain the behavior of the circuit according to the circuit response and phase shift

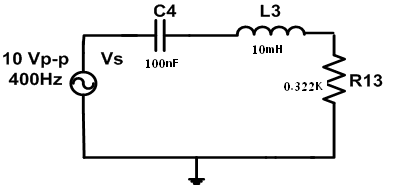


Fig (4.4)

# Sinosoidal steady state power:

1. Connect the circuit in Fig (4.5) in Pspice
2. Plot the voltage and current across R6
3. Plot Vs and Is and measure phase shift
4. Plot Vc and Ic and measure phase shift
5. Plot VL and IL and measure phase shift
6. Plot voltage across R1 and Is and measure phase shift

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Vs** | **Is** | **V(R1)** | **(ӨVs- ӨIs)** | **Vc** | **Ic** | **(ӨVc- ӨIc)** |
|  |  |  |  |  |  |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **VL** | **IL** |  | **(ӨVL- ӨIL)** | **VR6** | **IR6** | **(ӨR6- ӨIR6)** |
|  |  |  |  |  |  |  |

Table (1-5)



Fig (4.5)