**Experiment #8 - Prelab ENEE2103**

**The Field-Effect Transistor**

**Pre-lab Work:**

You have to apply PSPICE simulation to all practical circuits shown in the procedure below

**Procedure:**

***I. CHARACTERESTICS OF AN N-CHANNEL JFET.***

1. Simulate the circuit of Figure 8.1 using the pspice Figure shown below. ( note that you do not need to connect an ammeter as shown)
2. **Use parametric analysis for the 100k potentiometer (use appropriate steps in the parametric analysis to get multiple well-placed curves). Combined with DC sweep for the voltage source (V2) connected to the drain (from 0 to 20 V linearly)**
3. **Plot Id=f(Vds)**

Students need to get drawing one curve of ID against VDS for each value of VGS

|  |  |
| --- | --- |
|  | **ID( mA) for VDS=(V)** |
| **VGS(V)** | **0** | **0.5** | **1** | **2** | **5** | **10** | **15** |
| **0** |  |  |  |  |  |  |  |
| **-0.5** |  |  |  |  |  |  |  |
| **-1.0** |  |  |  |  |  |  |  |
| **-1.5** |  |  |  |  |  |  |  |
| **-2.0** |  |  |  |  |  |  |  |
| **-2.5** |  |  |  |  |  |  |  |

This table is not to be filled for the prelab, but to be used to get approximate values of Vgs for parametric sweep of the 100k potentiometer





Notes: When setting parametric sweep type try both linear or value list to get reasonable curves for different values of Vgs set by the potentiometer

 ***Questions:***

* From your graph, above which values of VDS is ID almost unaffected by VDS when VGS=0?
* For a given value of VDS , (say 10 V ),do equal changes of VGS cause equal changes of ID?
* Can you measure IG or is it too small?

***II. COMMON DRAIN AMPLIFIER.***

1. Connect the circuit as shown in fig. (8-3) in pspice, use J2N3819.



1. Perform bias point analysis and measure DC voltages of VG, and VS.
2. Now apply an input of 0.4 volts peak-to-peak from the generator, 1 kHz and observe the output.
3. Calculate the voltage gain and the phase shift between the input and output voltage.
4. Measure the values of Zin and Zout using the appropriate voltages and currents at the places shown in the previous figure.

***III. CONSTANT CURRENT SOURCE.***

* + Connect the circuit as shown in fig.(8-4). Use J2N4393



* + Perform DC sweep for value of RL within specified range
	+ Display VL across the resistor and IDS

|  |  |  |
| --- | --- | --- |
| **RL(KΩ)** | **VL(V)** | **ID(mA)** |
| **0.1** |  |  |
| **0.22** |  |  |
| **0.33** |  |  |
| **0.47** |  |  |
| **0.56** |  |  |
| **1** |  |  |
| **1.5** |  |  |
| **2** |  |  |
| **3** |  |  |

Table 8.2