L10: Introduction to FET's

Analog Electronics
ENEE236

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FET Vs conventional Transistors (BJT)

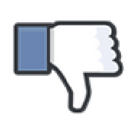
Advantages

1- High input impedance ; ~100 M !

2- Fewer steps in manufacturing process.

3- More devices can be packaged into smaller area for integrated circuit **IC**

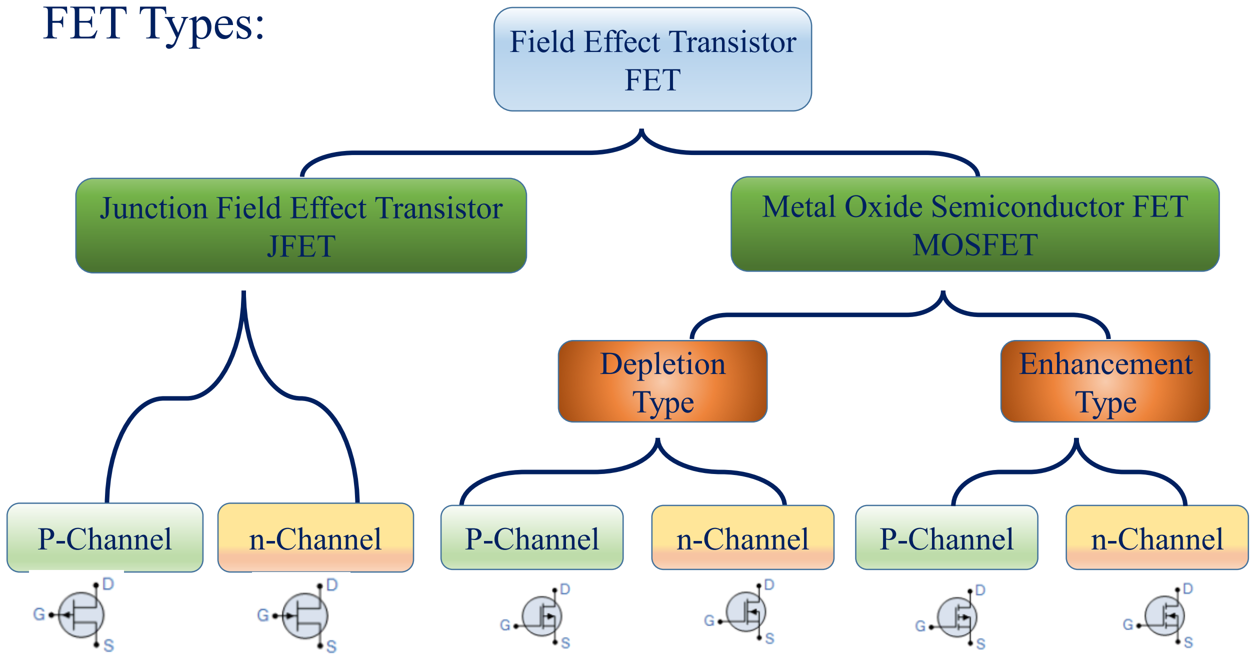
Disadvantages



1- Low values of voltage gain.

2- Poor high frequency performance.

FET Types:

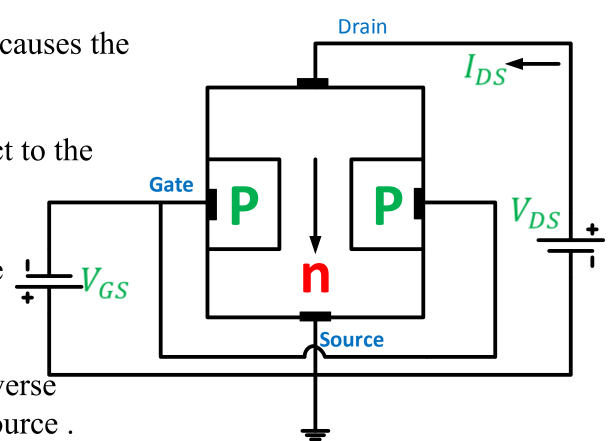


Junction Field Effect Transistor JFET

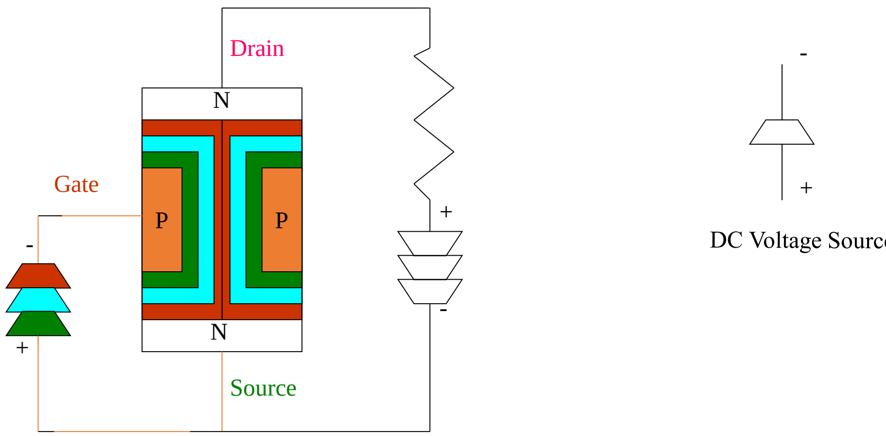
JFET construction:

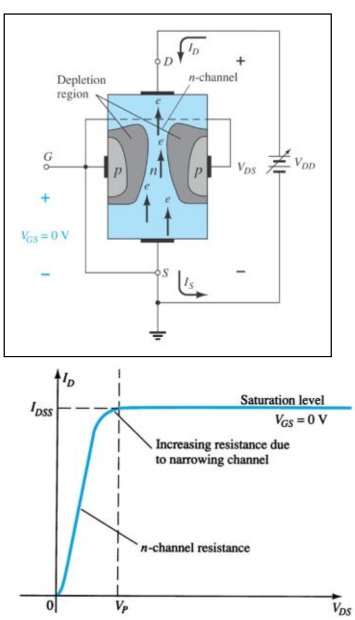
- ✓ Reverse biasing the gate to source junctions causes the formation of the depletion region
- ✓ The drain has the proper polarity with respect to the source to establish the drain current I_{DS}
- ✓ The value of I_{DS} depends on the width of the channel.
- ✓ The width of the channel is controlled by reverse biasing the pn-junctions between gate and source .
- ✓ If the channel width increases I_{DS} increases .

n-channel JFET



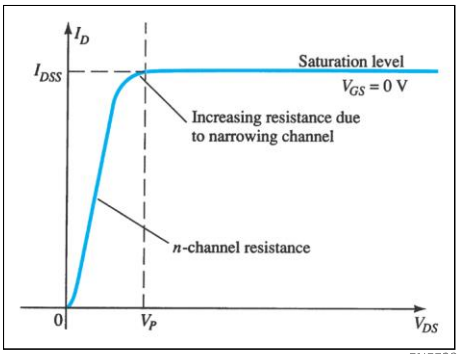
Operation of a JFET

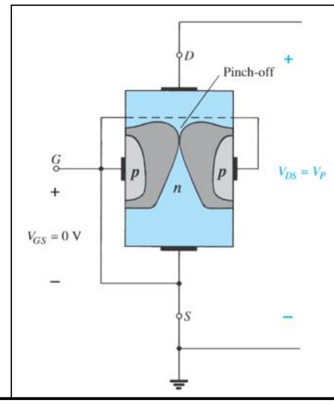




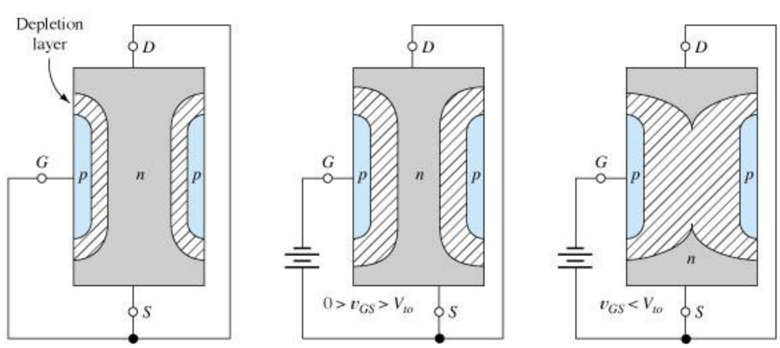
-When VDD is applied , electrons are drawn to the drain terminal establishing drain current ID
-Drain and source currents are equivalent (ID=Is)
-ID is limited by the resistance of the n-channel between the drain and source
-IG=0 (due to the fact that the pn junction id reverse biased)
-As VDS is increased , ID will also increase according to ohms law

- As V_{DS} is increased towards a value V_P (pinch off voltage) , the depletion region is widened and channel width is reduced increasing resistance to I_D and the two depletion regions will appear as touching each other
- These two effects result in I_D being kept almost constant





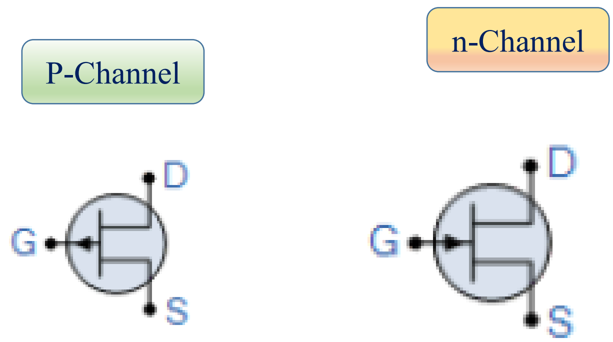
N-Channel JFET Operation



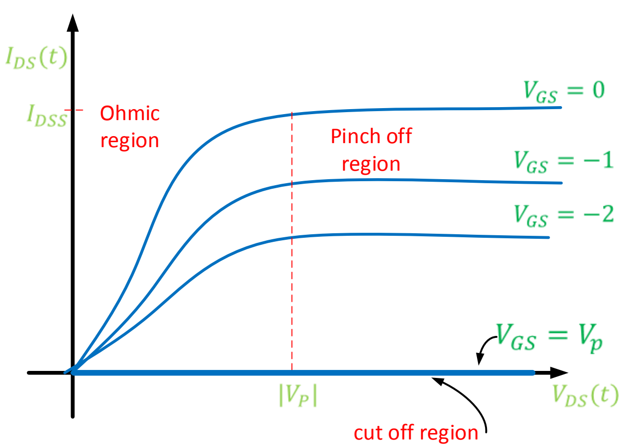
(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source
(b) Moderate gate-to-channel reverse bias results in narrower channel
(c) Bias greater than pinch-off voltage; no conductive path from drain to source

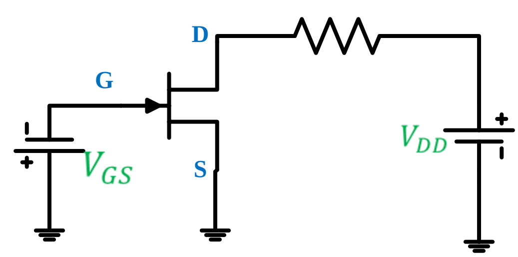
The nonconductive depletion region becomes thicker with increased reverse bias.
(*Note:* The two gate regions of each FET are connected to each other.)

JFET Circuit Symbol:



JFET output characteristic:



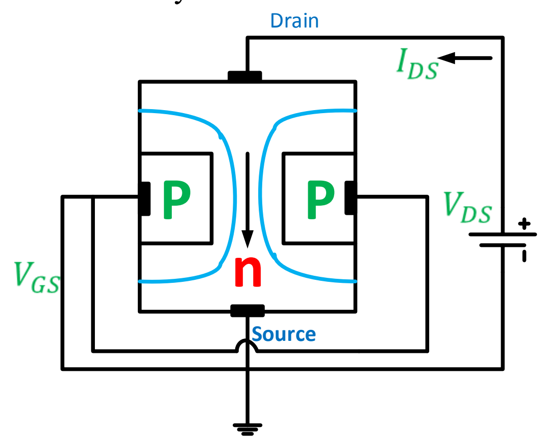


Pinch of voltage V_P:

For $V_{GS} = 0$,the value of V_{DS} at which I_{DS} becomes essentially constant
Is the absolute of the pinch of voltage
$V_{DS} = |V_P|$

Some literature refer to Vp as $V_{GS(off)}$

$$V_P = \begin{cases} negative\ value\ for\ n\_channel \\ positive\ value\ for\ p\_channel \end{cases}$$



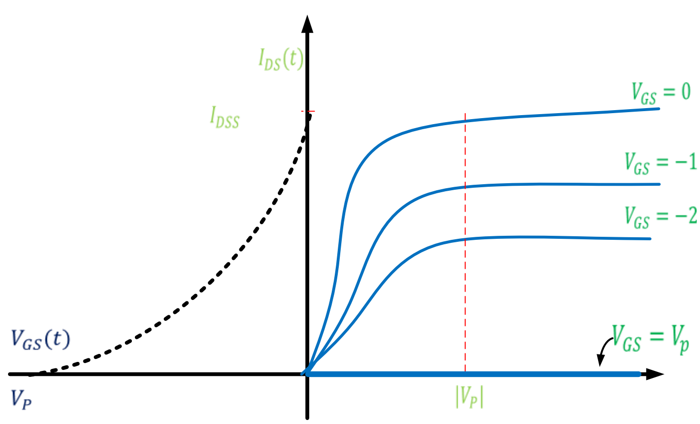
JFET Transfer characteristic curve:

$$I_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

In pinch off region:

$$V_P < V_{GS} \leq 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$



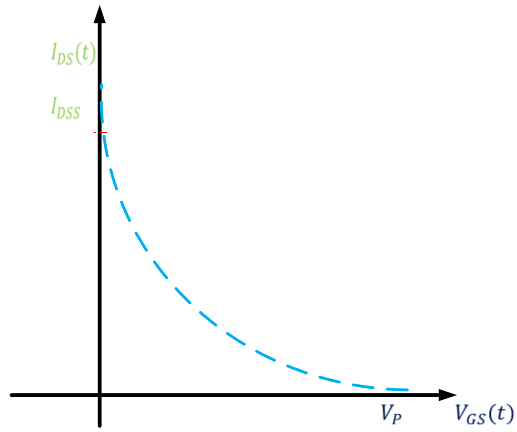
P-channel JFET

$$I_{DS}(\mathrm{t}) = I_{DSS}\left(1 - \frac{V_{GS}(t)}{V_P}\right)^2$$

In pinch off region:

$$|V_{DS}| > |V_P| - |V_{GS}|$$

$$V_P > V_{GS} \geq 0$$



Pinch off voltage:

- ✓ The voltage that cusses the depletion region to touch and close the channel is called pinch off voltage
- ✓ For the n-channel JFET to be in the pinch off region:

  $$V_P < V_{GS} \leq 0$$

  $$|V_{DS}| > |V_P| - |V_{GS}|$$
- ✓ For the p-channel JFET to be in the pinch off region:

  $$|V_{DS}| > |V_P| - |V_{GS}|$$

  $$V_P > V_{GS} \geq 0$$

Common JFET Biasing Circuits

- Fixed-Bias
- Self-Bias
- Voltage-Divider Bias

Basic Current Relationships

For all FETs:

$I_G \cong 0\text{ A}$

$I_D = I_S = I_{DS}$

For JFETS

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

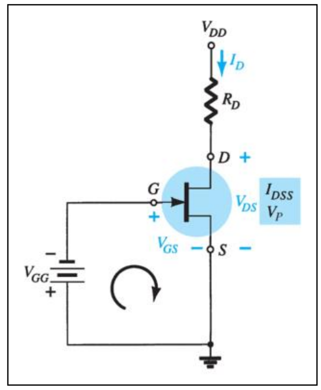
Fixed-Bias Configuration

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0\text{ V}$$

$$\therefore V_D = V_{DS}$$

$$\therefore V_{GS} = -V_{GG}$$



Example

$$V_{GS} = V_G - V_S = -1.5 - 0 = -1.5\text{ V}$$

Assuming JFET is in pinch off region

$$1)\ I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10\text{ mA}\left(1 - \frac{-1.5}{-4}\right)^2$$

$$= 3.9\text{ mA}$$

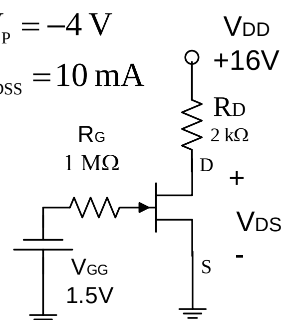
$$2)\ V_{DS} = V_{DD} - I_D R_D$$

$$= 16 - ((2\text{k})(3.9\text{ mA}))$$

$$= 8.2\text{ V}$$

$$V_P = -4\text{ V}$$

$$I_{DSS} = 10\text{ mA}$$



3)check for $|V_{DS}| > |V_P| - |V_{GS}|$?

$$|8.2| > |-4| - |-1.5|$$

assumption is true

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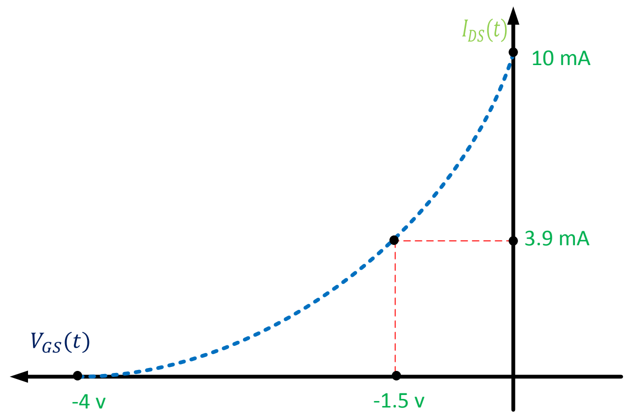
Graphical method:

- $I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$
- V_{GS}= **-1.5 v Fixed**



Self-Bias Configuration

$$V_{GS} = V_G - V_S = 0 - V_S = -V_S$$

$$V_S = I_D R_S$$

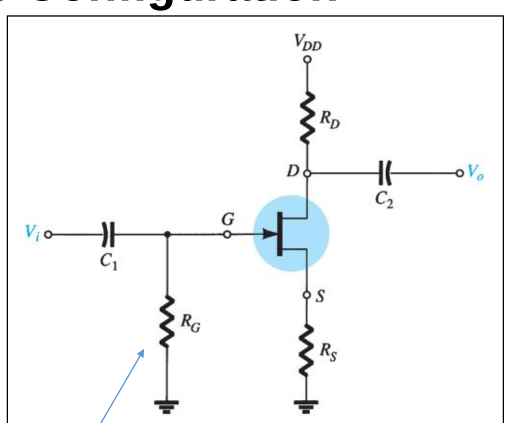
$$V_{GS} = -I_D R_S$$

$$V_D = V_{DD} - I_D R_D$$

$$V_{DS} = V_D - V_S$$

$$= V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_S + R_D)$$

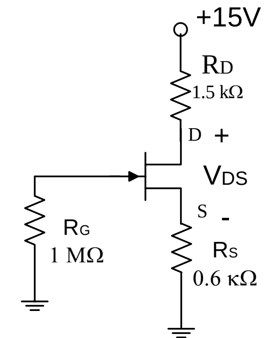


RG is important to isolate the bac signal from ground in amplifier circuits

Example

$V_P = -4\ \text{V}$

$I_{DSS} = 10\ \text{mA}$



$$V_{GS} = V_G - V_S = 0 - V_S = -V_S$$

$$V_S = I_D R_S = 600\ \text{I}_D$$

$$V_{GS} = -600 I_D$$

$$1)\ \ I_D = 10\ \text{mA}\left(1 - \frac{-600 I_D}{-4}\right)^2$$

$$ax^2 + bx + c = 0$$

$$x_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

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Example-continued

solving for I_D :

$I_{D1} = 14.77\ \text{mA} > \text{I}_{DSS}$ and this solution is not possible

$I_{D2} = 3\ \text{mA} \Leftarrow$ this is the correct solution

$$2)\ \therefore \text{V}_{GS} = -600\text{I}_D = -600\ \text{x}\ 3\text{mA} = -1.8\text{V}$$

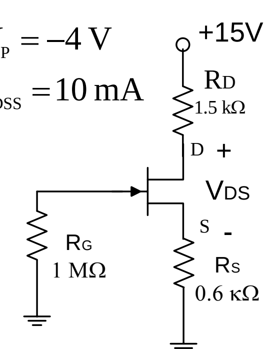
$$V_D = V_{DD} - I_D R_D$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$= 15 - 3\text{mA}\ (1\text{k} + 0.6\text{k}) = 10.2\ \text{V}$$

$V_P = -4\ \text{V}$

$I_{DSS} = 10\ \text{mA}$



3)check for $|\text{V}_{DS}| > |\text{V}_P| - |\text{V}_{GS}|$?

$$|10.2| > |-4| - |-1.8|$$

➡ assumption is true

Graphical method

- $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- V_{GS}= -(0.6K) I_{DS}

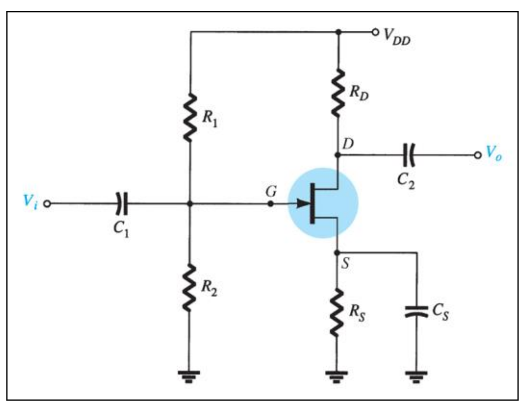
when V_{GS}=0 $\rightarrow$ I_{DS}= 0mA

when V_{GS}= -3v $\rightarrow$ I_{DS}= 5mA

Voltage-Divider Bias

I_G = 0 A

I_D responds to changes in V_{GS}.



Voltage-Divider Bias Calculations

$I_G = 0$ A

V_G is equal to the voltage across divider resistor R_2:

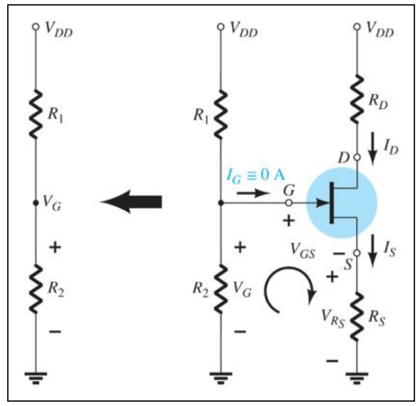
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_S = I_D R_S$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - I_D R_S$$



The Q-point is established by plotting a line that intersects the transfer curve.

Example

V_S must be more positive than V_G

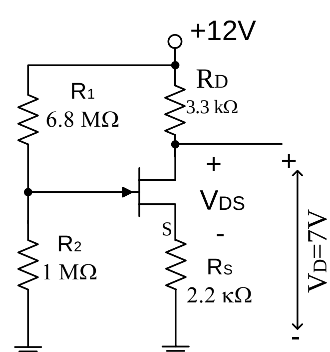
to keep the gate – source junction reverse biased

$$V_S = I_D R_S$$

$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = \frac{R_2 V_{DD}}{R_1 + R_2} - I_D R_S$$



$$V_D = V_{DD} - I_D R_D = 7\text{ V}$$

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12-7}{3300} = 1.52\text{ mA}$$

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Example

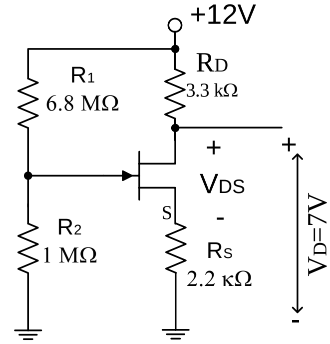
$$V_S = I_D R_S = (1.52\text{mA})\ (2.2\text{k}\Omega) = 3.34\text{ V}$$

$$V_G = \frac{1\text{ M}}{1\text{ M} + 6\text{ M}} 15 = 1.54\text{ V}$$

$$V_{GS} = 1.54 - 3.34 = -1.8\text{ V} < 0 \quad \Leftarrow \text{OK}$$

also

$$\text{I}_\text{D} = \frac{\text{V}_\text{S}}{\text{R}_\text{S}} = \frac{3.34}{2200} = 1.52\ \text{ mA}$$



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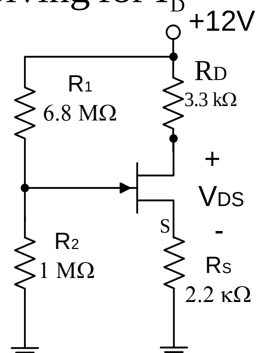
Example-V_D unknown

For the same example, if V_D was not given, then we use the square law rule $\text{I}_\text{D} = \text{f}(\text{V}_{\text{GS}})$ to find I_D and V_{GS} by substituting the expression for $\text{V}_{\text{GS}} = \frac{\text{R}_2 \text{V}_{\text{DD}}}{\text{R}_1 + \text{R}_2} - \text{I}_\text{D}\text{R}$ in it and solving for I_D

$$V_{GS} = 1.54 - I_D R_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{1.54 - I_D R_S}{V_P}\right)^2$$



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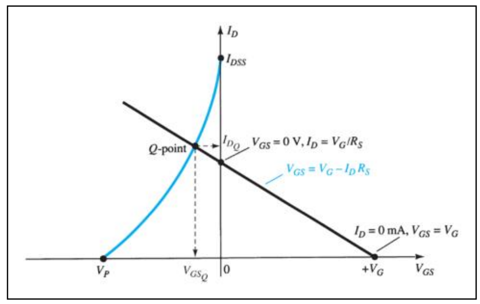
Voltage-Divider Q-Point

Plot the line that is defined by these two points:

$V_{GS} = V_G$, $I_D = 0$ A

$V_{GS} = 0$ V, $I_D = V_G / R_S$

Plot the transfer curve by plotting I_{DSS}, V_P and the calculated values of I_D



The Q-point is located where the line intersects the transfer curve

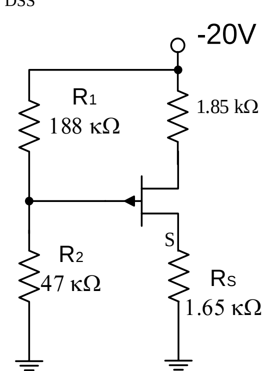
Example p-channel

$V_P = 5\,V$

$I_{DSS} = 18\,mA$

$$V_{GS} = \frac{R_2\ x - 20}{R_1 + R_2} + I_D R$$

$$V_{GS} = -4 + I_D R_S$$



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-4 + I_D R_S}{V_P}\right)^2$$

$$I_D = 18\text{ mA}\left(1 - \frac{-4 + 1650 I_D}{5}\right)^2$$

- Solving the quadratic equation and finding its roots yields:

$I_{D1} = 4.7\text{ mA}$

$I_{D2} = 7.4\text{ mA}$

both values of $I_D < I_{DSS}$ and are possible solutions

so we verify value of V_{GS} :

$V_{GS1} = -4 + (4.7\text{mA})(1.65\text{ k}\Omega) = 3.75\text{ V} < V_p \angle$ correct solution

$V_{GS2} = -4 + (7.4\text{mA})(1.65\text{ k}\Omega) = 8.21\text{ V} > V_p \times$ wrong solution

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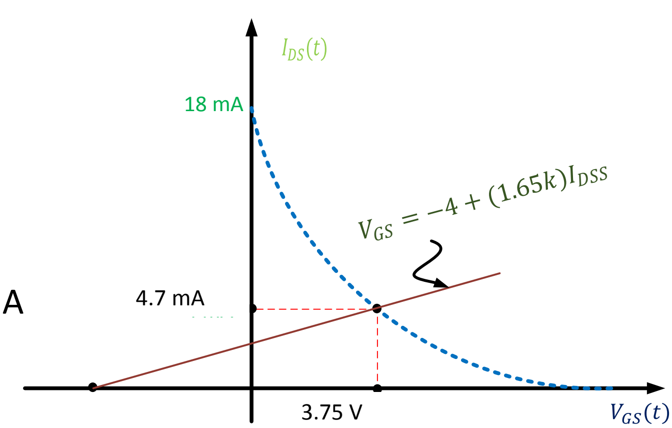
Graphical method

- $I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- V_{GS} = -4 + (0.6K) I_{DS}

when V_{GS} = -4v → I_{DS} = 0mA

when V_{GS} = 0v → I_{DS} = 2.42 mA



Midpoint Bias
For maximum Symmetrical Swing

- Place Q-point in the middle point of the transfer characteristic to allow for maximum swing between I_{DSS} and zero

$$1)\ let\ I_D = 0.5 I_{DSS}$$

$$0.5 I_{DSS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$0.5 = \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\sqrt{\frac{1}{2}} = 1 - \frac{V_{GS}}{V_P}$$

$$\frac{V_{GS}}{V_P} = 1 - \sqrt{\frac{1}{2}}$$

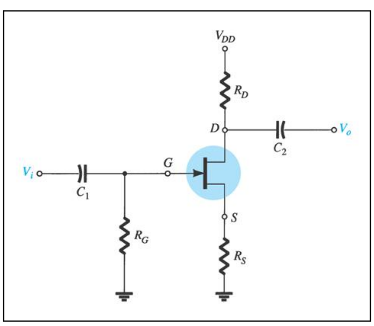
$$V_{GS} = V_P(1 - 0.707)$$

$$= V_P(0.2928)$$

$$\therefore V_{GS} \cong \frac{V_P}{3.41}$$

$$2)\ let\ V_D = 0.5 V_{DD}$$

Example



$$V_P = Vgs(off) = -3\text{ V}$$

$$I_{DSS} = 12\text{ mA}$$

Choose R_D and Rs for mid point bias

$$I_D = 0.5 I_{DSS} = 6\text{ mA}$$

$$V_D = 0.5 V_{DD} = 6\text{ V}$$

$$V_{GS} = \frac{V_{GS(off)}}{3.4} = \frac{-3}{3.4} = -0.882\text{ V}$$

$$Rs = \frac{Vs}{Rs} = \frac{0.882}{6\text{ mA}} = 147\Omega$$

$$V_{DD} - I_D R_D - V_D = 0$$

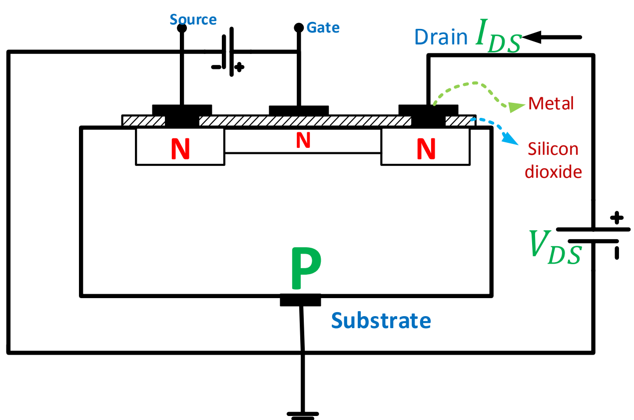
$$R_D = \frac{V_{DD} - V_D}{I_D} = 1\text{k}\Omega$$

Metal Oxide Semiconductor Field Effect Transistor MOSFET

- 1) Depletion type MOSFET: DMOSFET
- 2) Enhancement type MOSFET: EMOSFET
- The MOSFET differs from the JFET in that it has no pn junction structure; instead, the gate of the MOSFET in insulated from the channel by a silicon dioxide (S_iO_2) large.
- Due to this the input resistance of MOSFET is greater than JFET.

Depletion type MOSFET:

- Construction of n-channel DMOSFET:



Operation , characteristic and parameters of DMOSFET

♦ **n-channel DMOSFET**

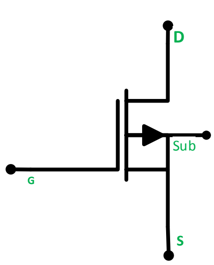
- On the application of $V_{DS}$and keeping V_{GS}=0 electrons from the n-channel are attracted towards positive potential of the drain terminal .

- This establishes current through the channel to be denotes as I_{DSS} at V_{GS}=0 .

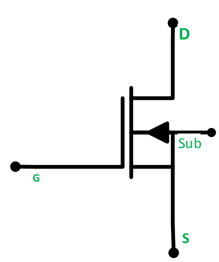
- If we apply negative gate voltage ($V_{GS}< 0$) the negative charge on the gate repel electrons from the channel . The number of repelled electrons depends on the magnitude of the negative voltage V_{GS}.

- The grater the negative voltage applied at the gate , the level of drain current will reduces until it reaches zero ; $V_{GS}= V_P$.

- For positive value of V_{GS}, the positive gate will draw additional electrons from the p-type substrate and the drain current increases .

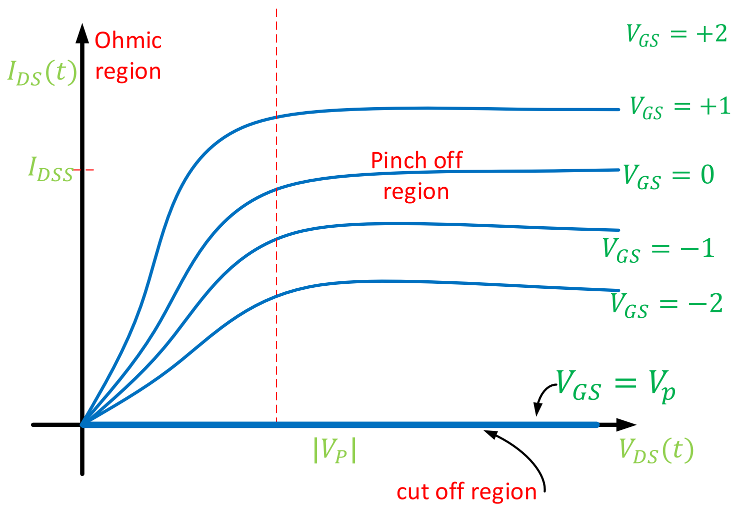


P-channel
DMOSFET

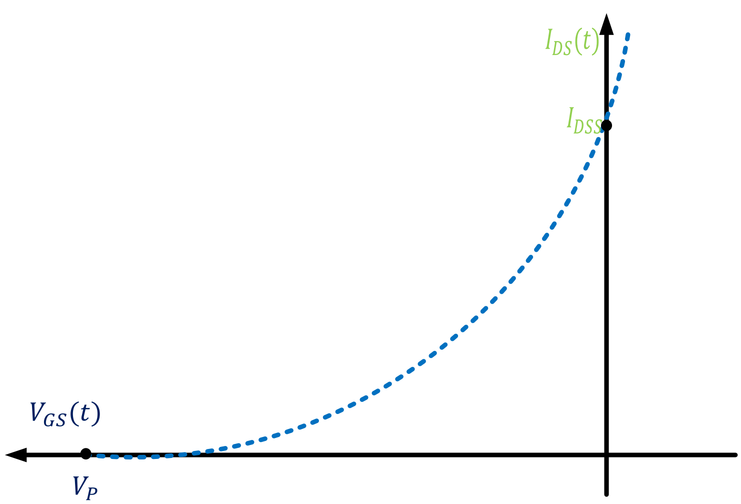


n-channel
DMOSFET

Drain characteristics for an n-channel DMOSFET

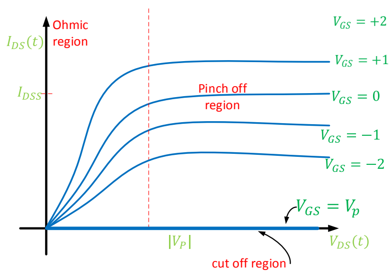


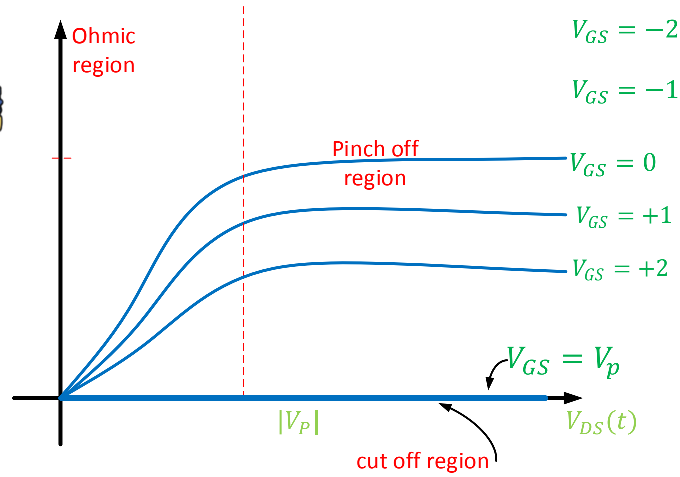
Transfer characteristics for an n-channel DMOSFET



Drain characteristics for an p-channel DMOSFET

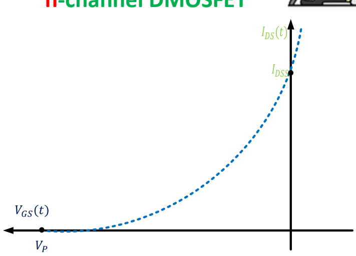
n-channel DMOSFET

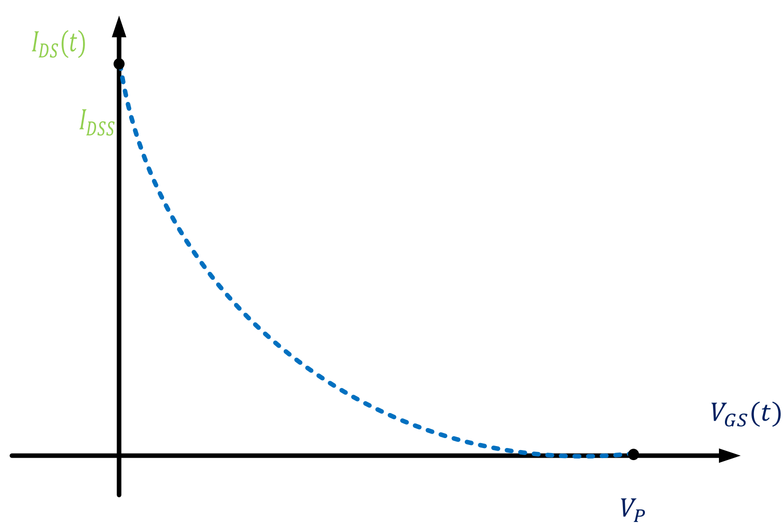




Transfer characteristics for an p-channel DMOSFET

n-channel DMOSFET





In the pinch off region

$$i_{DS}(t) = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

♦ For the n- channel

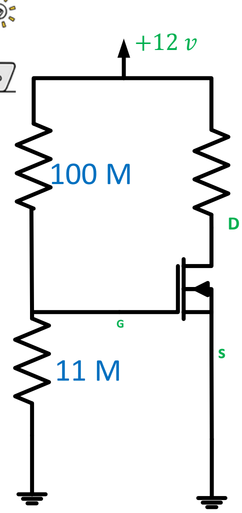
$V_{GS} > V_P$ (negative)
$V_{DS} > V_{GS} - V_P$

♦ For the p- channel

$V_{GS} < V_P$ (positive)
$V_{DS} < V_{GS} - V_P$

Example

Suppose that the DMOSFET is in the pinch off region



$I_{DSS} = 4mA$

$V_P = -5\ v$

I_{DSS}= 4mA V_P= - 5 v

$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ ………….1

$V_{GS} = V_G - V_S = V_G$

$V_G = \frac{11M}{11M+100M}(12) = 1.19$ v ………….2

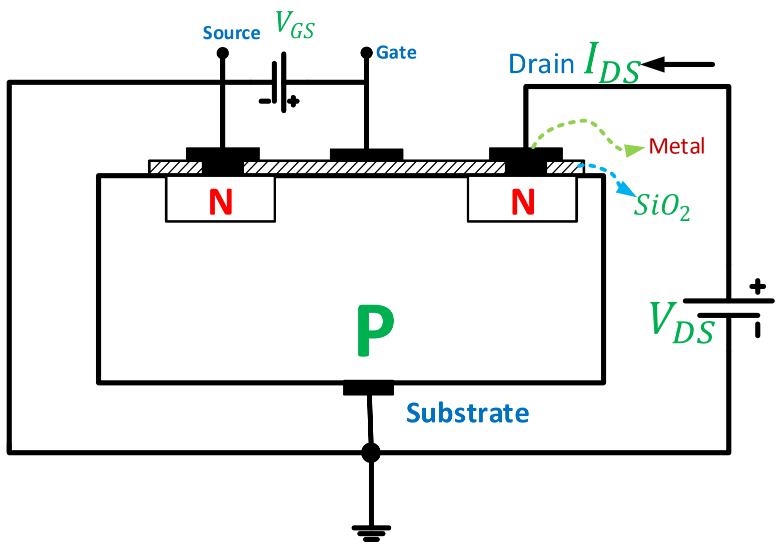
sub 2 into 1 , we obtain

I_{DS}= 6.13mA > I_{DSS} !! THIS IS POSSIBLE AND DMOSFET WILL OPERATE IN ENHANCEMENT MODE

$V_{DS} = V_{DD} - 0.5K\ I_{DS}$ = 8.93 v
$V_{DS} >^{?} V_{GS} - V_P$ = 6.19 v

Enhancement Type MOSFET

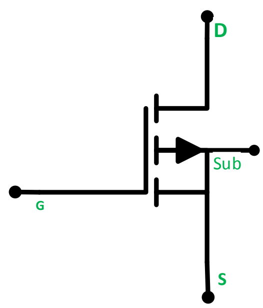
- Construction of n-channel EMOSFET:



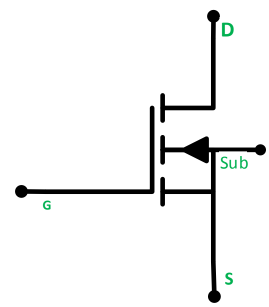
Operation , characteristic and parameters of EMOSFET

- On the application of $V_{DS}$and keeping V_{GS}=0 practically zero current flows .
- If we increase V_{GS} in the positive direction the concentration of electrons near the SiO_2 surface increases ,
- At particular value of V_{GS} there is a measurable current flow between drain and source ; I_{DS} .
- This value of V_{GS} is called threshold voltage denoted by V_T or $V_{GS(TH)}$
- A positive V_{GS} above V_T induce a channel and hence the drain current (I_{DS}) by creating a thin layer of negative charges (electrons) in the substrait adjacent to the SiO_2 large .

The conductivity of the channel is enhanced by increasing V_{GS} and thus pulling more electrons into the channel .

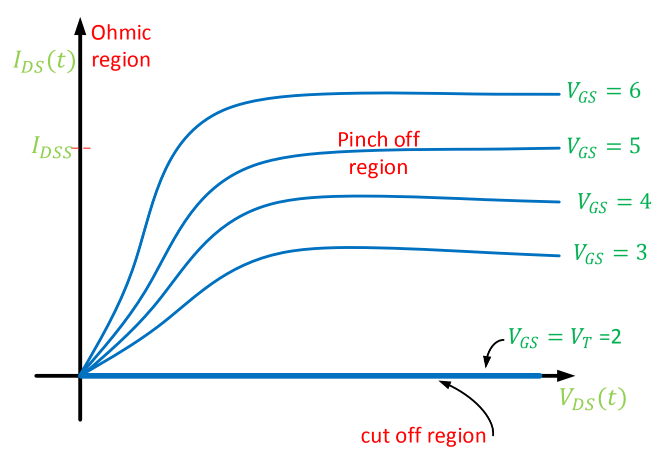


P-channel EMOSFET

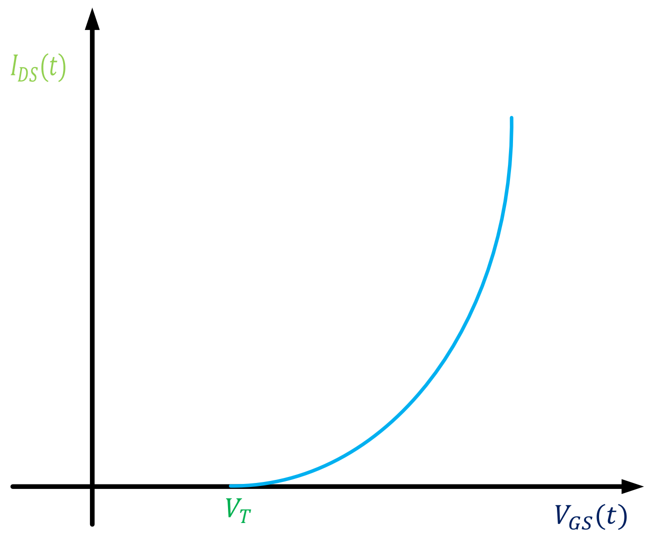


n-channel EMOSFET

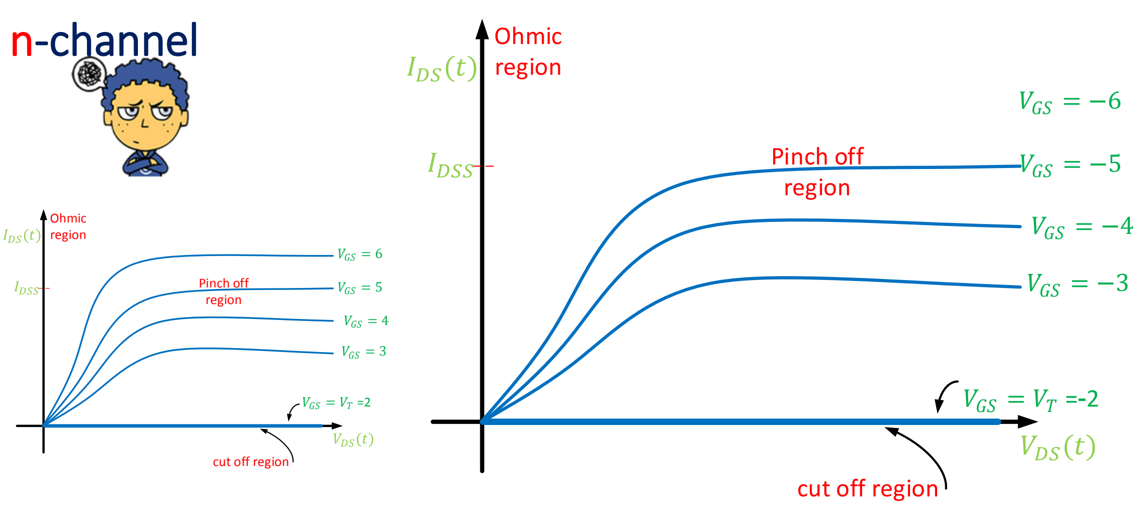
Drain characteristics for an n-channel EMOSFET



Transfer characteristics for an n-channel EMOSFET

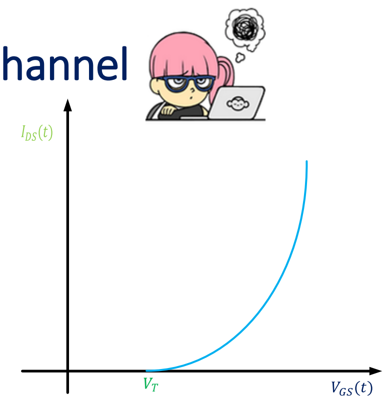


Drain characteristics for an p-channel EMOSFET

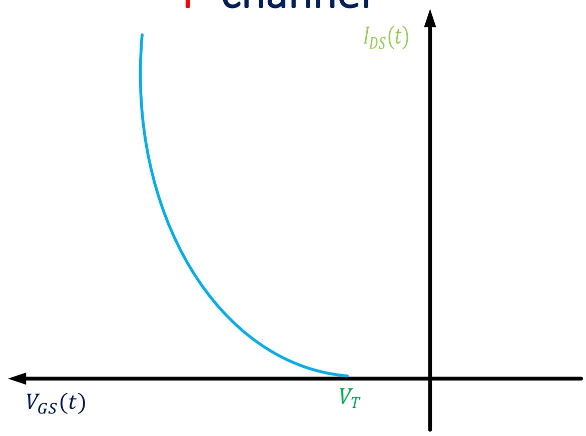


Transfer characteristics for an p-channel EMOSFET

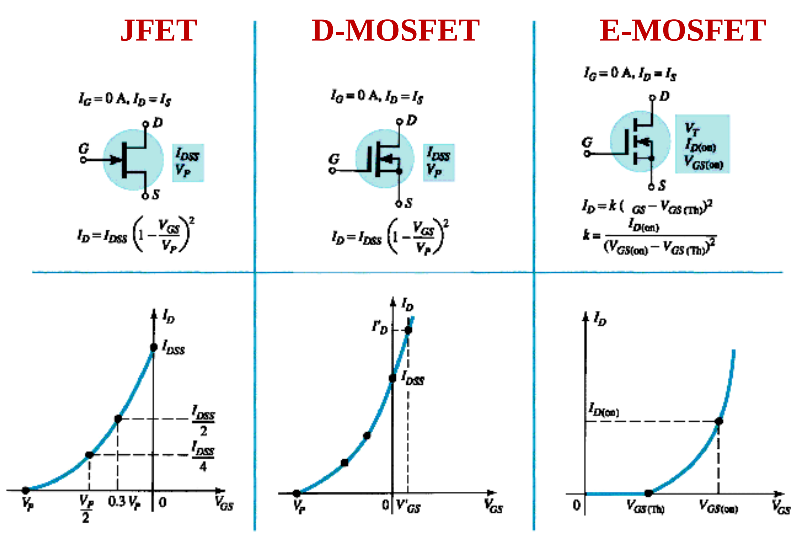
n-channel



P-channel



Summary Table



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In the pinch off region

$i_{DS}(t) = K_n(V_{GS}(t) - V_T)^2$

$|V_{DS}| > |V_{GS} - V_T|$

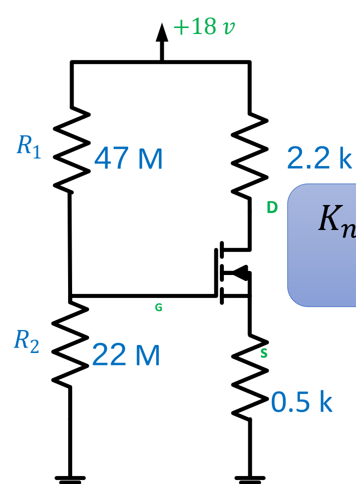
$V_{GS} > V_T$; n- channel
$V_{GS} < V_T$; p- channel

Example

$I_{DS} = K_n(V_{GS} - V_T)^2$ 1

$V_{GS} = V_G - V_S$

$V_G = \frac{22M}{22M+47M}(18) = 5.74\text{v}$



$K_n = 0.25\text{X}10^{-3} A/V^2$
$V_T = 2$ v

V_S= (0.5K) I_{DS}

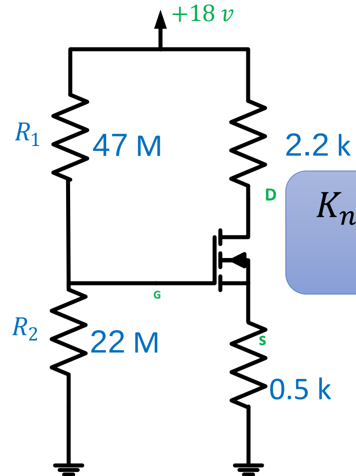
V_{GS} = 5.74 - (0.5K) I_{DS}............2

solving for $\boldsymbol{V_{GS}}$:

V_{GS}= 4.78v √
= -8.78v X

I_{DS}=1.92m A

V_{DS}= 12.82> | $V_{GS} - V_T$ |



K_n=0.25X10^{-3}A/V^2
V_T = 2 v