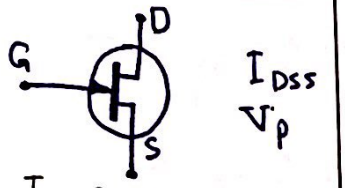
Electronisc : ENEE 236 ⇨ L16 FET ac Analysis

Summary table

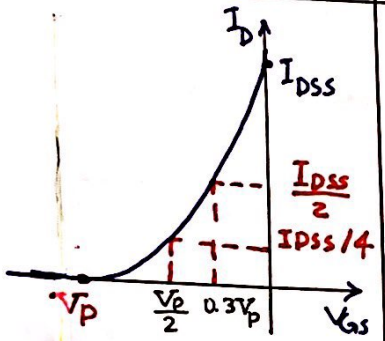
JFET



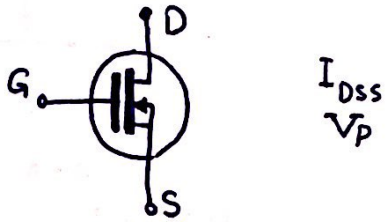
I_{DSS}
V_P

$I_G = 0$, $I_D = I_S$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

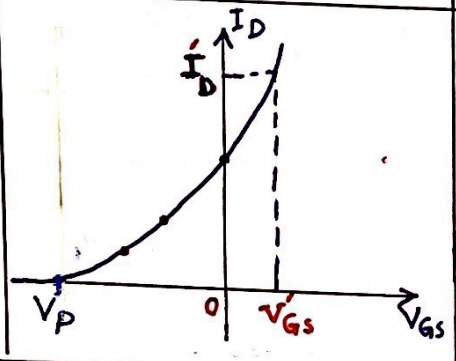


D-MOSFET

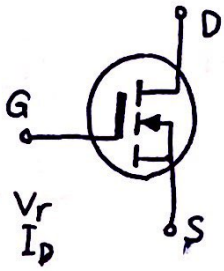


I_{DSS}
V_P

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$



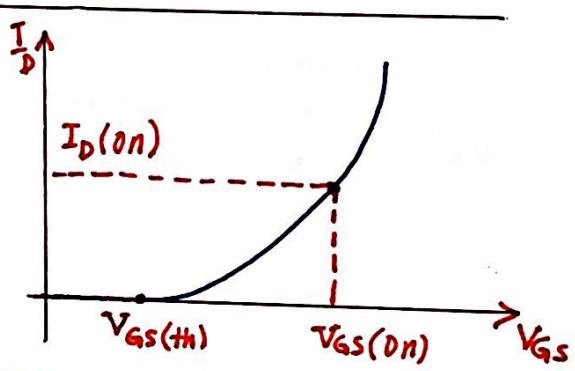
E-MOSFET



$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2$

$K = \frac{I_D}{\left(V_{GS} - V_{GS(Th)}\right)^2}$

V_r
I_D
V_{GS}

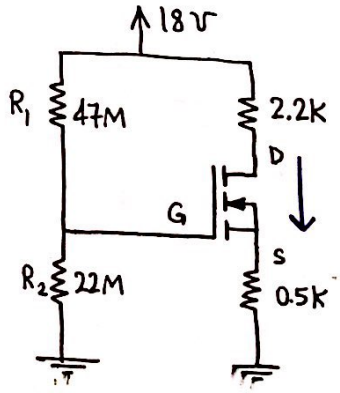


Example

$K_n = 0.25 \times 10^{-3}\ A/V^2$

$V_T = 2V$

n-Channel معناتها موجبة V_T لـ
P-Channel " سالبة V_T لـ



$I_{DS} = K_n\left(V_{GS} - V_T\right)^2 \ldots [1]$

$V_{GS} = V_G - V_S$

$V_G = \frac{22M}{22 + 47M} \cdot 18 = 5.74\ V$

$V_S = (0.5K)\, I_{DS}$

$V_{GS} = 5.74 - 0.5K\, I_{DS}$ ---[2]

$V_{GS} = 4.78\ V$ ✓ لازم اكبر من V_T
$= -8.78$ ✗

$I_{DS} = 1.92\ mA$

$V_{GS} = 12.82 > |V_{GS} - V_T|$

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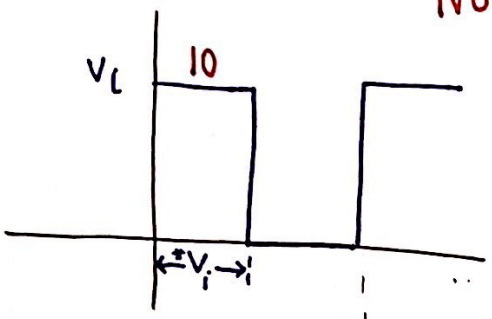
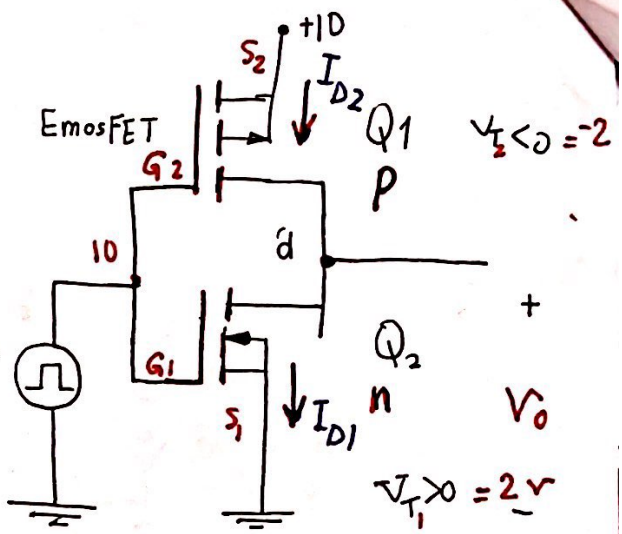
CMOS Inverter "Complementary MOS"

NOT Gate

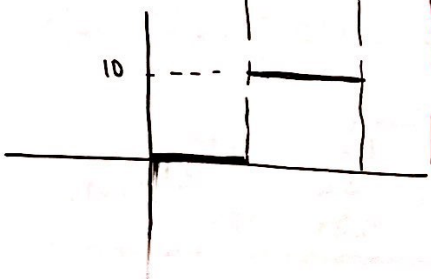


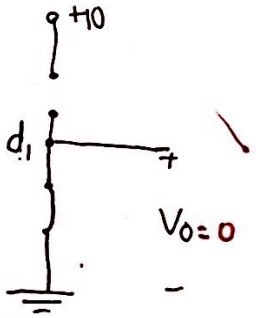


* $V_i = 10 = V_{GS1} > 2$ → يعني ممر (SC) بحط

$V_{GS2} = 0 > -2$ → يعني ~~قاطوع~~ OC بحط

إذا الانبوت 10 ⇐ الاوتبوت 0

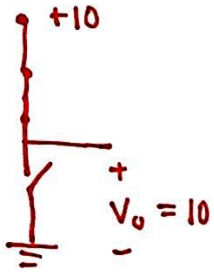




2 $V_i = 0V \Rightarrow V_{GS1} < 2$

Q_1-off

→ $V_{GS2} = 0-10 = -10 < -2$



هيك خلصنا لـ L10

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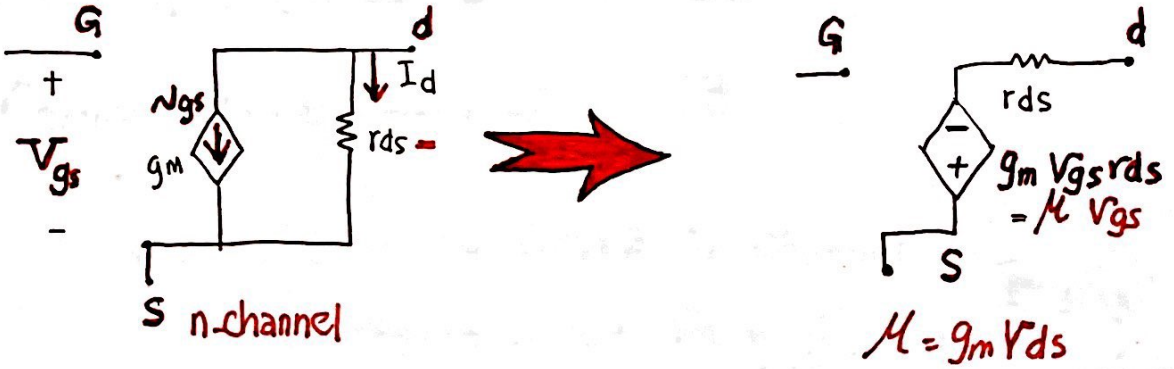
L11eNOTES : FET Amplifiers ac Small Signal analysis
I 16 AS Vidlos

For all FET Type



g_m - Transconductance

$\mu = g_m r_{ds}$

Amplification Factor

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \quad \Omega^{-1} \text{ mho} \quad [\text{Always + ve}] \quad [\text{Siemens}]$$

For JFET & DMOSFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\frac{\partial I_D}{\partial V_{gs}} = \frac{2 I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m_0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

dc value

$g_{mo} = g_m\big|_{V_{GS}=0}$

$\sqrt{\frac{I_D}{I_{DSS}}}$

$$= \frac{2 I_{DSS}}{|V_P|}\sqrt{\frac{I_D}{I_{DSS}}} = \frac{2}{|V_P|}\sqrt{I_D \cdot I_{DSS}}$$

For EMOSFET

$$I_D = K_n (V_{GS} - V_T)^2$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2K_n (V_{GS} - V_T)$$

$$= 2K_n \sqrt{\frac{I_D}{K_n}} = 2\sqrt{I_D K_n}$$

$K_n = \frac{I_D}{(V_{GS} - V_T)^2}$ @ the Q-point "dc value"

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FET Amplifier

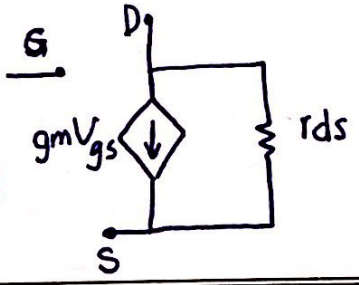
Common Sourse ⟶ eq. to CE "Input Gate, Output Drain"

Common Drain ⟶ eq. to CC

Common Gate ⟶ eq. to CB

all have the same eq. Circuit "n-channel"

For P-channel → current from S to D "↑"

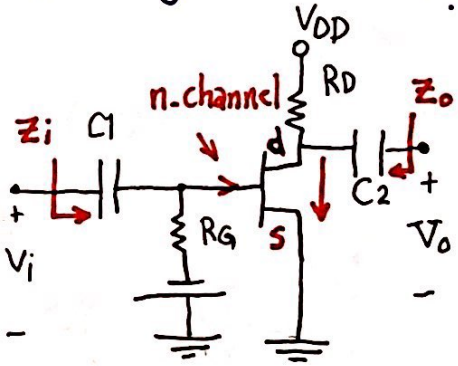


1 Common Source Amplifier with self Bias "Inverting" Yup!

Find A_V, Z_i, Z_o

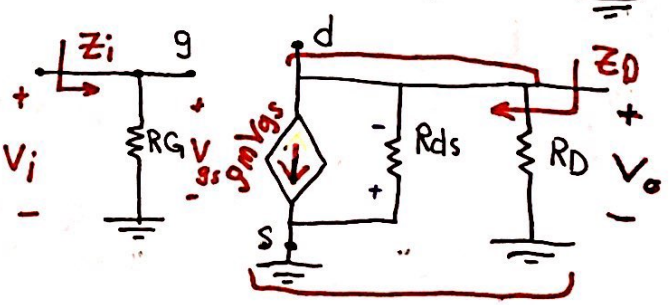
ac ss quantities ⟶ Construct ac eq. Circuit

- C_1, C_2 "Short"
- $V_{DD}=0$ (GND)
- JFET ac ss. Model



- $Z_i = R_G$
- $Z_o = R_D // r_{ds}$ (كبيرة كتير)

$V_i = 0$ لهيك مرات بتكون بتساوي الـ R_D



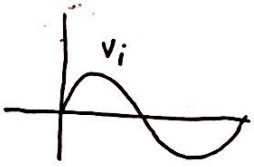
For this $r_{ds} \gg R_D$

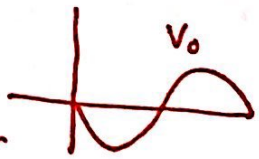
$\therefore Z_o = R_D$

R_{ds}, R_D → Shared Ground & Shared Drain

$$A_V = \frac{V_o}{V_i}$$

$$\begin{cases} V_o = V_{ds} = -g_m V_{gs} (r_{ds} // R_D) \\ V_i = V_{gs} \end{cases}$$





Inverting Amplifier
V_o is shifted 180° relative to V_i

$$A_V = \frac{-g_m V_{gs} (r_{ds} // R_D)}{V_{gs}} = -g_m (r_{ds} // R_D)$$

$$= -g_m (R_D)$$

.4.

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Common Source (self Bias)

$(r_{ds} \cong \infty)$

$V_{gs} \neq v_i$

$V_{gs} = V_g - V_s$

$V_{gs} = V_i - g_m v_{gs} R_s \Rightarrow V_{gs} = \dfrac{v_i}{1 + g_m R_s}$

$A_V = \dfrac{V_o}{V_i}$;

$V_o = -g_m v_{gs} R_D$

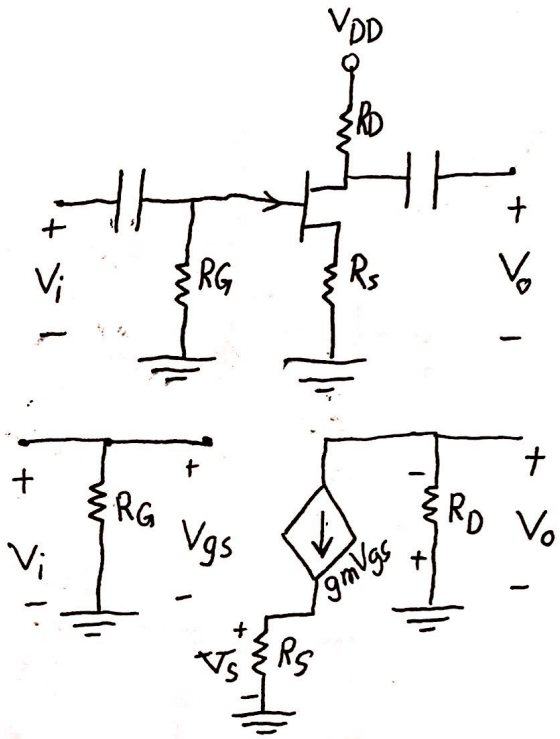
$V_{gs} = V_g - V_s$

$= V_i - \dots$

$A_V = \dfrac{-g_m R_D}{1 + g_m R_s}$;

(كبر المقام ← A_V تقل)

A_V is ↓ due to R_s



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