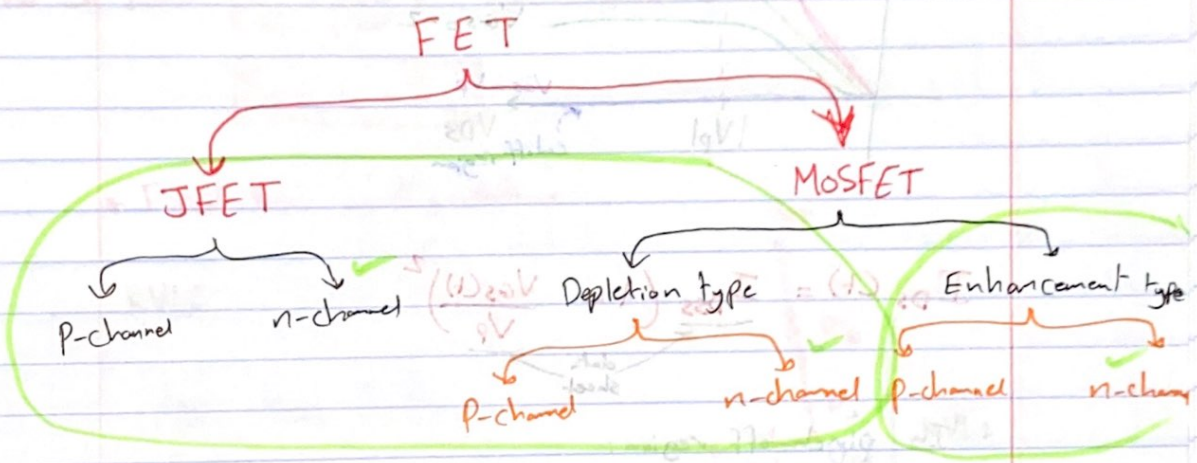
T10: Field Effect Transistor - FET

Adv.:

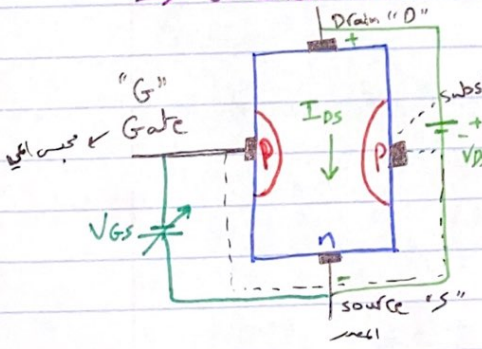
① High input impedence.
② Fewer steps in manufacturing.
③ smaller area.

disAdv.:

① low Voltage gain.
② Poor high frequency performance.
③ sensitive to (ESD). (special handling is required)



⇒ Junction Field Effect Transistor (JFET)



$I_{DS} = I_D = I_S$

إذا الفولتية $V_{GS} = -1$ ⇐ الويث بقل ⇐ التيار بقل

* كل ما زدنا قيمة الـ V_{GS} بنقل الويث والتيار

⇒ $V_{GS} = V_p$

↳ no channel

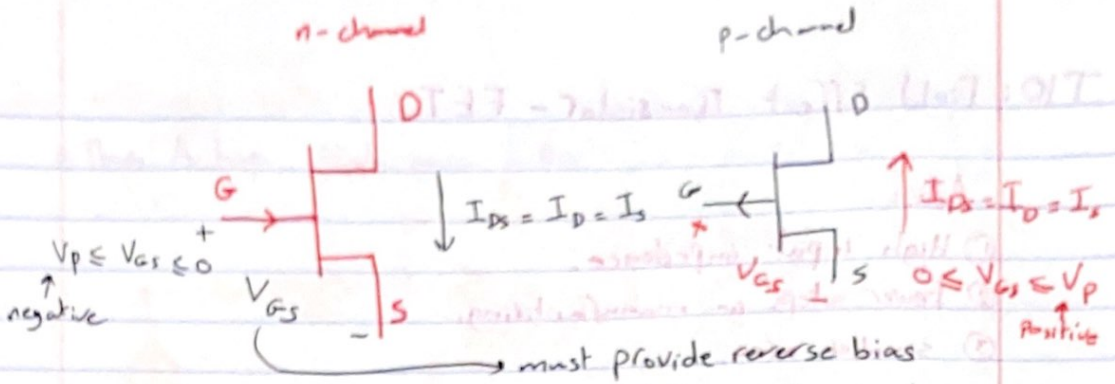
$I_D = 0$

$0 \le V_{GS} \le V_p$

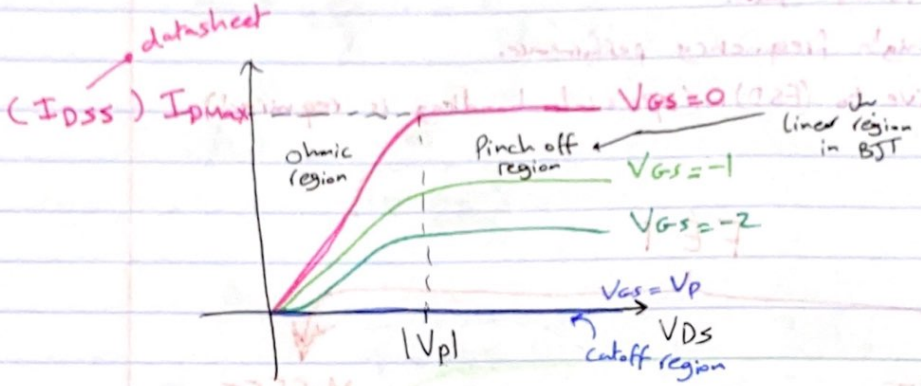
$I_D = max$ ← maximum channel width

minimum channel width ⇒ $I_D = 0$

$I_D = f(V_{GS})$



$I_G = 0$ (pn is reverse biased)



$$I_{DS}(\text{Ht}) = \underbrace{I_{DSS}}_{\text{data sheet}} \left(1 - \frac{V_{GS(\text{Ht})}}{V_P}\right)^2$$

In pinch-off region:

$$V_P < V_{GS} \leq 0$$

$$|V_{DS}| > |V_P| - |V_{GS}|$$

↳ for both n & p channel

Summary: Pinch off voltage ≡ active region in BJT

- For n-channel: $V_p < V_{GS} \leq 0$, $|V_{DS}| > |V_p| - |V_{GS}|$
- For p-channel: $V_p > V_{GS} \geq 0$, $|V_{DS}| > |V_p| - |V_{GS}|$

⟹ Common JFET Biasing Circuits

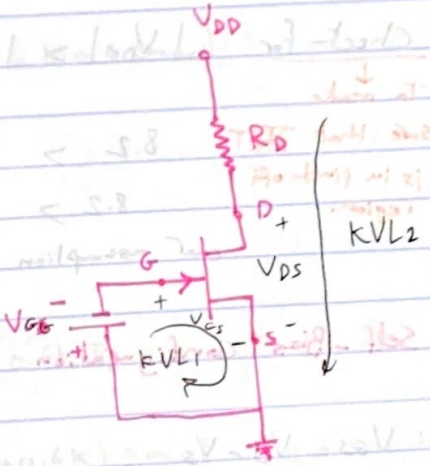
For JFETS: $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Given in the data sheet

For all FETS: $I_G \cong 0A$ ← gate-to-source junction is reversed bias

$$I_D = I_S = I_{DS}$$

* Fixed-Bias Configuration



KVL2:

$$V_{DS} = V_{DD} - I_D R_D$$

$V_S = 0 \Rightarrow V_{DS} = V_D$

KVL1:

$$V_{GS} = -V_{GG}$$

ex $V_p = -4V$, $I_{DSS} = 10mA$, V_{DD}, $R_D = 2K$, R_G, 1M, 9.5

Find V_{GS} & I_D & V_{DS}?

Assume in pinch-off region

KVL2 $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

$$I_D = 10m\left(1 - \frac{V_{GS}}{-4}\right)^2$$

KVL1:

1) $\boxed{V_{GS} = -1.5V}$

2) $I_D = 10m\left(1 - \frac{-1.5}{-4}\right)^2$

3) $\boxed{I_D = 3.9mA}$

KVL2:

3) $16 = I_D R_D + V_{DS}$

$16 = (3.9m)(2k) + V_{DS}$

$\boxed{V_{DS} = 8.2V}$

4) Check for $|V_{DS}| > |V_p| - |V_{GS}|$?

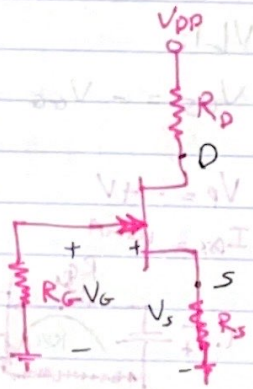
To make sure that JFET is in pinch off region.

$8.2 > 4 - 1.5$

$8.2 > 2.5$ ✓

our assumption is true.

* Self-Bias Configuration



KVL1: $V_{GS} = V_G - V_S$

$V_{GS} = -V_S$

$V_{GS} = -I_D R_S$ ——— (1)

KVL2: $V_S = I_D R_S$

$V_D = V_{DD} - I_D R_D$

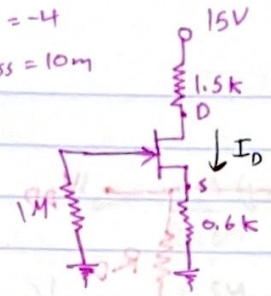
OR

$V_{DS} = V_D - V_S$

$V_D = V_{DS} + V_S$

$V_p = -4$

$I_{DSS} = 10m$



ex Find V_{GS}, I_D, V_{DS}?

KVL1: $V_{GS} = -I_D R_S$

$V_{GS} = -I_D (0.6)k$ —— ①

assume pinch-off region:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 10m\left(1 - \frac{V_{GS}}{-4}\right)^2$$ —— ②

$$I_D = 10m\left(1 - \frac{+I_D(0.6k)}{+4}\right)^2$$ ← quadratic equation

$$ax^2 + bx + c = 0$$

$$x_{1,2} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

$I_{D1} = 14.7mA$ X ($I_{DSS} = 10mA$ (max))

$\boxed{I_{D2} = 3mA}$

$V_{GS} = -I_D (0.6k)$

$\boxed{V_{GS} = -1.8V}$

KVL2: $-15 + 1.5k I_D + V_{DS} + 0.6k I_D = 0$

$V_{DS} = 15 - (1.5k + 0.6k)\,3m$

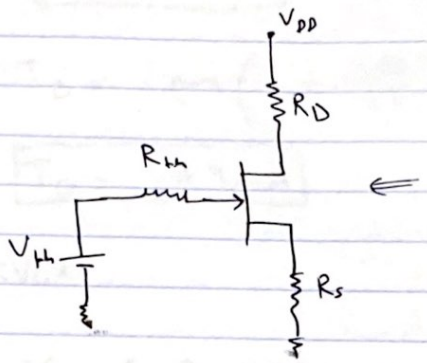
$\boxed{V_{DS} = 8.7V}$

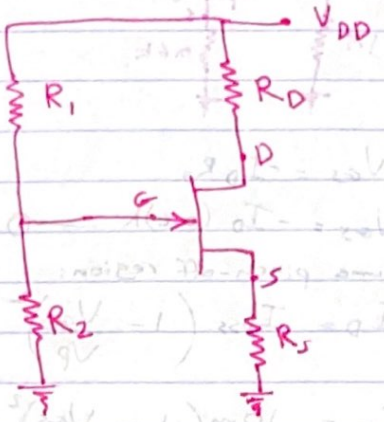
check: $|V_{DS}| > |V_P| - |V_{GS}|$?

$8.7 > 4 - 1.8$ ✓

assumption is true.

* Voltage-Divider Bias





$$V_{Th} = \frac{R_2}{R_1 R_2} V_{DD}$$

$$V_G = V_{Th} -$$

$$V_G = \frac{R_2}{R_1 R_2} V_{DD}$$

$$V_{GS} = \frac{R_2}{R_1 R_2} V_{DD} - I_D R_S \quad \text{——①}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{——②}$$

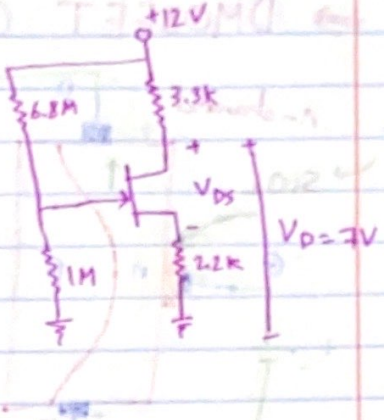
(1) in (2):

$$I_D = I_{DSS}\left(1 - \frac{V_G - I_D R_S}{V_P}\right)^2$$

$I_{D1} \longrightarrow ?$

$I_{D2} \longrightarrow ?$

ex



$$V_G = \frac{1M}{7.8M}(12) = \boxed{1.54V}$$

$$V_{GS} = 1.54 - 2.2k I_D$$

$$V_D = -3.3k I_D + 12$$

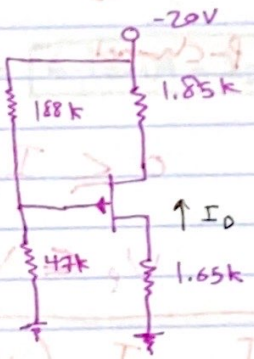
$$3.3k I_D = 12 - 7$$

$$\boxed{I_D = 1.52mA}$$

$$\boxed{V_{GS} = -1.8V}$$

$$V_{DS} = V_D - V_S$$
$$= 7 - (2.2k)(1.52)$$
$$\boxed{V_{DS} = 3.656V}$$

ex p-channel:



$V_p = 5$

$I_{DSS} = 18mA$

$$V_{GS} = \frac{47k}{188k}(-20) + I_D(1.65k)$$

$$V_{GS} = -4 + 1.65k I_D \quad \text{—— ①}$$

Assume pinch-off region:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$I_D = 18m\left(1 - \frac{V_{GS}}{5}\right)^2 \quad \text{—— ②}$$

① in ②:

$$I_D = 18m\left(1 - \frac{-4 + 1.65k I_D}{5}\right)^2$$

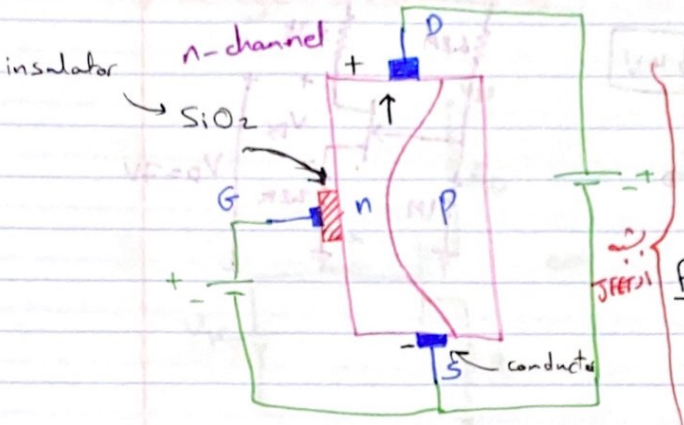
$I_{D1} = 4.7mA$ ✓ $\rightarrow$ $V_{GS} = 3.75 < V_p$ ✓

$I_{D2} = 7.4mA$ ✓ $\rightarrow$ $V_{GS} = 8.21 > V_p$ ✗

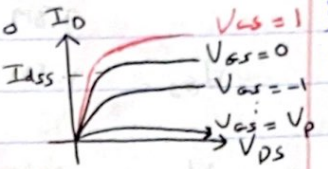
$\boxed{I_D = 4.7mA}$, $\boxed{V_{GS} = 3.75V}$

[27:00][1:00:49]

⇒ DMOSFET (Depletion MOSFET)



for $V_{GS} = 0$



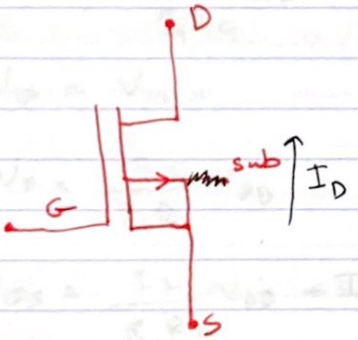
for $V_{GS} = -1$

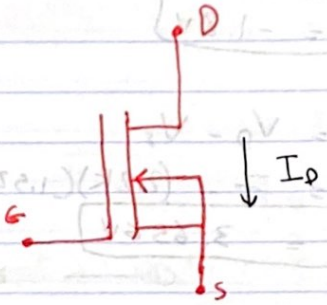
width decreases

I_D becomes less

for $V_{GS} = V_p$

for $V_{GS} = 1$





P-channel n-channel

$$0 \leq I_D \leq I_{DSS}$$

$$V_p \leq V_{GS} \leq 0$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad *$$

→ for $V_p \leq V_{GS} \leq 0 \Rightarrow 0 \leq I_D \leq I_{DSS}$

Depletion mode

→ for $V_{GS} > 0 \rightarrow I_D > I_{DSS}$

Enhancement mode

- for n-channel

$V_{GS} > V_p$ (negative) *

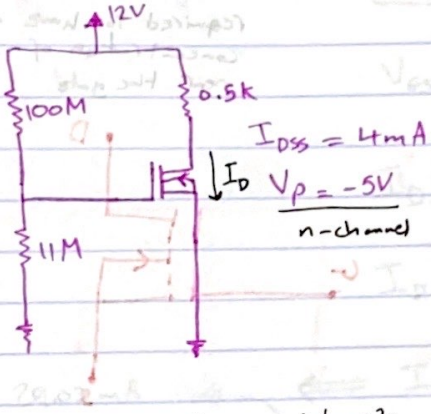
$V_{DS} > V_{GS} - V_p$

- for p-channel

$V_{GS} < V_p$ (positive) *

$V_{DS} < V_{GS} - V_p$

ex



$I_{DSS} = 4mA$

$V_p = -5V$

n-channel

Suppose in pinch-off region:

$V_G = \frac{11M}{(11+10g)M}(12)$

$\boxed{V_G = 1.19V}$

$\boxed{V_{GS} = V_G = 1.19V}$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$

$= 4m\left(1 - \frac{1.19}{-5}\right)^2 = \boxed{6.13mA = I_D}$

~~$I_D = 4.952mA$~~

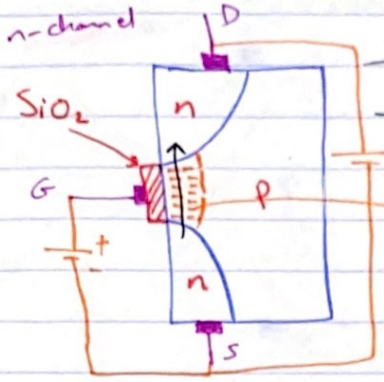
$V_{DS} = 12 - 0.5k(6.13m)$

$\boxed{V_{DS} = 8.935V}$

$V_{DS} > \underbrace{V_{GS} - V_p}_{6.19V}$ ✓

our assumption is true!

⇒ EMOSFET (Enhancement MOSFET)



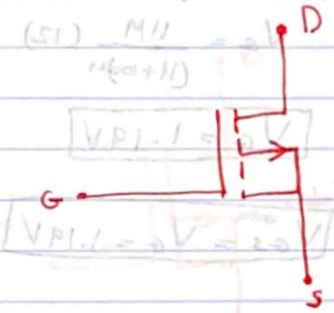
→ no physical channel

→ we will have an induced channel due to V_{GS}

$V_{GS} > V_{GS(th)} = V_T$

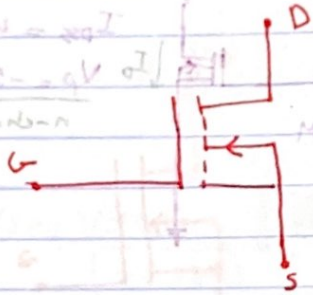
→ gate-to-source threshold voltage

→ This is the minimum voltage required to have a good concentration of carriers near the gate.



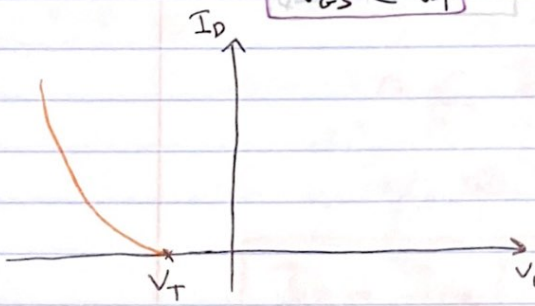
p-channel

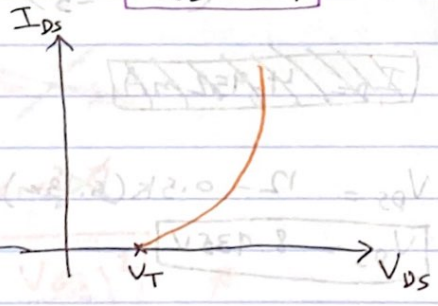
$V_{GS} < V_T$



n-channel

$V_{GS} > V_T$



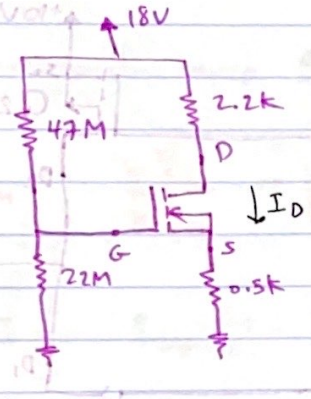


$$I_D = K_n (V_{GS} - V_T)^2$$

$$K_n = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$

$|V_{DS}| > |V_{GS} - V_T|$ → both n & p channels

ex Find V_{GS}, I_D, V_{DS}?



$k_n = 0.25 mA/V^2$

$V_T = 2V$ must be given
$\neq 25.7 mV$

$V_G = \frac{22M}{(22+47)M}(18)$

$\boxed{V_G = 5.74V}$

$V_{GS} = 5.74 - 0.5k I_D$ ——①

$I_D = k_n (V_{GS} - V_T)^2$

$I_D = 0.25m (5.74 - 2 - 0.5 I_D)^2$

$\Leftarrow I_D = 0.25m (3.74 - 0.5k I_D)^2$

$I_{D1} = 29.03 mA$
$I_{D2} = 1.92 mA$
$V_{GS1} = -8.775 < V_T$ ✗
$V_{GS2} = 4.78V$ ✓

$\Rightarrow \boxed{I_D = 1.92mA}$

$\boxed{V_{GS} = 4.78V}$

$18 = (2.2k)(1.92) + V_{DS} + (0.5k)(1.92m)$

$\boxed{V_{DS} = 12.816V}$

To check $|V_{DS}| > |V_{GS} - V_T|$
$12.816 > 2.78$ ✓

23:30

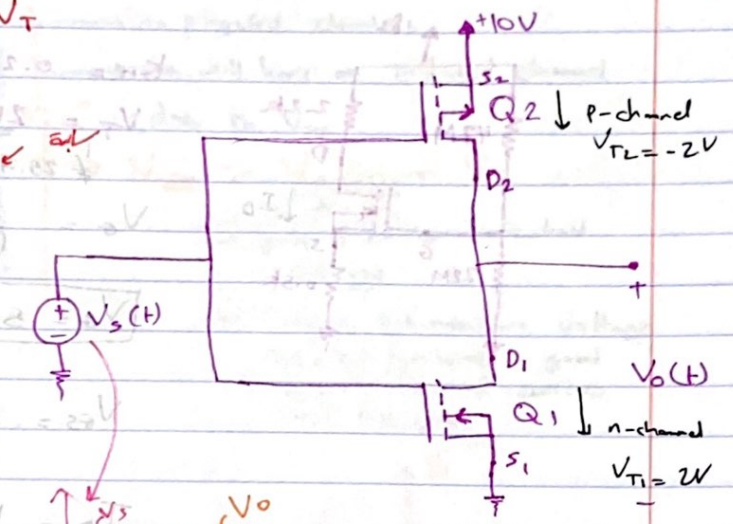
⇒ Complementary MOS (CMOS) inverter

n-channel: $V_{GS} > V_T$

if $V_{GS} \gg V_T$

$V_D \simeq 0V$ (short)

p-channel: $V_{GS} < V_T$



* $[0, t_1]$

$V_{GS1} = V_{G1} - V_{S1}$

$= 10 - 0$

$V_{GS1} = 10V \gg V_{T1}$ (2V)

⇒ Q1 is on, replaced with short circuit

$V_{GS2} = V_{G2} - V_{S2}$

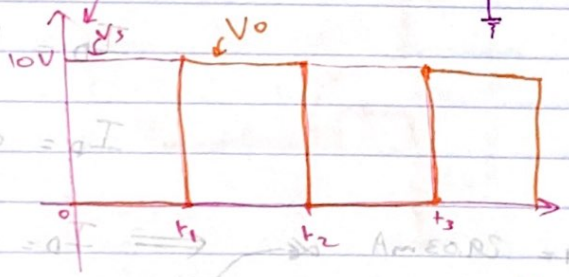
$= 10 - 10$

$= 0V$

$V_{GS} \overset{?}{<} V_T$

$0 \overset{?}{<} 2$ ✗

⇒ Q2 is off, replaced with open circuit ⟹



$V_o = 0V$

* $[t_1, t_2]$

$V_{GS1} = V_{G1} - V_{S1}$

$V_{GS1} = 0V$

$V_{GS1} \overset{?}{>} 2V$

$0 \overset{?}{>} 2$ ✗

⇒ Q_1 is off, replaced with open circuit

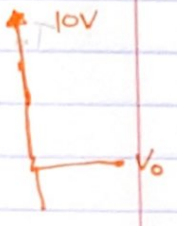
$V_{GS2} = V_{G2} - V_{S2}$

$= 0 - 10$

$V_{GS2} = -10V$

$V_{GS2} \overset{?}{<} V_{T2}$

$-10 < -2$ ✓



⇒ Q_2 is on, replaced with short circuit ⟹

$V_o = 10V$

33:00

* FET Amplifiers & AC small signal analysis

⇒ Transconductance g_m ← always positive

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \rightarrow \left[\frac{A}{V}\right] = \frac{1}{\Omega} = \Omega^{-1} = \text{siemens}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

OR

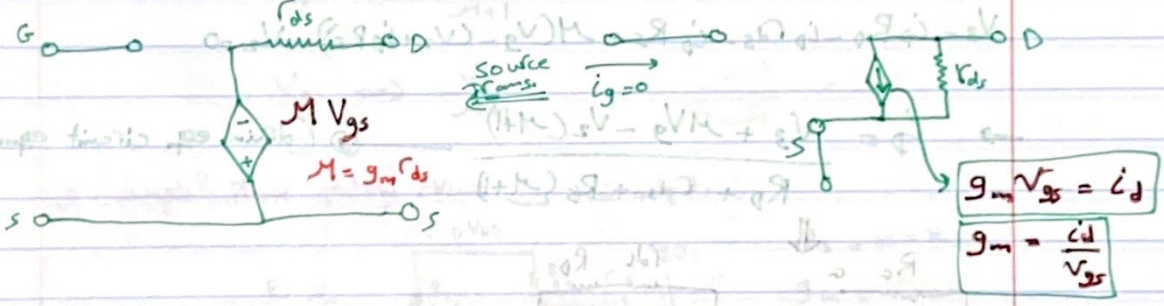
$$I_D = K_n(V_{GS} - V_T)^2$$

* JFET & DMOSFET

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right] = g_{mo}\sqrt{\frac{I_D}{I_{DSS}}} \; ; \; g_{mo} = \frac{2I_{DSS}}{|V_P|} = g_m\Big|_{V_{GS}=0}$$

* EMOSFET

$$g_m = 2\sqrt{I_D K}$$ ← constant; ← dc analysis



FET Amplifier

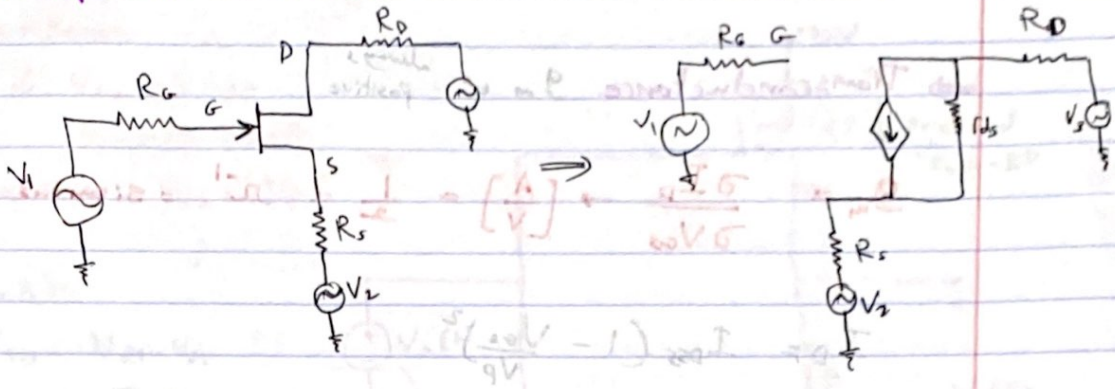
BJT

have the same ac ss eq. circuit

1. Common Source (CS) → CE
2. Common Drain (CD) → CC
3. Common Gate (CG) → CB

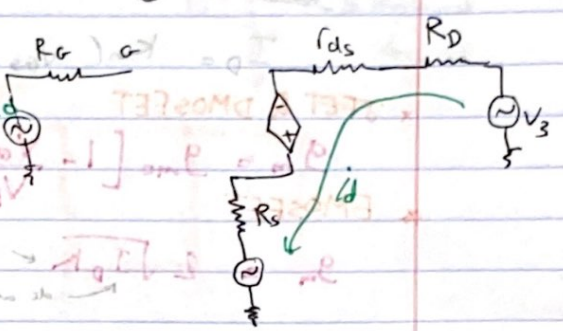
- To construct ac ss eq. circuit:
  1. C_1 & C_2 replaced by short circuit.
  2. $V_{DD} = 0$ (short), $V_{GS} = 0$ (short)
  3. FET ac ss MODEL

⇒ Impedence Reflection



⇓

• KVL for drain-source loop



① ⟶ $V_3 - i_D R_D - i_D r_{ds} + \mu V_{gs} - i_D R_S - V_2 = 0$

$V_{gs} = V_g - V_s$

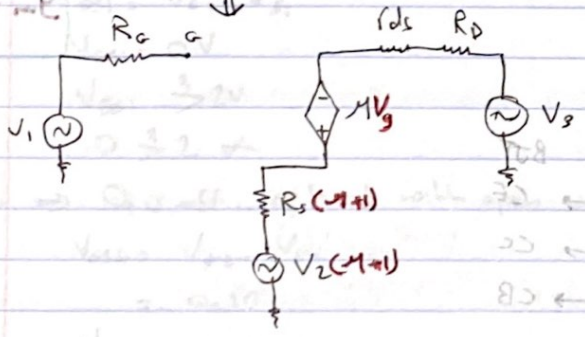
$V_{gs} = V_g - (V_2 + i_D R_S)$ ⟶ ②

② in ①

$V_3 - i_D R_D - i_D r_{ds} - i_D R_S + \mu(V_g - (V_2 + i_D R_S)) - V_2 = 0$

$\Rightarrow i_D = \dfrac{V_3 + \mu V_g - V_2(\mu+1)}{R_D + r_{ds} + R_S(\mu+1)}$ ⟶ ③ (drain eq. circuit equation)

⇓



Reflection from source to drain:

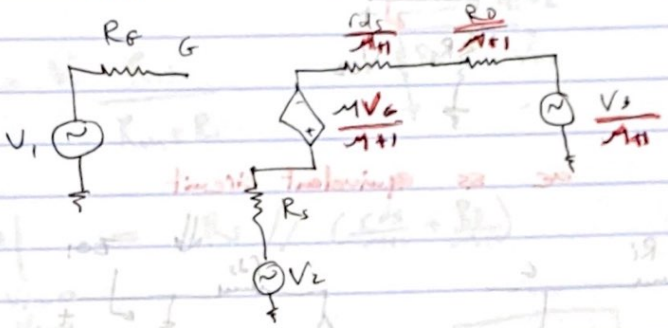
$\mu V_{gs} \Rightarrow \mu V_g$

$R_S \Rightarrow R_S(\mu+1)$

$V_2 \Rightarrow V_2(\mu+1)$

divide eq. (3) by $(\mu+1)$

$$i_d = \frac{\frac{V_3}{\mu+1} + \frac{\mu V_3}{\mu+1} - V_2}{\frac{R_D}{\mu+1} + \frac{r_{ds}}{\mu+1} + R_s} \quad \text{(4) (source eq. circuit equation)}$$



Reflection Drain to source:

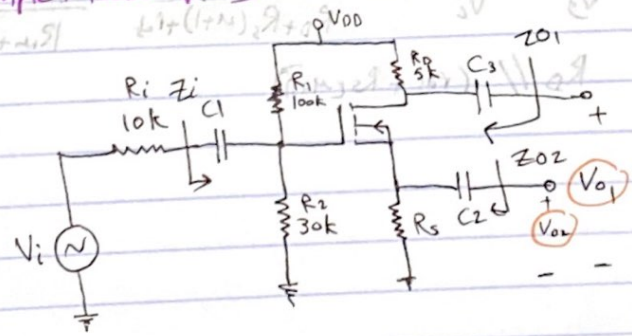
$$\mu V_G \Rightarrow \frac{\mu V_G}{\mu+1}$$

$$R_D \Rightarrow \frac{R_D}{\mu+1}$$

$$r_{ds} \Rightarrow \frac{r_{ds}}{\mu+1}$$

$$V_3 \Rightarrow \frac{V_3}{\mu+1}$$

⇒ example: Phase splitting circuit → two outputs



$r_{ds} = 100\ k\Omega$

$g_m = 1\ mS$

* Find A_v, ~~A_i~~, Z_{O1}, Z_{O2}, Z_i

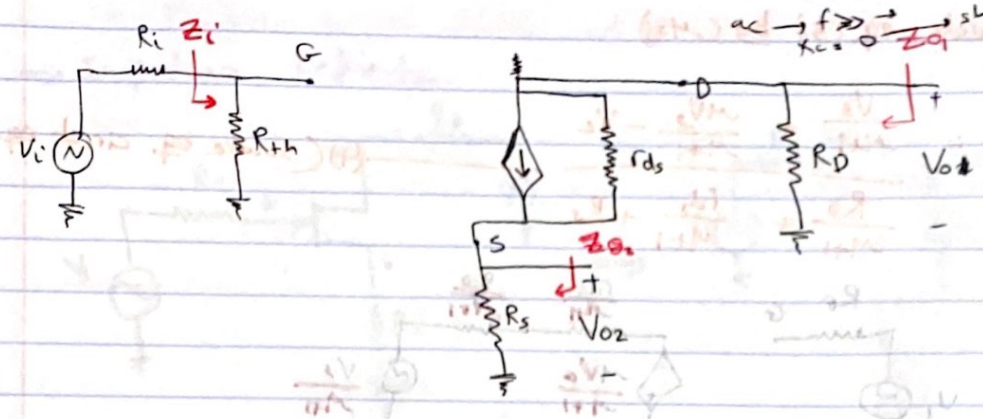
↳ $A_{V1} = \frac{V_{O1}}{V_i}$

↳ $A_{V2} = \frac{V_{O2}}{V_i}$

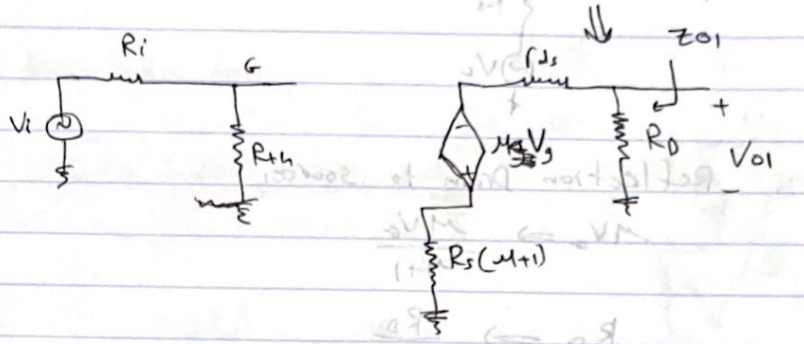
$$X_C = \frac{1}{2\pi f C}$$

dc → $f = 0$, $X_C = \frac{1}{0} = \infty$ → open

ac → $f \gg$ → $X_C = 0$ → short



ac ss equivalent circuit



$$V_{o1} = \frac{R_D}{R_D + R_s(\mu+1) + r_{ds}} \cdot (-\mu V_g) \quad \text{(Voltage Divider)}$$

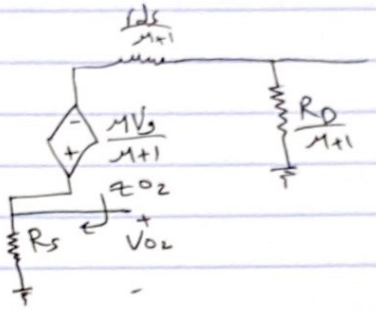
$$V_G = \frac{R_{th}}{R_{th} + R_i} \cdot V_i$$

$$A_{V_1} = \frac{V_{o1}}{V_g} \times \frac{V_g}{V_i} = \frac{-\mu R_D}{R_D + R_s(\mu+1) + r_{ds}} \cdot \frac{R_{th}}{R_{th} + R_i}$$

$$Z_{o1}\Big|_{\substack{V_i = 0 \\ V_g = 0 \\ \mu V_g = 0 \\ \text{(short)}}} = R_D \,//\, (r_{ds} + R_s(\mu+1))$$

. To Find V_{o2} :

$$V_{o2} = \frac{R_s}{R_s + \frac{r_{ds}+R_D}{\mu+1}} \left(\frac{\mu V_g}{\mu+1} \right)$$



$$V_g = V_i \frac{R_{th}}{R_{th}+R_i}$$

$$Z_{o2}\Big|_{\substack{V_i=0 \\ V_g=0 \\ \frac{\mu V_g}{\mu+1}=0}} = R_s \,//\, \left(\frac{r_{ds}}{\mu+1} + \frac{R_D}{\mu+1} \right)$$

$$\boxed{\mu = g_m r_{ds}}$$

if $r_{ds} \longrightarrow \infty \Rightarrow$ $\boxed{Z_{o2}\Big|_{r_{ds}=\infty} = R_s \,//\, \frac{1}{g_m}}$

$$\lim_{r_{ds}\to\infty} \frac{r_{ds}+R}{\mu+1} = \lim_{r_{ds}\to\infty} \frac{r_{ds}+R}{g_m r_{ds}+1} = \frac{1+\frac{R}{r_{ds}}^{\,0}}{g_m + \frac{1}{r_{ds}}^{\,0}} = \frac{1}{g_m}$$

$$Z_i = R_{th}$$

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