Faculty of Information Technology

Electrical Engineering Department

ANALOG ELECTRONICS

ENEE 236_Q2

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Abstract:

The aim of this assignment is to design a Common Emitter (CE) Amplifier with Voltage Divider Bias. And to be able to calculate the unknown resistors from the DC Analysis, and to use h-parameter AC Analysis to make the amplifier with the aimed Voltage Gain (Av) and input Impedance (Zi).

Notes for the assignment:

1) RL=100kohm
2) Aimed impedance (Zi) must be >10kohm
3) Aimed Voltage Gain (Av) must be around -50 at 5kHz frequency
4) 12V < Vcc < 18V
5) 12uF < Caps < 18uF

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❖ Qustion2:

Design a Common Emitter Amplifier using **QbreakN** npn transistor from pspice .

- Use voltage divider bias configuration.
- Assume load resistor RL= 100kohm,
- The amplifier input Impedance must be > 10 kohm
- Voltage gain Av= -50 (at 5kHz)
- 12 < Vcc <18 V
- 12uF < Caps <18uF

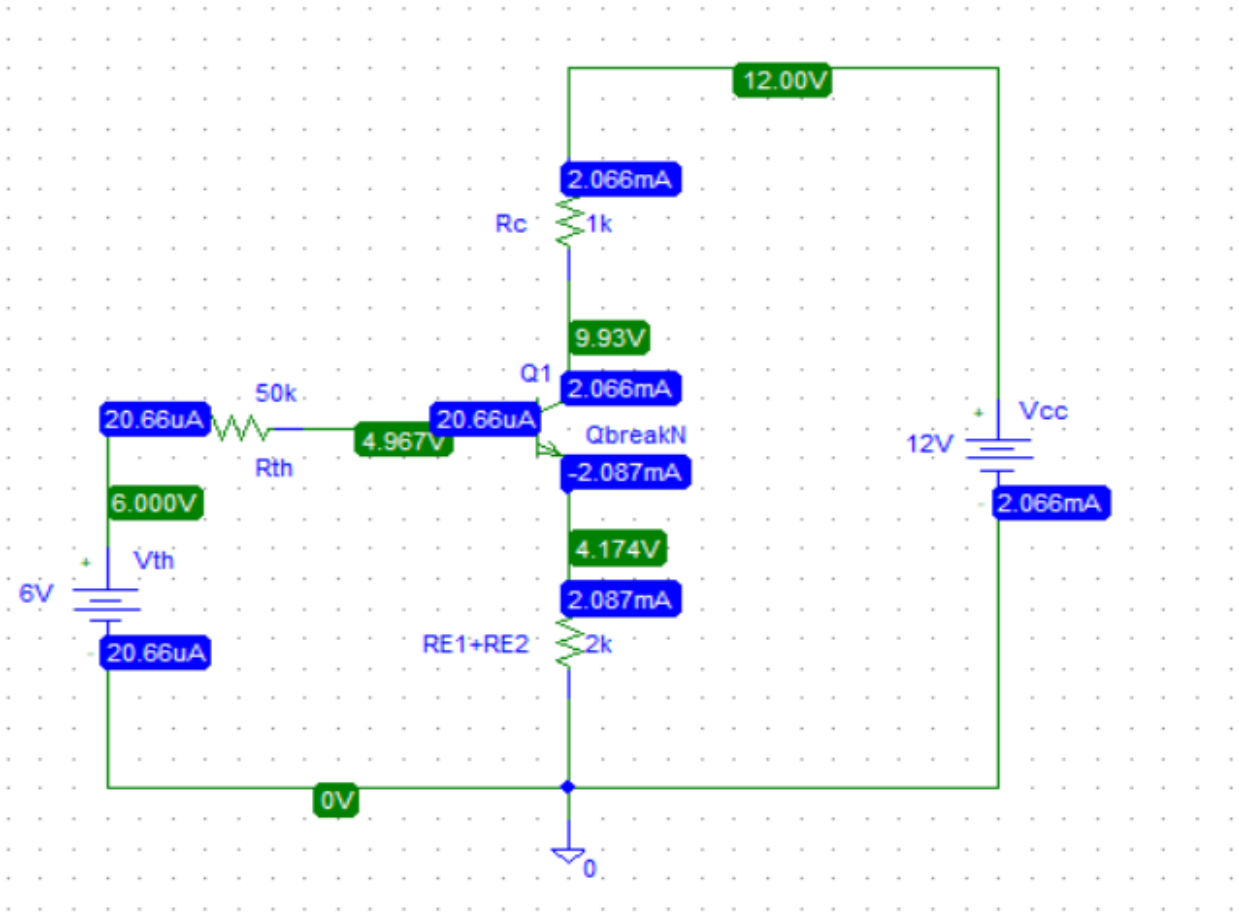
1. Test the transistor in pspice using a simple thevinin equivalent bias circuit to estimate its current gain value beta that will be used in further calculations (use bias point detail)
2. Design the dc bias such that VCE is approximately 0.5Vcc , 1mA < Ic < 5mA
3. Test the voltage gain with input sinusoidal signal that has an amplitude =10 mV and different frequencies: 1kHz, 5kHz and 10kHz (use transient analysis)
4. Test the voltage gain with an ac signal with amplitude=1V using ac sweep (decade type from 1Hz to 10MHz) , plot Vo and dB(Vo)

Show all design steps using methods learned in the course and use h-parameter equivalent circuit in your modeling

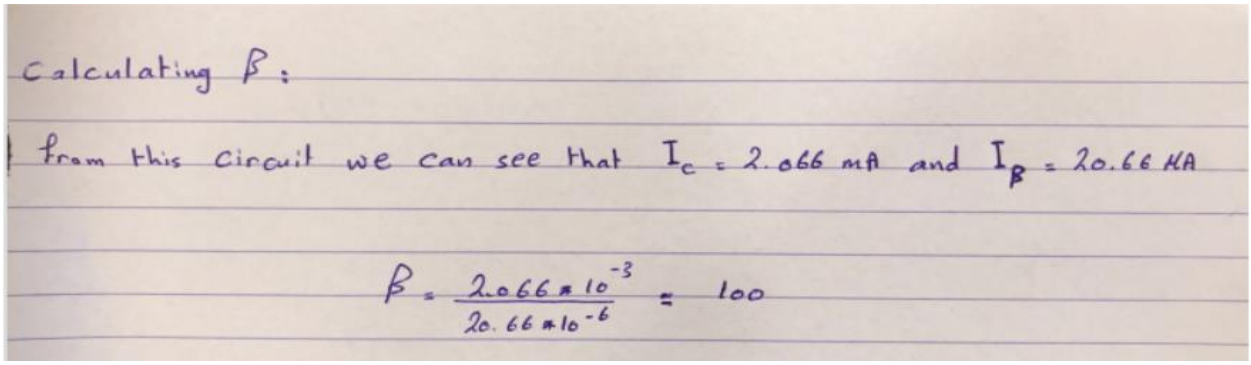
❖ Procedure:

- **1) Calculating the Current Gain value B.**

To calculate the current gain value B, I used a DC simple thevinin equivalent circuit shown in this figure:



To calculate B:



- **2) Designing DC bias circuit with VCE=0.5VCC and 1mA < Ic < 5mA.**

The calculations:

Designing D.c voltage Divider Bias

Thevenin equivelant circuit :

* to make Z_i as high as possible, V_{cc} should be high and I_{CQ} should below:

$1mA \leq I_c < 5mA \Rightarrow \boxed{I_{CQ} = 1.5\,mA}$

$12 < V_{cc} < 18 \Rightarrow \boxed{V_{cc} = 18}$

* calculations :

$V_{CEQ} = 0.5\,V_{cc} = 9\,V$ assume $V_E = 1.8\,V$

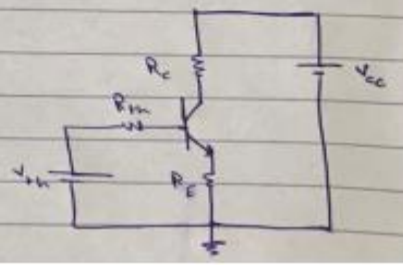
* $I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.5\,mA}{100} = 15\,\mu A$

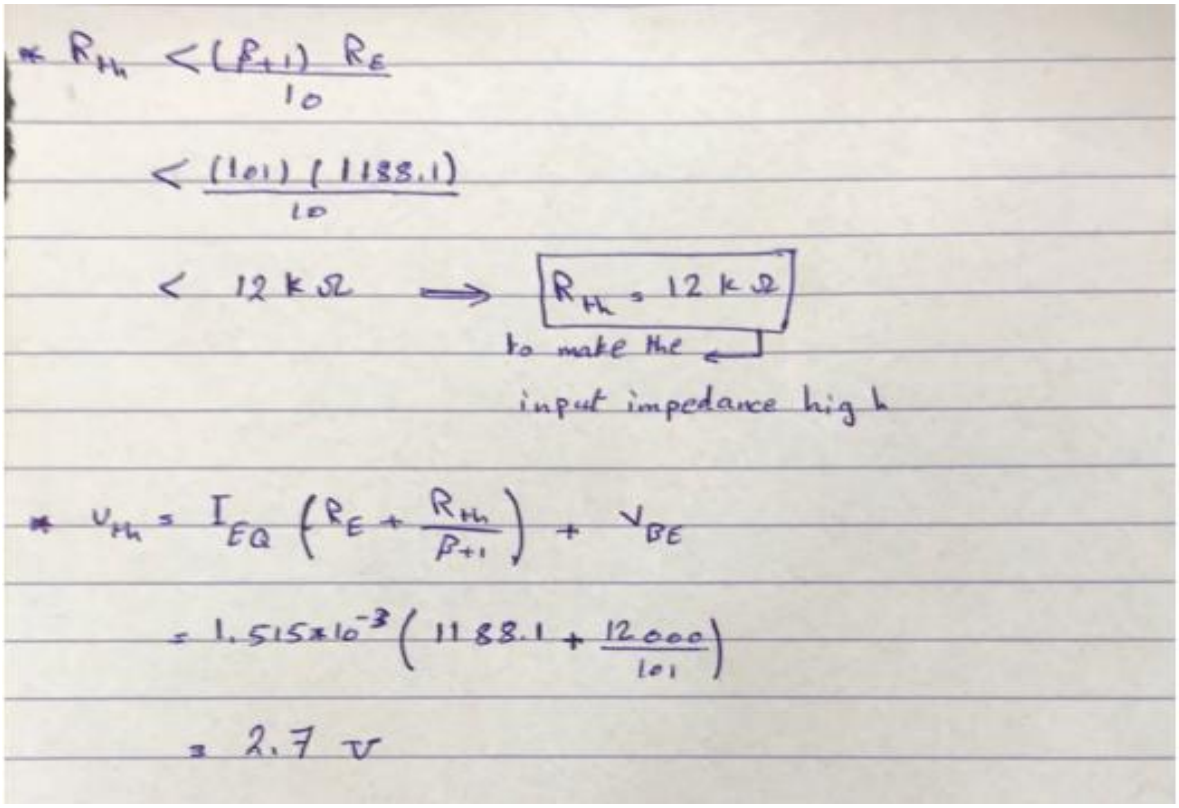
* $I_{EQ} = I_{CQ} + I_{BQ} = 1.515\,mA$

* $R_E = \frac{V_E}{I_{EQ}} = \frac{1.8}{1.515 \times 10^{-3}} = 1188.1\,\Omega$

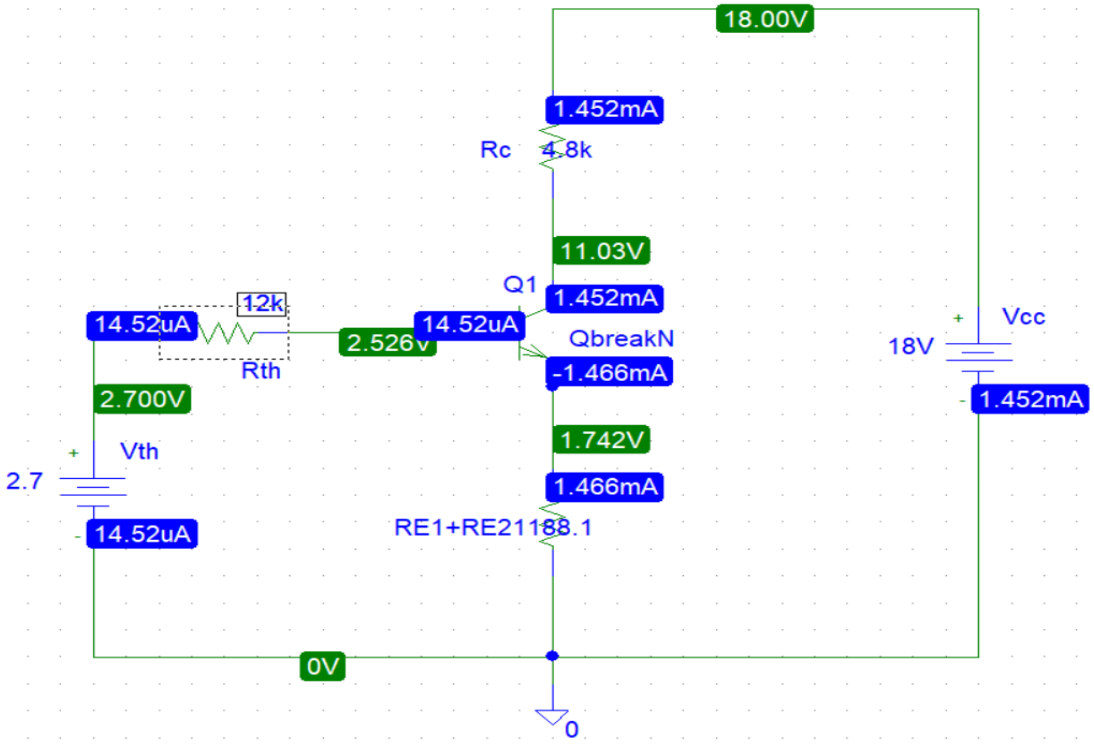
* $R_C = \frac{V_{cc} - V_{CEQ} - I_{EQ} R_E}{I_{CQ}}$

$= \frac{18 - 9 - 1.515 \times 10^{-3} \times 1188.1}{1.5 \times 10^{-3}} = 4.8\,k\Omega$



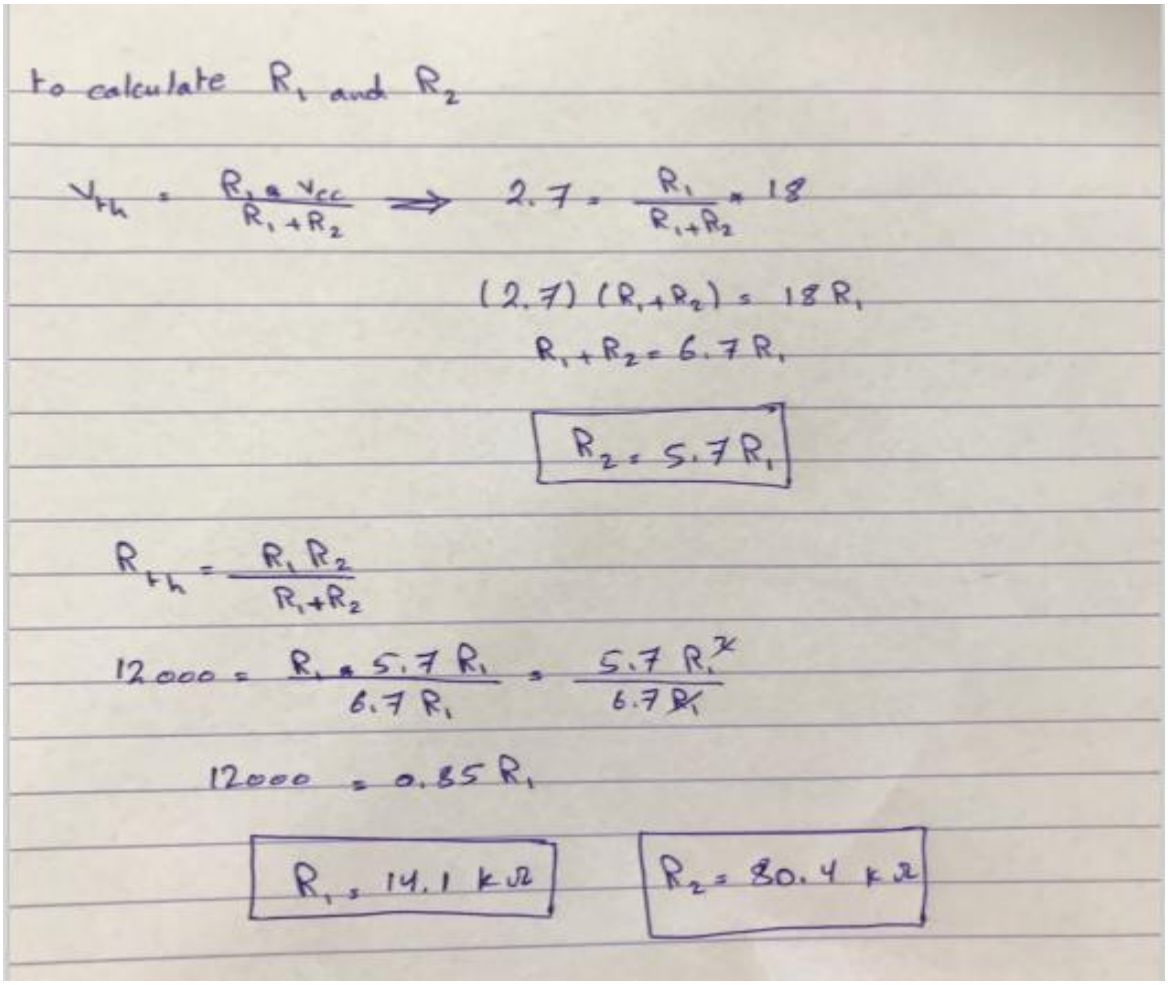

* $R_{TH} < \frac{(\beta+1) R_E}{10}$
$< \frac{(101)(1188.1)}{10}$
$< 12\,k\Omega \Longrightarrow \boxed{R_{TH} = 12\,k\Omega}$
to make the input impedance high
* $V_{TH} = I_{EQ}\left(R_E + \frac{R_{TH}}{\beta+1}\right) + V_{BE}$
$= 1.515\times10^{-3}\left(1188.1 + \frac{12000}{101}\right)$
$= 2.7\ V$

The circuit:


18.00V
1.452mA
Rc
4.8k
11.03V
Q1
1.452mA
12k
14.52uA
14.52uA
2.526V
QbreakN
Rth
-1.466mA
18V
Vcc
2.700V
1.452mA
1.742V
Vth
2.7
1.466mA
14.52uA
RE1+RE21188.1
0V
0

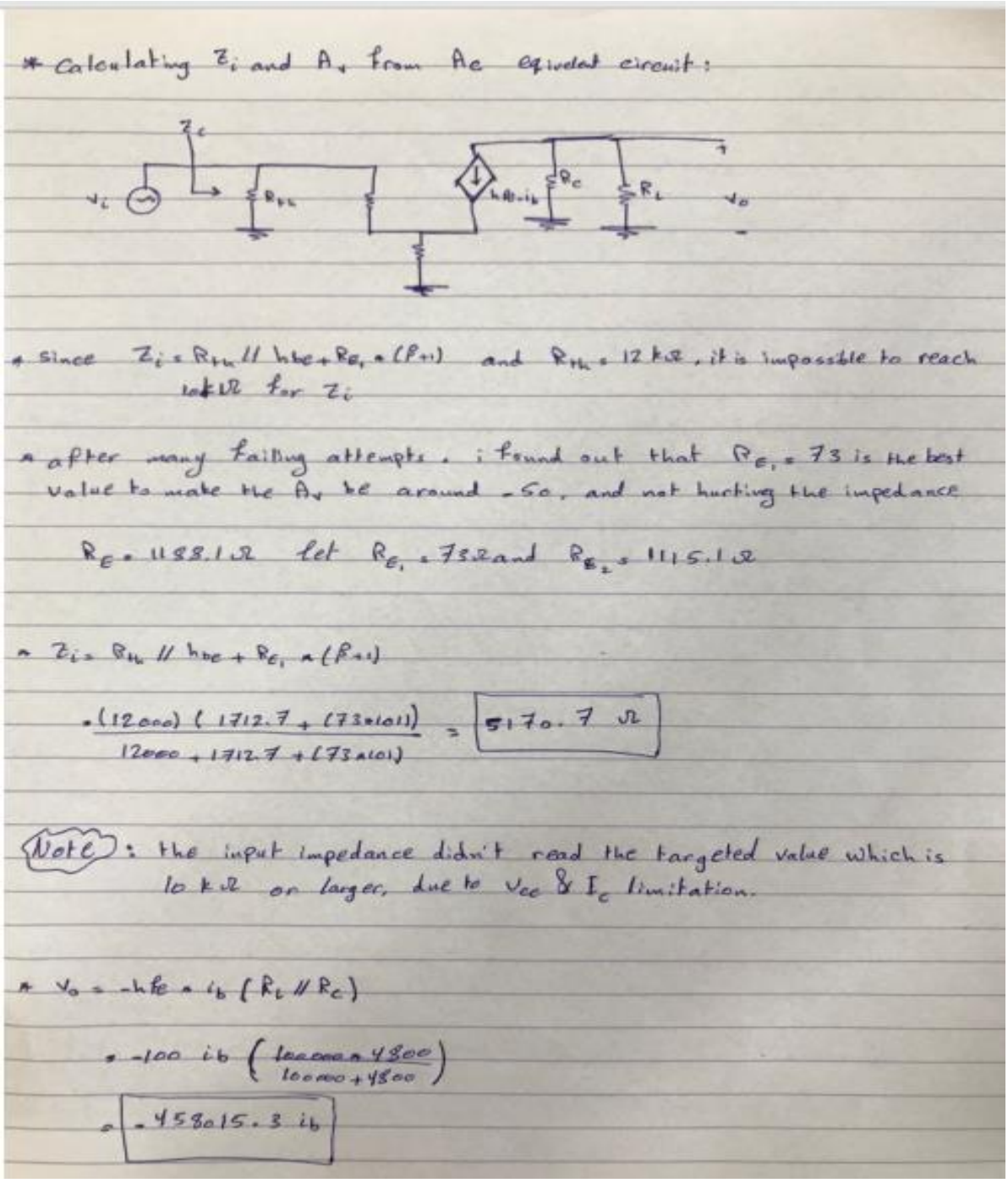
We can see that Ic=1.452mA, still in the range that we aimed for, and also we can see that VCE=(11.03-1.742)=9.3V, it is very close to the aimed VCEQ which is 0.5Vcc=9V.

Now, to calculate R1 and R2 (They will be used in the final circuit):



- **3) Testing Voltage Gain using transient analysis.**

Supposing there is no (Ri), these are the calculations for (Zi) and Av, assuming RE1=73ohm (I had so many different attempts to find out that this value of RE1=73ohm is great to have Av around the aimed -50, and also not making the input impedance (Zi) drop by much), We can note that (Zi) did not reach 10kohm because it is impossible to reach that because it must be less than (Rth) which is 12kohm.



* $V_i = Z_i \, i_i = \boxed{5170.7 \, i_i}$

* $i_b = \dfrac{R_{TH}}{R_{TH} + h_{ie} + R_{E_1}(\beta+1)}$

$i_i = \dfrac{12000 + 1712.7 + (73.101)}{12000} \, i_b$

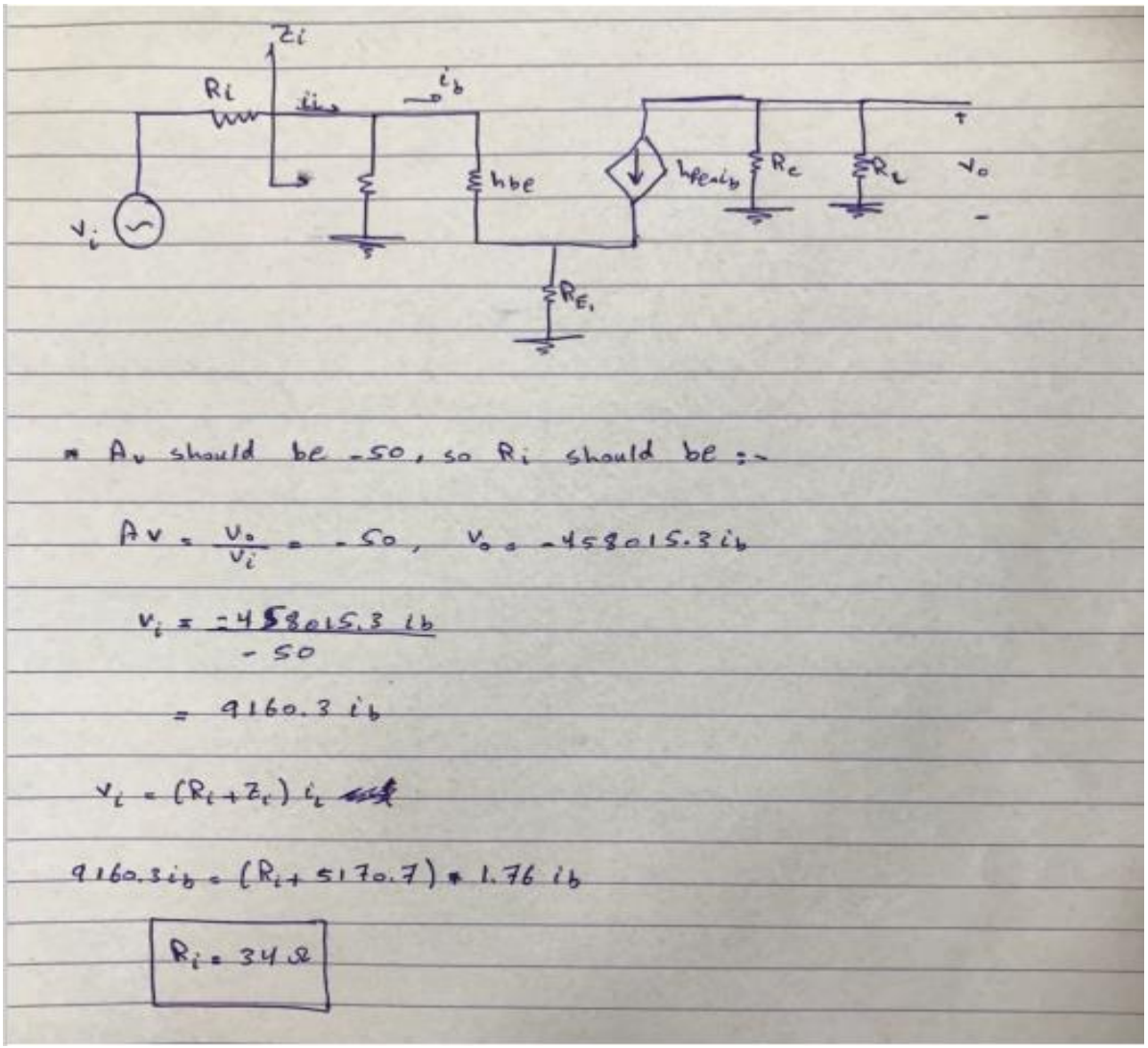
$\boxed{i_i = 1.76 \, i_b}$

* $V_i = Z_i * i_i = \boxed{9100 \, i_b}$

* $A_V = \dfrac{V_o}{V_i} = \dfrac{-458015.3 \, i_b}{1.76 * 5170.7} = \boxed{-50.329}$

it is a little higher than the aimed -50 so we need a resistor R_i

After making these calculations assuming (Ri) does not exist, we can see that Av turned out to be (-50.329), but we aimed for (-50), so we need to have (Ri), this is the calculations of (Ri) to have the theoretical value of (Av) equal exactly (-50).



* A_v should be -50, so R_i should be :-

$$A_v = \frac{V_o}{V_i} = -50, \quad V_o = -458015.3\, i_b$$

$$V_i = \frac{-458015.3\, i_b}{-50}$$

$$= 9160.3\, i_b$$

$$V_i = (R_i + Z_i)\, i_i$$

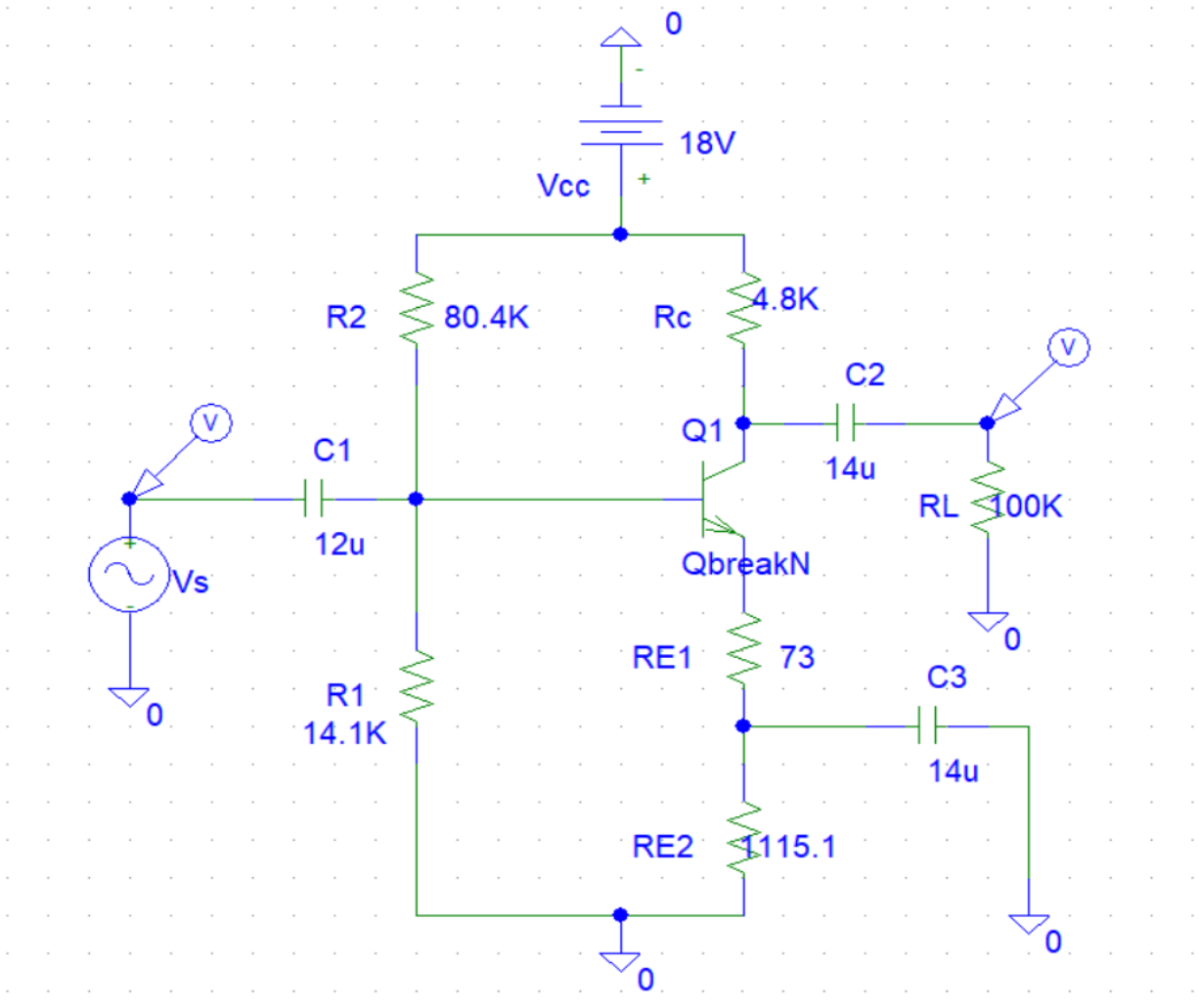
$$9160.3\, i_b = (R_i + 5170.7) * 1.76\, i_b$$

$$\boxed{R_i = 34\ \Omega}$$

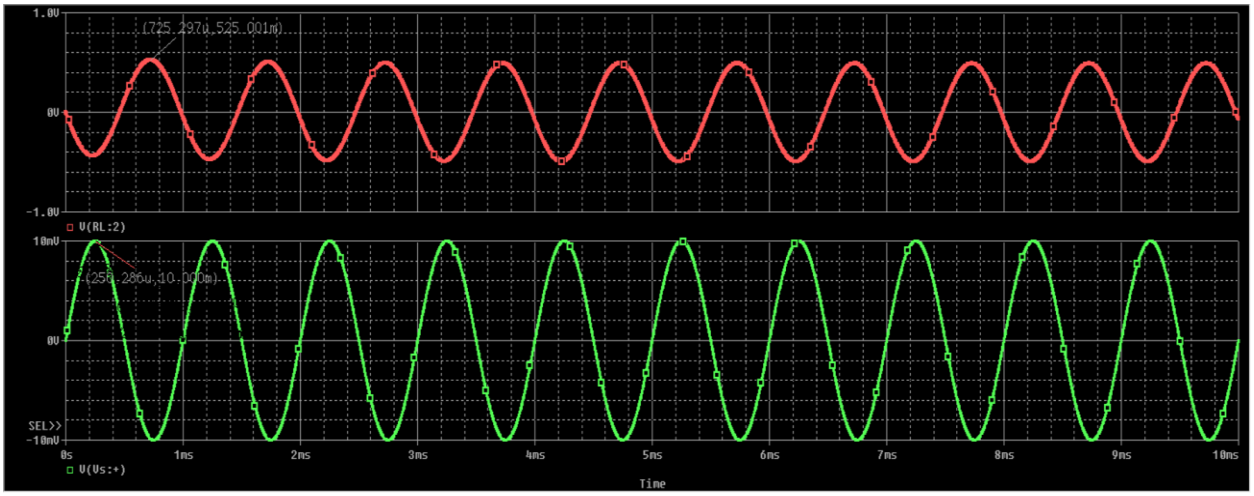
Now that we have all the unknowns ready, we can finally test the Voltage Gain in the main circuit that is shown in this figure:

Note that I put 14uF for the capacitor which is in the range that we were asked for.

Note: The Vsin has amplitude 10mV.



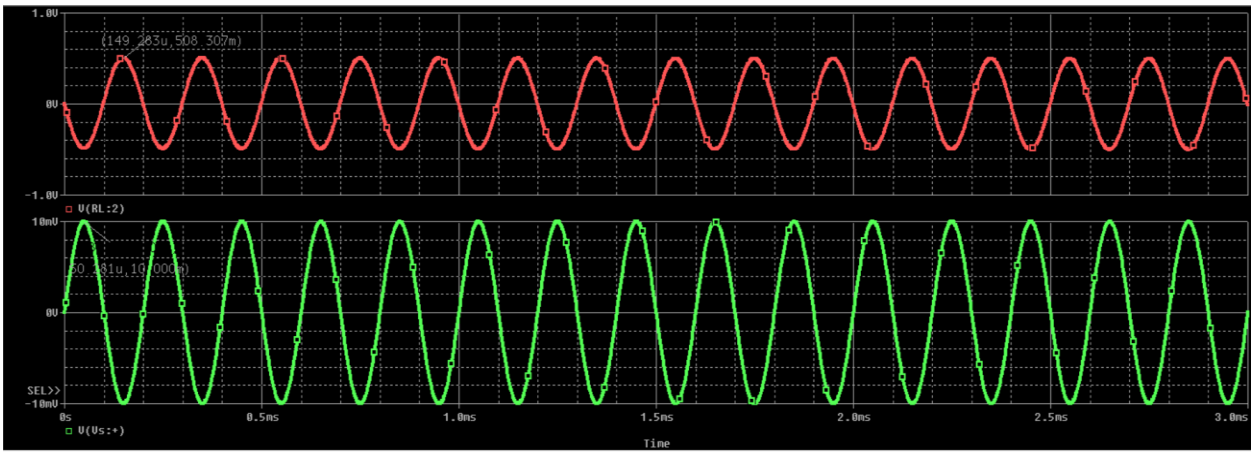
Test1: 1kHz. (Vo in red, Vin in green)



We can see that the output peak value is 525.001m, and the input was 10m,

So **Av=-52.5,** which is very close to the aimed -50.

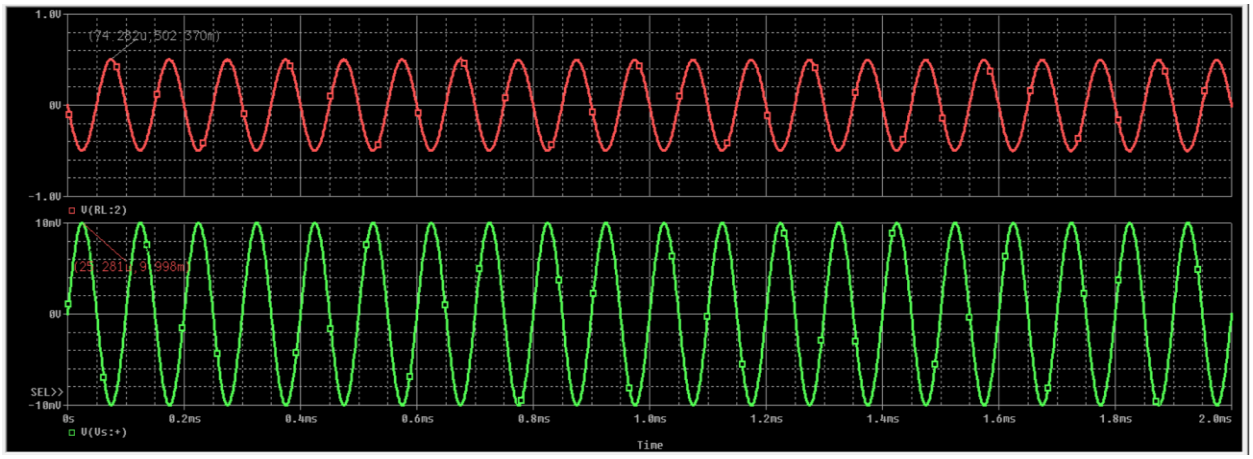
Test2: 5kHz. (Vo in red, Vin in green)



We can see that the output peak value is 508.307m, and the input was 10m,

So **Av=-50.8,** which is very close to the aimed -50.

Test3: 10kHz. (Vo in red, Vin in green)



We can see that the output peak value is 502.370m, and the input was 9.998m,

So **Av=-50.2,** which is very close to the aimed -50.

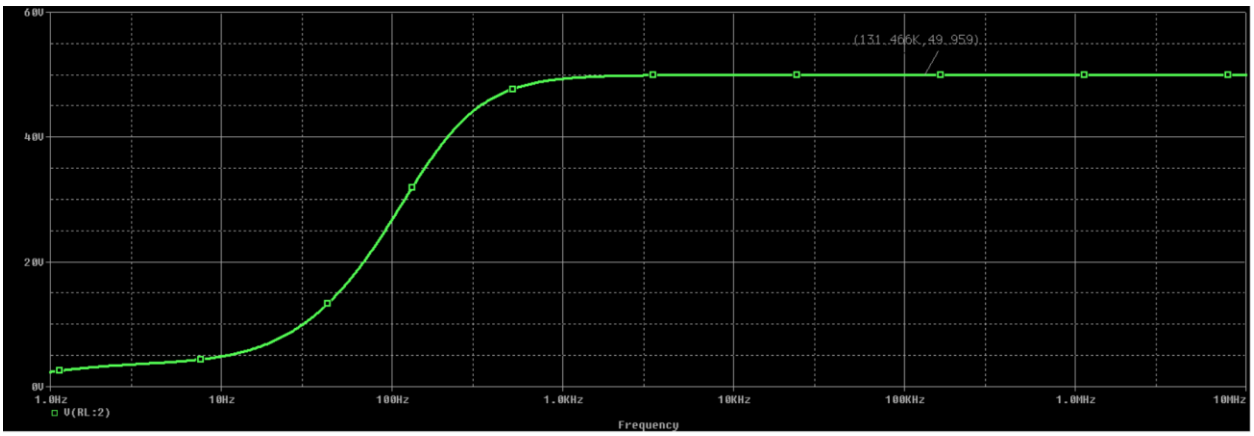
Results:

	Theoretical	PSPice at 1kHz	PSPice at 5kHz	PSPice at 10kHz
Voltage Gain (Av)	*-50*	*-52.5*	*-50.8*	*-50.2*

- **4) Testing Voltage Gain using AC sweep.**

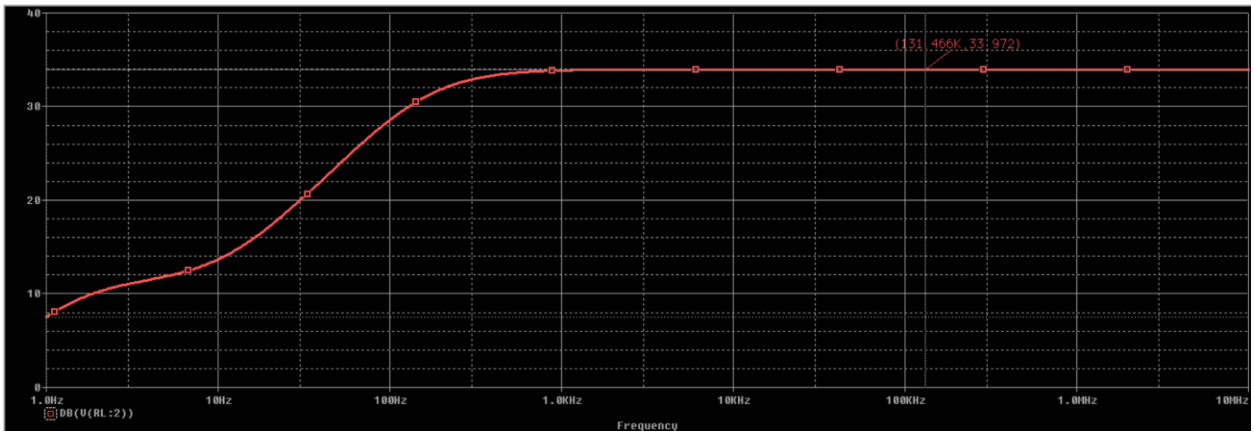
Note: The AC amplitude is 1V, decade type from 1Hz to 10MHz.

The Plot of Vo:



The peak value is 49.959, so **Av=-49.959.**

The Plot of dB(Vo):



The peak value is 33.972, so:

20Log (-Av) = 33.972

Log (-Av) = 1.6986

-Av = 49.95

Av=-49.95.

Results:

	Theoretical	Vo Plot	dB(Vo) Plot
Voltage Gain (Av)	*-50*	*-49.959*	*-49.95*

❖ Conclusion and Discussion:

After finishing this Question, we learnt a lot about designing amplifiers using the BJT Transistor, and how we can use software like PSpice to simulate it, and how we can use the DC Analysis and h-parameter AC Analysis to find out what is the values of the unknown resistors and to make the amplifier close to the aimed Voltage Gain (Av).

We can note that the BJT Transistor that we used is QbreakN has the Current Gain value (B) of 100.

The value of the input impedance should always be less than (Rth), and the value of (Rth) cannot exceed 10kohm and that is because of the limitations of the range of (Ic) and the range of (Vcc), probably if I assumed that (Ve)=0.2*(Vcc), the values of (RE) and (Rth) would be higher that what I got, but still there is no way that it could exceed 10kohm, and even if it does, it would affect the Voltage Gain and prevent it from being around -50.

For the tests of the Voltage Gain (Av) at different frequencies, we can see that all of the had a Voltage Gain (Av) around -50, which is what we aimed for, but by looking at the graph of the AC sweep, we can note that if we take a value that is less than 1kHz, we might have a lower Voltage Gain (Av).