

Faculty of Engineering and Technology

Electrical and Computer Engineering Department

**ENEE 3102 – Electronics Lab**

Pre-lab for Experiment No.5

**The Field-Effect Transistor**

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Sec#: 1

**Part 1: CHARACTERESTICS OF AN N-CHANNEL JFET**

The circuit below was built using PSpice simulation as shown:



The potentiometer was setting anti-clockwise and the variable dc voltage to zero, the plot of ID against VDS shown in figure below at difference values of VGS and VDS:



When VDS was set to 10 V and VGS to -1.0 V, The values of DC currents were shown in figure below, noticed that IG = 880.68 fA.



**Part 2: A JFET AMPLIFIER**

The circuit below was built using PSpice simulation as shown:



The frequency of the sine wave generator was set to 1 kHz with amplitude equal zero, the value of the set value of the potentiometer as shown in figure below equal 0.602 to make VDS = 10V

The plot of the output voltage when the input voltage equal 2V peak-to-peak:



From the figure above, noticed that the output voltage is approximately between 3.6V and 13.7V, so the peak value approximately equal 5V.

Voltage gain (AV) = VO / Vin = 5

The plot of the AC input voltage:



The plot of the AC input current:



Zi = Vi / Ii = 1 / 1u = 1 Mega

**Part 3: COMMON DRAIN AMPLIFIER**

The circuit below was built using PSpice simulation as shown:



The frequency of the sine wave generator was set to 1 kHz with amplitude equal zero, the DC voltages were shown in figure below:



From the circuit above, the values of VG and VS:

VG = 652.17 mV

VS = 12.11V

The plot of the output voltage when the input voltage equal 0.4V peak-to-peak:



From the figure above noticed that the peak value of output voltage equal 159 mV.

Voltage gain (AV) = VO / Vin = 0.795.

The plot of the output voltage and input voltage:



From figure above noticed that the phase shift between the input and output voltage is approximately equal zero.

Zin = Vi / Ii = 12.17 V / 65.22 µA = 168599.2

ZO = VO / IO = 12.11 V / 12.11 mA = 1000

**Part 4: CONSTANT CURRENT SOURCE**

The circuit below was built using PSpice simulation as shown:



The graph below shows the plot of ID against VDC at difference values of RL, ID on the y-axis:



Its clearly from the figure shown ID is linearly proportional with the DC voltage and reach the steady state value which is approximately equal 12 mA (constant current).