

**Faculty of Engineering and Technology**

**Electrical and Computer Systems Engineering**

ENEE3102

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***Course Name***

ELECTRONICS LAB (section 2)

***Experiment No. 4***

The Field-Effect Transisto*r*

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Hiam arar

***Date of Experiment***

March 12, 2016

***Date Submitted***

March 19, 2016

**-** **Abstract:**

**- Objective:**

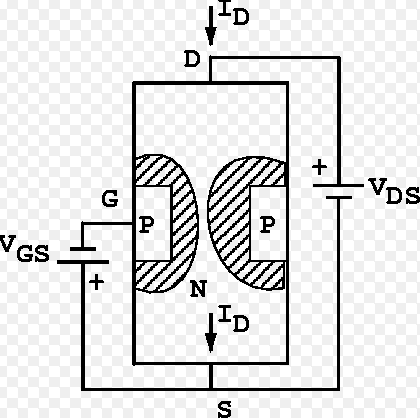
The aim of the experiment is to get understand the difference between the bipolar and field effect transistor and gets an ideaabout thecharacteristics of an n-channel JFET and how it is work as amplifier.

**- Theory:**

The Field Effect Transistor (FET) is a three terminal device. Three terminals are Drain (D), Source (S) and Gate (G). FETs have some advantages **like high input impedance (100 ), fewer steps in manufacturing and more devices can be package into smaller area for integrated circuit IC , however it have some disadvantages such as low values of voltage gain and poor high frequency performance .**

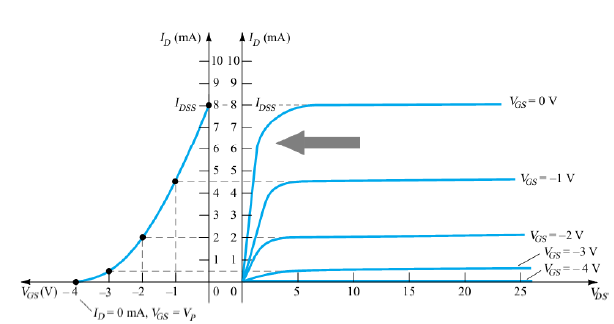
**Two types of JFET: 1) N-channel JFET as shown in fig (1)**

**2) P- channel JFET**

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**Fig (1) : N-channel JFET**

In this experiment we will obtain output characteristics of N-channel FET as we show in fig (1), reverse biasing the gate to source junction cause the formation of depletion region, the drain has the proper polarity with respect to the source to establish the drain current I DS, the value of I DS depends on the width of the channel, the width of the channel is controlled by reverse biasing the pn junction between gate and source. If the channel width increases IDS increase. And the voltage causes the depletion region to touch close the channel is called pinch off voltage

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**Fig (2): JFET transfer** characteristics **curve**

**As show in fig (2) different region represented ohmich region, pinch off region and cut off region. And the VGS (t) can show.**

**IDS (t) = IDSS (1- ) 2**

**In the pinch off region for n-channel:**

**VP < VGS (t) 0**

**- Experimental / Procedure:**

*I. CHARACTERESTICS OF AN N-CHANNEL JFET.*

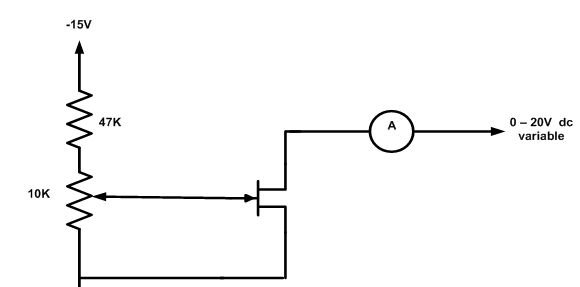
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Fig (3)

Circuit shown in fig(3) was connected , power supply was switch on , and VDS was set to the first value in table (1) and then ID was read for each value of VGS, all steps were repeated for all values of VDS and ID was being recorded .

II. A JFET AMPLIFIER.

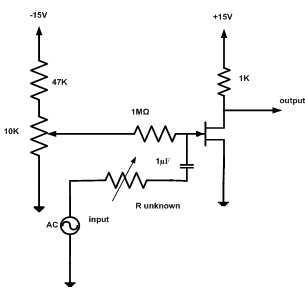
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Fig (4)

Circuit in fig (4) was connected and the sine wave generator was set to 1 KHz and its output amplitude turned to zero, the potentiometer was set to give a value of +10 v for VDS and R unknown to zero. Now input was applied to 2 volts peak to peak from the generator and then the output was observed on the oscilloscope and now the output voltage was measured and then the R unknown was increased until the output signal about half its original size .

*III. COMMON DRAIN AMPLIFIER.*

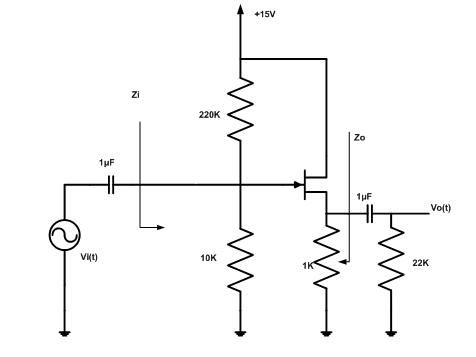


Fig (5)

Circuit in fig (4) was connected and the sine wave generator was set to 1 KHz and its output amplitude turned to zero, the DC voltages of VG and VS was measured, now input was applied to 2 volts peak to peak from the generator and then the output was observed on the oscilloscope, finally the input and output impedances was measured.

IV. CONSTANT CURRENT SOURCE.

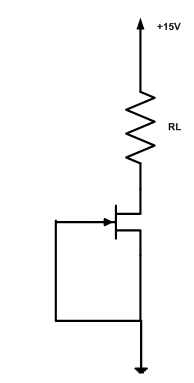


Fig (6)

The circuit shown in fig(6) was connected , the VR was measured and ID was calculated for each value of the resistor , then the result was recorded in table (2) .

***- Calculations:***

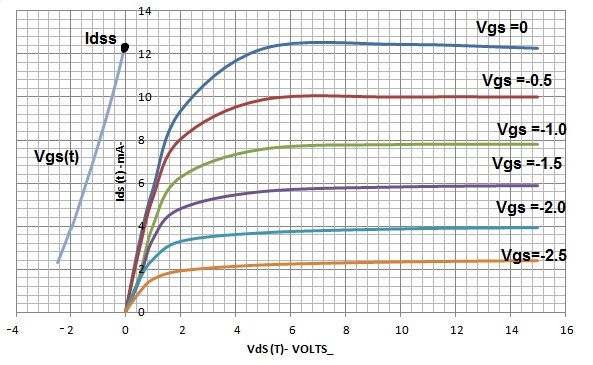
*I. CHARACTERESTICS OF AN N-CHANNEL JFET.*

**- Results:**

*I. CHARACTERESTICS OF AN N-CHANNEL JFET.*

Table (1): characteristics of an n-channel JFET

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **ID (mA) for VDS = (v)** | | | | | | |
| **VGS (v)** | **0** | **0.5** | **1** | **2** | **5** | **10** | **15** |
| **0** | 0.0232 | 3.24 | 5.75 | 9.36 | 12.26 | 12.46 | 12.28 |
| **-0.5** | 0.0241 | 2.91 | 5.33 | 8.03 | 9.86 | 9.98 | 9.98 |
| **-1.0** | 0.0224 | 1.656 | 4.04 | 6.28 | 7.59 | 7.80 | 7.81 |
| **-1.5** | 0.0226 | 1.477 | 3.4 | 4.8 | 5.6 | 5.81 | 5.87 |
| **-2.0** | 0.0218 | 1.51 | 2.46 | 3.3 | 3.7 | 3.88 | 3.94 |
| **-2.5** | 0.0213 | 0.914 | 1.53 | 1.916 | 2.19 | 2.33 | 2.39 |

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*II. A JFET AMPLIFIER.*

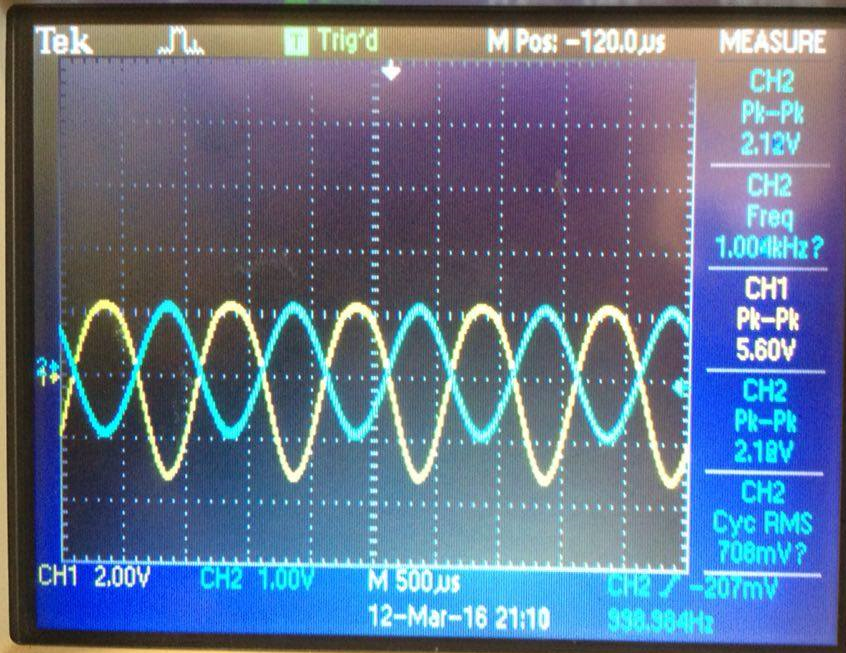
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Photo (1): output signal in oscilloscope when R unknown in fig ( ) is zero

Vo p-p = 5.6 v

A = Vo /Vin = 5.6/2 = 2.8

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Photo (2): output signal in oscilloscope when R unknown in fig ( ) increase to a value that make output about half its original size (R = 2 Ω)

*III. COMMON DRAIN AMPLIFIER.*

(VS) DC = 3.452 v (VG) DC = 1.337 v

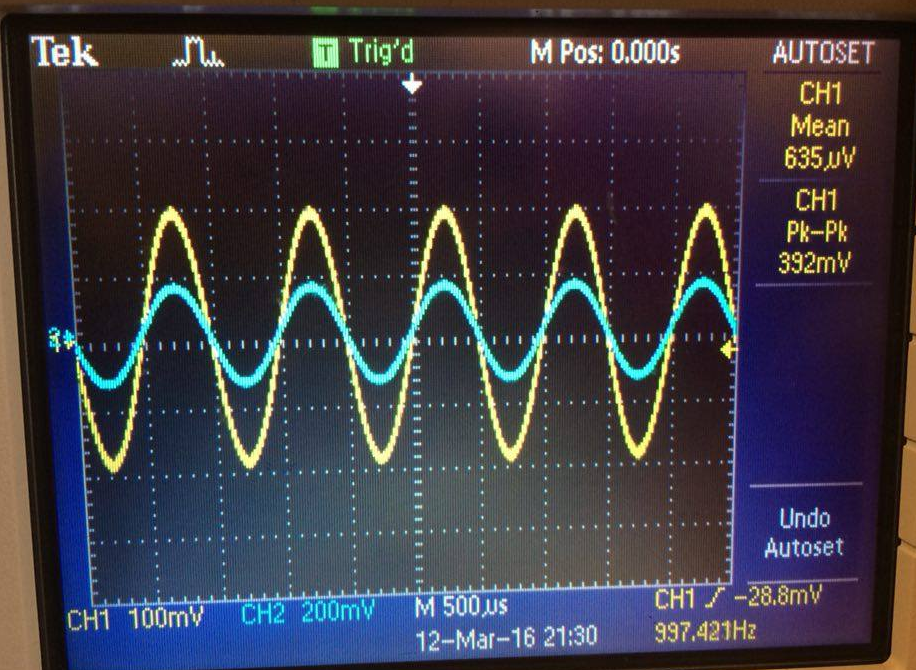


Photo (3): output signal in oscilloscope when input signal in fig () is 0.4v peak-peak

Vo p-p = 392 mv in phase

Vin = 131 mv Vout =113 mv

Iin  = 6.2 Iout = 101.3

Since Z =V/ I Zin = 21.129 KΩ Zout = 1.1155 KΩ

IV. CONSTANT CURRENT SOURCE.

Table (2): constant current source

|  |  |  |
| --- | --- | --- |
| **RL (kΩ)** | **VR (v)** | **ID (mA)** |
| **0.1** | 1.208 |  |
| **0.22** | 3.966 |  |
| **0.33** | 5.3 |  |
| **0.47** | 6.971 |  |
| **0.56** | 8.044 |  |
| **1** | 12.033 |  |
| **1.5** | 13.178 |  |
| **2** | 13.799 |  |
| **3** | 14.212 |  |

**- Discussion of Results:**

**- Conclusion:**

**- Appendix:**

**- References :**

* Faculty of Engineering, electronics Laboratory, Birzeit University, Birzeit, 2016
* [**https://www.google.ps/webhp?sourceid=chrome-instant&ion=1&espv=2&ie=UTF-8#q=fet%20experiment%20pdf**](https://www.google.ps/webhp?sourceid=chrome-instant&ion=1&espv=2&ie=UTF-8#q=fet%20experiment%20pdf)