

**Electrical & Computer Engineering Department**

**ENEE3102**

**Electronics Lab**

**Report for Experiment 5**

**The Field-Effect Transistor**

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**Abstract**

**The aim of the experiment**

The aim of this experiment to get understand the difference between the bipolar and field effect transistor.And basically to study the characteristics of N-channel JFET when using as a common source and common drain .

**Methods used**

This experiment was done using the following :

• Some components including: JFET transistor ,resistors and capacitors .

• Some devices (equipments) : oscilloscope , DVM and power supplies (AC and DC).

**Theory**

The field effect transistor is a three terminal device .The three terminals are Drain (D), Source (S) and Gate (G).There are two types of JFET which are ( N-channel JFET) and (P- channel JFET) and their symbols are shown in fig(1).

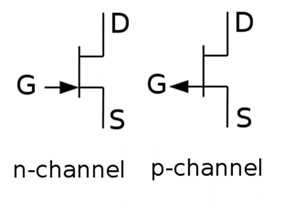


Figure 1:JFET symbols

A schematic representation of an n channel JFET is shown in Fig(2). An n-type channel is formed between two p-type layers which are connected to the gate. Majority carrier electrons flow from the source and exit the drain, forming the drain current. The pn junction is reverse biased during normal operation, and this widens the depletion layers which extend into the n channel only (since the doping of the p regions is much larger than that of the n channel). As the depletion layers widen, the channel narrows, restricting current flow.

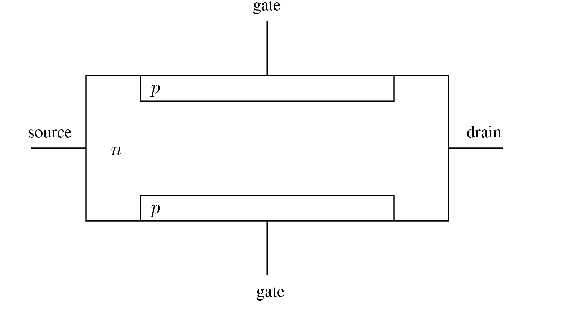


Figure :JFET n channel structure

In this experiment we will obtain output characteristics of N-channel FET as we show in fig (3), reverse biasing the gate to source junction cause the formation of depletion region, the drain has the proper polarity with respect to the source to establish the drain current I DS, the value of I DS depends on the width of the channel, the width of the channel is controlled by reverse biasing the pn junction between gate and source. If the channel width increases IDS increase. And the voltage causes the depletion region to touch close the channel is called pinch off voltage .

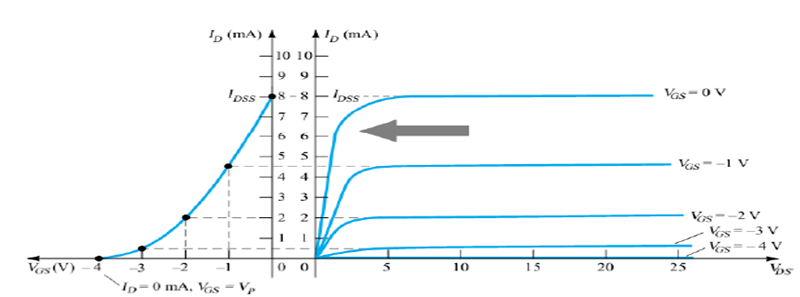
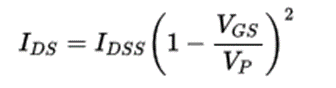


Figure :characteristic curves of JFET

As show in fig (3) ,different regions represented ohmic region, pinch off region and cut off region. And the VGS (t) can be shown.

In saturation region The drain current in the saturation region is often approximated in terms of gate bias as:



Where IDSS is the saturation current at zero gate–source voltage, i.e. the maximum current which can flow through the FET from drain to source at any (permissible) drain-to-source voltage .

In the pinch off region for n-channel:

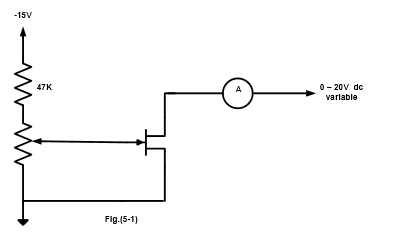
VP < VGS (t) ≤0

|VDS|>|Vp|- |VGS |

FETs have some advantages like high input impedance (100 μΩ ), fewer steps in manufacturing and more devices can be package into smaller area for integrated circuit IC , however it have some disadvantages such as low values of voltage gain and poor high frequency performance .

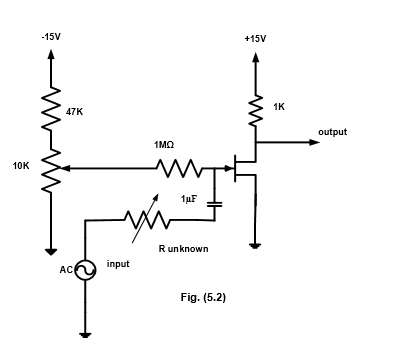
**Procedure**

1. **Characterestics of an N-CHANNEL JFET**



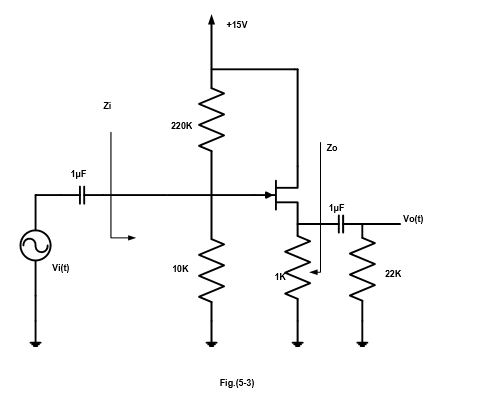
First, the following circuit was connected . Second , the potentiometer and the variable dc voltage were turned to zero(fully-anti clockwise). Then,the power supply was switched on. After that,VDS was set to zero and ID was recorded.Finally,the previous step was repeated for many values of of VDS .

1. **A JFET Amplifier**



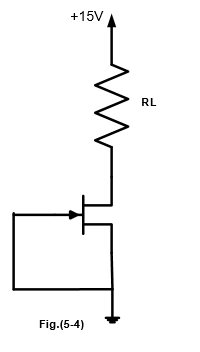
First ,the shown Circuit in fig was connected .Then the sine wave generator was set to 1 KHz and its output amplitude turned to zero.After that,the potentiometer was set to give a value of +10 v for VDS and R unknown to zero. Then,an input was applied to 2 volts peak to peak from the generator and then the output was observed on the oscilloscope and the output voltage was measured.

1. **Common drain amplifier**



First ,the Circuit shown above was connected .Then, the sine wave generator was set to 1 KHz and its output amplitude was turned to zero(here there is no input signal to the circuit).The DC voltages of VG and VS were measured.After that,an signal input of 2 volts peak to peak was applied from the generator and then the output was observed on the oscilloscope. finally the input and output impedances were measured.

1. **CONSTANT CURRENT SOURCE.**

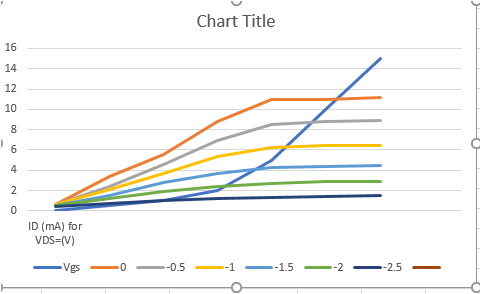


The circuit shown was connected , the ID was measured and VRL was calculated for each value of the resistor .Then the resultS was recorded in a table .

**Data & Calculations & Results**

1. CHARACTERESTICS OF AN N-CHANNEL JFET

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **ID (mA) for VDS=(V)** | | | | | | |
| **Vgs** | **0** | **0.5** | **1** | **2** | **5** | **10** | **15** |
| **0** | 0.600 | 3.400 | 5.530 | 8.782 | 10.990 | 11.000 | 11.200 |
| **-0.5** | 0.656 | 2.452 | 4.600 | 6.935 | 8.540 | 8.780 | 8.870 |
| **-1.0** | 0.632 | 2.090 | 3.670 | 5.311 | 6.220 | 6.430 | 6.450 |
| **-1.5** | 0.574 | 1.560 | 2.770 | 3.720 | 4.230 | 4.420 | 4.500 |
| **-2.0** | 0.516 | 1.200 | 1.940 | 2.430 | 2.730 | 2.870 | 2.940 |
| **-2.5** | 0.409 | 0.702 | 1.013 | 1.181 | 1.338 | 1.435 | 1.492 |



Questions :

1)when vds =5,10,15.

2)yes ,but for vgs equal -1.5 and below.

3)yes but it is too small almost zero

1. A JFET AMPLIFIER

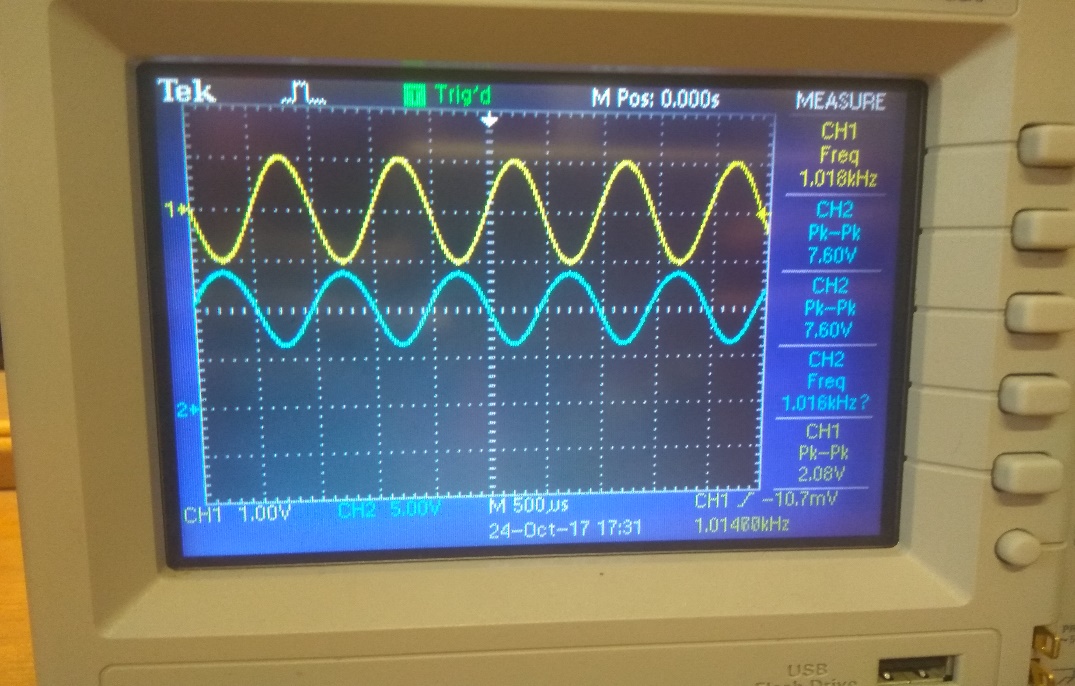


Photo (1): output signal in oscilloscope when R unknown is zero

Vin p-p = 2 volts

Vo p-p = 7.6 volts

A = Vo /Vin = 7.6/2 = 3.8

Question :

NO, since the input impedance should be very large ,to neglect the effect of R unknown

1. COMMON DRAIN AMPLIFIER.

(VS) DC = 2.64 v

(VG) DC = 0.64 v

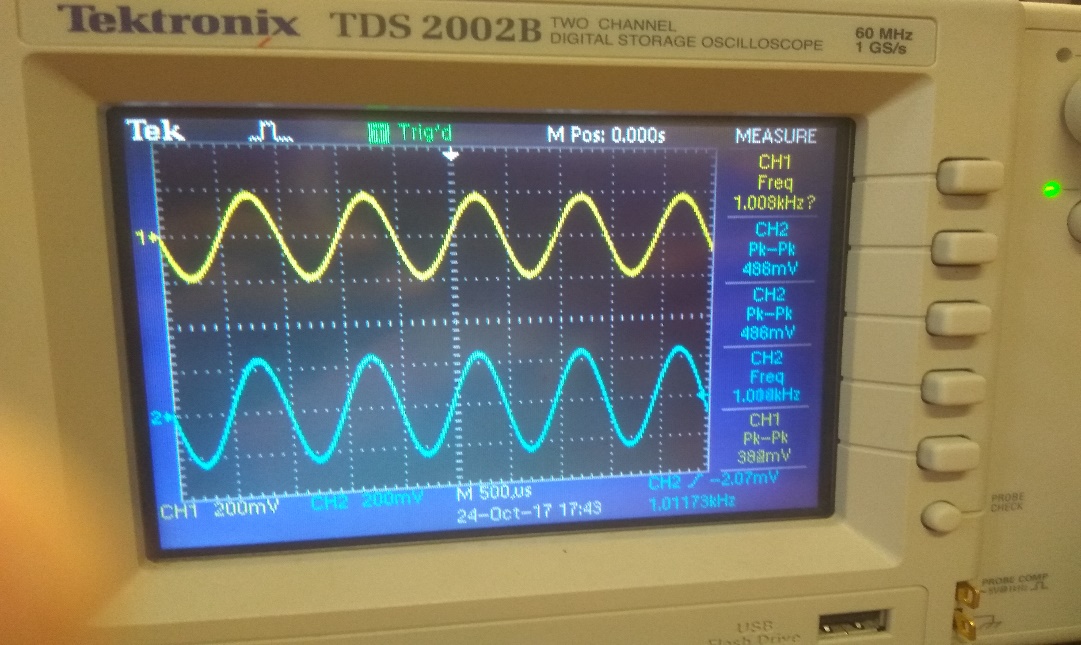


Photo (2): output signal in oscilloscope when input signal in is 0.4v peak-peak

Vo p-p = 469 mv in phase

Vin=168 mv

Iin=16.92 uA

Zin=Vin/Iin=9.92k

Vo=90mv

Io=142.5 uA

Zo=Vo/Io=0.631k

Question :

It is nearly the same value .

1. CONSTANT CURRENT SOURCE.

|  |  |  |
| --- | --- | --- |
| RL(K-Ohms) | ID(mA) | VL(V) |
| 0.1 | 11.30 | 1.13 |
| 0.22 | 11.30 | 2.49 |
| 0.33 | 11.23 | 3.71 |
| 0.47 | 11.23 | 5.28 |
| 0.56 | 11.22 | 6.28 |
| 1 | 10.80 | 10.80 |
| 1.5 | 8.70 | 13.05 |
| 2 | 6.90 | 13.80 |
| 3 | 4.78 | 14.34 |

Questions :

1)RL,max=1 k

2)Theoretical and practical values are the same.

**Conclusion**

To conclude ,in this experiment the characteristic of a JFET is studied in part one which is nonlinear .Then the output curve is plotted to show the relation between ID and VDS for some values of input gate-source voltage (Vgs).In the second part the JFET is used as an amplifier ,the voltage gain is calculated .Input and output voltages are observed on oscilloscope.In the third part ,the JFET is recognized as a common drain amplifier ,then we showed that the input impedance is greater than the output impedance .In the last part, the current decreased while increasing the value of load resistor .

By comparing the theoretical and experimental values ,they are nearly closed to each other .It is still an experiment that might include some errors due to many factors including the devices accuracy and the humane non-perfection that couldn’t be a 100% eliminated ,but we can decrease them by checking the vadility of devices and elements used .