

**Electrical & Computer Engineering Department**

**ENEE3102**

**Electronics Lab**

**Report for Experiment: The Field-Effect Transistor**

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Abstract

# The aim of the experiment

We want to know what is the characteristics of Junction field effect transistor (N-channel) when using as a common source and common drain. And also to know the difference between the BJT and FET.

# Theory

FET has three terminals Drain, Source and Gate that uses an electric field to control the current through the device. It has large input impedance that is useful in many circuits constructed from discrete components.

JFET have two types:

1) N-channel

2) P- channel

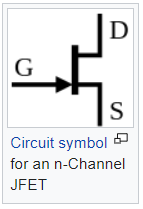
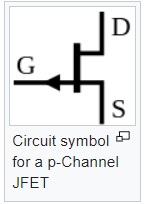
 

Figure 1 Figure 2

The N-channel JFET consists of a silicon bar of N-type semiconductor with two P type regions on both sides. JFET biasing requires that the pn junctions are reverse-biased. In order to have a current flowing through the channel.

The JFET electric characteristics curves are similar to the bipolar transistor curves. However, the JFET devices are controlled by a voltage, and bipolar transistors are controlled by current.

JFET has 3 main parameters:

* ID: [Current](https://electronicsarea.com/electric-current/) flowing from drain to source
* VGS: Gate to Source voltage
* VDS: Drain to Source voltage

FET operates in four region:

1.**Ohmic Region**

2.**Pinch-off region**

3.**Saturation region**

4.**Breakdown region**

The JFET characteristics curves that explain the regions shown in figure 3:

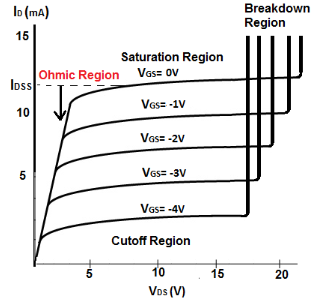
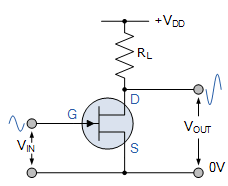


Figure 3

**Common Source Configuration**

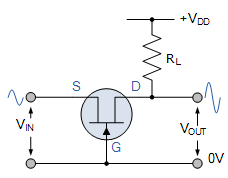
In the **Common Source**, the input is applied to the Gate and its output is taken from the Drain as shown in figure 4.



### Figure 4

### Common Gate Configuration

In the **Common Gate**, the input is applied to the Source and its output is taken from the Drain with the Gate connected directly to ground (0v) as shown in figure 5



### Figure 5

### Common Drain Configuration

In the **Common Drain**, the input is applied to the Gate and its output is taken from the Source as shown in figure 6

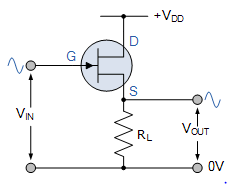


Figure 6

# Procedure and data:

1. **Characterestics of an N-CHANNEL JFET**

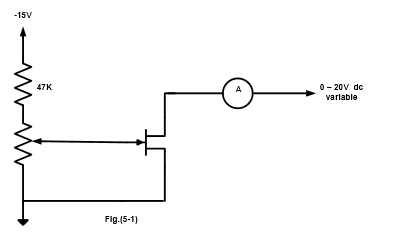


Figure 7

In the first step, The circuit was connected by us (me and the partners) that show in the figure 7. We turned the potentiometer and dc voltage to zero in the second step. After that, we switched on the power supply. In the last step we recorded Id at Vds equals zero, then we repeated this for other values of Vds which are in the table.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **ID (mA) for VDS=(V)** | | | | | | |
| **Vgs** | **0** | **0.5** | **1** | **2** | **5** | **10** | **15** |
| **0** | 0.138 | 4.0 | 5.9 | 9.4 | 12.0 | 12.3 | 12.2 |
| **-0.5** | 0.133 | 3.4 | 5.08 | 7.68 | 9.56 | 9.8 | 9.8 |
| **-1.0** | 0.129 | 2.8 | 4.2 | 6.1 | 7.25 | 7.5 | 7.68 |
| **-1.5** | 0.12 | 2.08 | 3.4 | 4.2 | 4.8 | 5.1 | 5.5 |
| **-2.0** | 0.111 | 1.67 | 2.3 | 3.14 | 3.56 | 3.75 | 4.03 |
| **-2.5** | 0.100 | 1.15 | 1.48 | 1.77 | 1.99 | 2.12 | 2.43 |

After putting vds=10 volt and VGs =-1 volt. Then we measured :

IG= 1.1  .

1. **A JFET Amplifier**

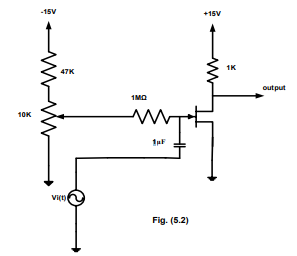
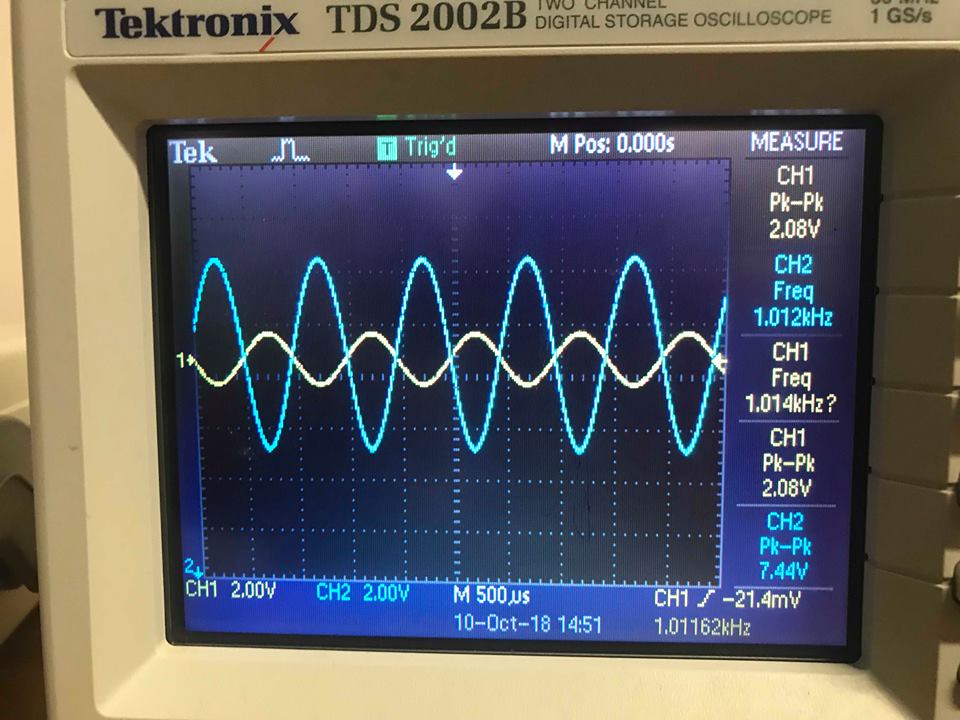


Figure 8

In the first step, The circuit was connected by us (me and the partners) that show in the figure 8. We set the sine wave generator to 1 KHz and the output was disconnected to be no signal at the input in the second step. Then we set the potentiometer for Vds to give a value of +10 in the third step. We applied from the generator the input to 2 peak – peak and we took a photo of the output on the oscilloscope. Then we measured the output voltage to know the voltage gain.



Voutput peak to peak = 7.44V

**Gain =vo/vin =3.7,** Zin=Vi/Iin=x V/A, Zout= V/A

1. **Common drain amplifier**

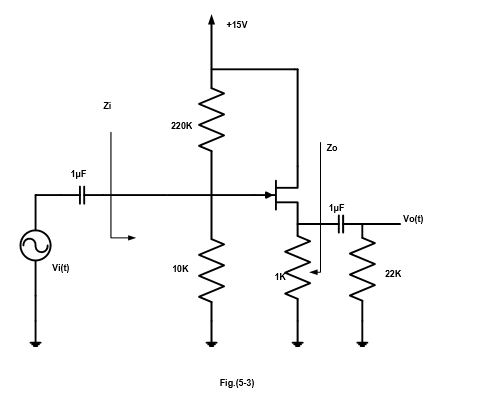
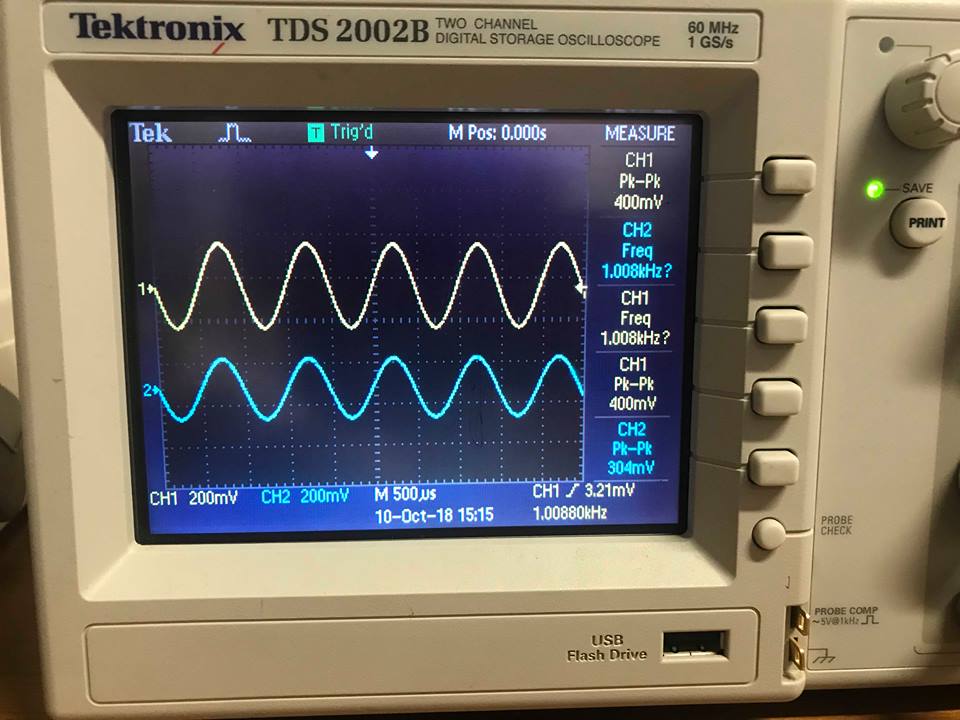


Figure 9

In the first step, The circuit was connected by us (me and the partners) that show in the figure 9. We set the sine wave generator to 1 KHz and the output was disconnected to be no signal at the input in the second step.Then we measured the DC voltages of VG and VS. We applied from the generator the input to 0.4 peak – peak and we took a photo of the output on the oscilloscope. In the last step, we measured the input and output impedances (zin , zout).



Voutput peak to peak =304mV

Vin-RMS=140.2mV , I in -RMS =38.6 .

Vout-RMS= 140.2mV , I out -RMS =140.7µA

Gain **= 0.76 ,** Z input =3.632K , Zoutput =0.996k

1. **CONSTANT CURRENT SOURCE.**

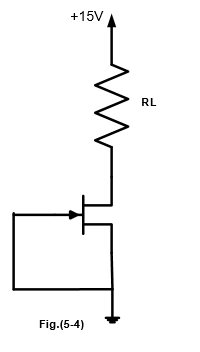


Figure 10

In the first step, the circuit was connected by us (me and the partners) that show in the figure 9. In the second step, we measured the ID and we calculated VR for each value of the resistor in the table. Finally, we recorded all the results in the table.

|  |  |  |
| --- | --- | --- |
| **RL(K)** | **VL(V)** | **ID(mA)** |
| **0.1** | **1.203** | **12.03** |
| **0.22** | **2.64** | **12.0** |
| **0.33** | **3.96** | **12.0** |
| **0.47** | **5.66** | **12.05** |
| **0.56** | **6.72** | **12.0** |
| **1** | **11.33** | **11.33** |
| **1.5** | **13.215** | **8.81** |
| **2** | **13.8** | **6.9** |
| **3** | **14.31** | **4.77** |

# Conclusion

The output curve at the characteristic of a JFET part appear the relation between ID and VDS for values of VGS.The JFET is used as an amplifier at the second part(JFET amplifier) .The JFET is renowned as a common drain amplifier at the third part (common drain amplifier). we showed that the input impedance(z input) is bigger than the output impedance(z output). We also noticed that the current decreased while the value of load resistor increasing, i mean direct relationship.

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