

**Faculty of Engineering & Technology**

**Electrical & Computer Engineering Department**

**ENEE 3102 – Electronics Lab**

**Experiment #5**

**The Field-Effect Transistor**

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# ***Abstract :-***

In this experiment, understood the difference between the bipolar and the effect transistor and consider the characteristics of N-channel JFET when used as a common source, common drain and constant current source. studied the gain, the input impedance, the output impedance and behaver of them .

Equipment’s List :-

1. network panel
2. short circuit ‘ wire ‘
3. DVM
4. Oscilloscope
5. DC voltage source
6. Variable DC voltage
7. Resistance
8. Capacitor
9. AC voltage source
10. variable resistance
11. JFET

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# ***Theory :-***

## **JFET transistor**

A transistor is a linear semiconductor device that controls current with the application of a lower-power electrical signal. Transistors may be roughly grouped into two major divisions: bipolar and field effect. we’ll introduce the general concept of the field effect transistor a device utilizing a small voltage to control current and then focus on one particular type: the junction field effect transistor.

The junction field effect transistor has two type :

* N-type semiconductor
* P-type semiconductor

The difference between them is that N-type is inside the current on agate, but P-type is the current outside of the gate and the composition of the construction of each of them and began to specialize in talking to N-type . The schematic of an n-channel JFET along with its circuit symbol is shown in Figure 1. From the layered structure shown by Figure 1a, it is clear that the n-channel JFET has its major portion made of n-type semiconductor. The mutually-opposite two faces of this bulk material from the source and the drain terminals. Further, it is also seen that there are two relatively-small p-regions embedded into this substrate which are internally joined together to form the gate terminal. Thus, here, the source and the drain terminals are of n-type while the gate is of p-type. Due to this, two pn junctions will be formed within the device, whose analysis reveals the mode in which the JFET works. Further the circuit symbol shown by Figure 1b has an arrow pointing towards the device at its Gate terminal which indicates the direction in which the current would flow, provided the pn junction is forward biased. ………………….[2 ]



 Figure ..... N-channel JFET (a) layered structure (b) circuit symbol……………(2 )

**The characteristics curve** of an N channel JFET transistor shown below is the the graph of the drain current, ID versus the gate-source voltage,it is represents the gain of the transistor.

 

 Figure .... the characteristics curve of N-channel JFET transistor……(2 )

When no voltage is applied to the transistor VDS = 0 and VGS = 0 so will no current flows through it IDS = 0 , but when add a voltage ( the positive side at the drain and the negative at the source so VDS = +Ve and VGS = 0 . at this instant , start the current flow to drain then to source as you noted when VDS is increase the current flowing through the device at initial state which can be termed to be JFET‘s **Ohmic region**. However when add voltage at the gate ( the negative side ) VGS = -Ve and VGS = +Ve . in this case , the device behaves the same when VGS = 0 , but for lower value of VDS

As you notice when VDS gets to VP the device becomes in a saturation level and when the VGS = - VP , the device has no voltage at the drain side and no current flow in the device .

Note :-

**Saturation Region:** This is the region where the JFET transistor is fully operation and maximum current, for the voltage, VGS, that is supplied is flowing. During this region, the JFET is On and active

## **Transistor amplifier**

Transistor amplifier circuits such as the common emitter amplifier are made using Bipolar Transistors, but small signal amplifiers can also be made using Field Effect Transistors. These devices have the advantage over bipolar transistors of having an extremely high input impedance along with a low noise output making them ideal for use in amplifier circuits that have very small input signals…………..[ 3]

## **JFET Common-Drain Amplifier**

The common drain JFET amplifier is shown figure below. The configuration , which is sometimes known as source follower , characterized by a voltage gain of less than unity , and features a large current as a result of having a very large input impedance and a small output impedance …..[4 ]

 

 Figure ......JFET common-drain amplifier .....(4 )

The Equations for JFET common- drain amplifier :-

VOut = Vin  - Vgs  ………………………(1)

VOut = Vin  - VT – $\sqrt{\frac{I\_{bias}}{\frac{µ\_{n}\*C\_{ox}\*W }{2L}}}$ ………….(2)

VT = f ( VBS) …………………………..(3)

AV = $\frac{g\_{m}\*R\_{s}}{g\_{m}\*R\_{s}+1}$……………………………(4)

## **Constant current source**

The combination of low associated operating voltage and high output impedance makes the FET attractive as a constant-current source. An adjustable-current source may be built with a FET, a variable resistor, and a small battery. For optimum thermal stability, the FET should be biased near the zero temperature coefficient point. Whenever the FET is operated in the current saturated region, its output conductance is very low. This occurs whenever the drain-source voltage VDS is at least 50% greater than the cut-off voltage VGS(off). The FET may be biased to operate as a constant-current source at any cur- rent below its saturation current IDSS………[5 ]

# ***Procedure :-***

**I.CHARACTERESTICS OF AN N-CHANNEL JFET.**

The circuit below was connected.

 

 Figure ...... N-channel JFET

The potentiometer was set to anticlockwise and the variable dc source to zero then put VDS by values in the table.1 and recorded the values of IDS  for each value of VGS . repeated all steps for all the value of VDS in the table.1 . then VDS was set 10V and VGS was set -1V then recorded IG .

***II.* A JFET AMPLIFIER.**

The circuit below was connected.

 

 Figure ...... A JFET amplifier

The sign wave generator frequency was set to 1KHz and the amplitude was set to zero. In addition, the potentiometer was set so that VDS = 10V and R unknown was set to zero. Then 2VP-P from the generator was applied and the output was observed on the oscilloscope. Afterwards, the peak to peak output voltage was recorded then the ac input current and voltage was recorded using DMM.

***III.* COMMON DRAIN AMPLIFIER.**

The circuit below was connected.

 

 Figure ..... common-drain JFET amplifier

The sign wave generator frequency was set to 1KHz and the amplitude was set to zero. In addition, the DC voltages of VG and VS was recorded. Then 0.4VP-P from the generator was applied and the output was observed on the oscilloscope. Afterwards, the input voltage, input current, output voltage, and output current were recorded.

***IIII.* CONSTANT CURRENT SOURCE.**

The circuit below was connected.

 

 Figure ..... constant current source for JFET

The values of ID  and VL  was recorded for different RL values in the table.2

# ***Data , calculation and dissociation :-***

**I.CHARACTERESTICS OF AN N-CHANNEL JFET.**

The table of N-channel JFET

 Table ...... The values of the characteristics of an N-channel JFET

|  |  |
| --- | --- |
|  | **ID( mA) for VDS=(V)** |
| **VGS(V)** | **0** | **0.5** | **1** | **2** | **5** | **10** | **15** |
| **0** | 0.14 | 3.05 | 5.23 | 8.32 | 10.4 | 10.4 | 10.6 |
| **-0.5** | 0.14 | 2.59 | 4.64 | 6.67 | 7.9 | 8.06 | 8.06 |
| **-1.0** | 0.13 | 2.2 | 3.7 | 5.12 | 5.8 | 6.06 | 6.06 |
| **-1.5** | 0.12 | 1.6 | 2.6 | 3.41 | 3.84 | 4.01 | 4.07 |
| **-2.0** | 0.12 | 1.46 | 2.2 | 2.76 | 3.11 | 3.23 | 3.36 |
| **-2.5** | 0.1 | 0.6 | 0.7 | 1.03 | 1.04 | 1.04 | 1.22 |

When VDS was set 10V and VGS to -1V so the IG = 0.01µA

Figure ....the characteristics of an N-channel JFET

The current stabilized ID when the value of VDC is 5 volts. When VGS = 0. Notice when VDS = 10 volt every time VGS increases in minus the current ID is decreased. When VDS = 10 and VGS = -1 notice that IG is very too low. When VDS gets increased by 0.5 in minus, ID gets decreased by $≅$2.

Transconductance = gm = $\frac{∆I\_{D}}{∆V\_{GS}}$ = $\frac{1.04-10.4}{-2.5-0 }$ = 3.744 $(mΩ)^{-1 }$

***II.* A JFET AMPLIFIER.**

The waveform output :-

 

 Figure .......the output voltage of JFET amplifier

The output voltage = $\frac{9}{2}$ = 4.5 V the input current = 6µA

The voltage gain = $\frac{V\_{out }}{V\_{in}}$ = $\frac{4.5}{1}$ = 2.5V the input impedance = $\frac{V\_{in}}{I\_{in }}$ = $\frac{1}{6\*10^{-6}}$ = 166KΩ

Noticed from input and output voltage, when the input is Trest the output is Trough which means that the output is the inverse of the input.

***III.* COMMON DRAIN AMPLIFIER.**

The DC voltage :-

Of VG  = 638mV

Of VS  = 1.931V

The waveform of output voltage :-

 

 Figure ...... the output voltage of common-drain JFET amplifier

The output voltage = $\frac{0.316}{2}$ = 0.158V the voltage gain = $\frac{V\_{out }}{V\_{in}}$ = $\frac{0.158}{0.2}$ = 0.79V

The phase shift between the input and output voltage $≅$ 0

The input current = 13.6µA

The output current = 78.2µA

The input impedance = $\frac{V\_{in}}{I\_{in}}$ = $\frac{0.2}{13.6\*10^{-6}}$ = 14.7KΩ

The output impedance = $\frac{V\_{out}}{I\_{out}}$ = $\frac{0.158}{78.2\*10^{-6}}$ = 2.021KΩ

* As noted from the figure the peek to peek output is higher from the peek to peek input, and the phase shift between the input and output is almost zero. The theoretical v:
$\rightarrow \rightarrow $Vin = 800mV, Vo = 600mV $\rightarrow \rightarrow $ Av = 0.75
the theoretical and practical gain were almost the same with the theoretical one (0.75) and the practical one (0.79).

***IIII.* CONSTANT CURRENT SOURCE.**

The table of constant current source :-

 Table .... the table have the values of VL & ID

|  |  |  |
| --- | --- | --- |
| **RL(KΩ)** | **VL(V)** | **ID(mA)** |
| **0.1** | 10.91 | 1.07 |
| **0.22** | 10.8 | 2.3 |
| **0.33** | 10.8 | 3.5 |
| **0.47** | 10.8 | 5.06 |
| **0.56** | 10.83 | 6.03 |
| **1** | 10.43 | 10.4 |
| **1.5** | 5.54 | 13.7 |
| **2** | 4.69 | 14 |
| **3** | 3.57 | 14.2 |

As noticed from the table above when the variable resistor value is in tenths, the current (ID) was almost constant and the voltage around the resistor increases when increasing the resistance around 1 volt. When the variable resistor became greater than 1 the current decreases and the voltage increases slowly. The resistance greatest value is 1 kohm when it generates a constant current which is equal to the voltage around the resistor. As noticed from the theoretical and measured values its almost the same and when the theoretical gets applied on the second equation = VL = RL \* ID so the VL theoretical is almost the same VL measured.

# ***Conclusion :-***

The results generated is this experiment was close to the theoretical as expected and the measurements are acceptable and similar to the theoretical, but a small problem happened in the last branch of the experiment, as noticed in the datasheet RL at these values VL values and ID values after 1, from 1.5 to 3 is flipped, but in the data in this report it is corrected. The graphs in the first branch and the waveform of the output in the second and third branches is acceptable. In the experiment, the carless use of the instruments led to the damage of two transistors. The results can be improved by using a lot more accurate instruments and be precise by taking measurements and reading them and be more carful using the instruments. The experiment was useful.

# ***References:-***

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