**Faculty of Engineering and Technology**

**ENEE3102, Electronics Lab.**

**Experiment #6 Report**

**Multistage Amplifiers and Frequency Response**

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**Abstract:**

The purpose of this experiment is to study and design multistage amplifiers, the effect of frequency on the gain of an amplifier and the deferential amplifier and its functions.

**Theory:**

An average gain of a voltage amplifier is around 100 which is ok in some applications but not all. When a much higher gain is needed then multistage amplification must be used. Amplifiers are connected in cascade in multistage amplifiers; meaning that the output of one stage is the input of the next stage, this will result in theory in a gain equal to the multiplication of all the gains of the separate stages. Connecting amplifiers in cascade can be achieved using three methods: 1) capacitive coupling 2) transformer coupling 3) direct coupling. The first and second methods block DC currents completely which is very good but their downside is that they use energy storage devices (capacitors and inductors) which are relatively large and can’t be manufactured into ICs easily.

The general circuit of a two stage BJT type amplifier can be seen in figure 1.



Figure 1 : Two stage amplifier

When designing a multistage amplifier one must first design the dc biasing of each stage alone, then design the ac small signal circuit for the whole multistage amplifier.

DC analysis using voltage divider biasing:



Let VE = VCC/10 and RE = VE/IE



AC analysis:



**Frequency response:**

The gain of an amplifier varies with the frequency of the input voltage. The gain is highly attenuated at low and high frequencies as it can be seen in figure 2. At medium frequencies the gain is constant. Attenuation of the gain at low frequencies is due to bypass capacitors found in the amplifier circuit. Attenuation at high frequencies is due to inner capacitances in the transistor itself between the different layers of the doped semiconductor material.



Figure 2 : Frequency response of an amplifier

**Differential Amplifiers:**

A differential amplifier amplifies the difference between its two input signals. Usually the two parts of the differential amplifier are identical resulting in a zero output when the two input signals are equal. See figure 3.



Figure 3 : Differential amplifier

**Procedure and results:**

**I.MULTISTAGE AMPLIFIER DESIGN:**

A multistage amplifier with a gain of 200 was analyzed. With a first stage gain of 100 and a second stage gain of 2.

The following circuit was given to be analyzed:



Figure 4 : The given multistage amplifier

First the dc analysis of the first stage was done. The following measurements were taken: Vc1=4.87 V , Vb1=2.97 V , Ve1=2.32 V

Afterwards the two stages were separated and the ac analysis of the first part was done by feeding the first stage with an 18.0m Vp-p sinewave input with 1KHz frequency. The output was Vo1=2.24 Vp-p. Thus the first stage has a gain of Av1=-124.4.



Figure 5 : First stage input (CH1) and output (CH2)

Next the dc analysis of the second stage was done. The following measurements were taken: Vc2=6.54 V , Vb2=2.25 V , Ve2=1.6 V

Then the second stage was fed with a 1.25 Vp-p sinewave input with 1KHz frequency. The output of the second stage was Vo2=2.56 Vp-p. Thus the voltage gain of the second stage is Av2=-2.048



Figure 6 : second stage input (CH1) and output (CH2)

Now the two stages were connected together again in cascade. The DC voltages were measured again: Vc1=5.07 V , Vb1=2.86 V , Ve1=2.22 V , Vc2=6.45 V , Vb2=2.3 V , Ve2=1.89 V

A sinewave input of 16m Vp-p was fed to the input with 1KHz frequency. The output was Vo=3.84 Vp-p. The voltage gain Av=234.14. Which is less than the theoretical total gain ((-124.4)\*(-2) = 248.8) which is expected due to losses in the circuit.



Figure 7 : amplifier input (CH1) and output (CH2)

-If the coupling capacitor didn’t have a negligible impedance at the source frequency then the voltage gain would drop drastically due to a voltage drop across the capacitor.

**II.FREQUENCY RESPONSE:**

For the same circuit in part one the frequency is changed from 10 Hz to 2MHz and the gain is calculated.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Frequency(Hz)** | **Vin(Vrms)** | **Vout(Vrms)** | **Av** | **Log(f)** | **20\*log(Av)** |
| **10** | **24m** | **0.55** | **22.9** | **1** | **27.196** |
| **100** | **24m** | **3.36** | **140** | **2** | **42.922** |
| **200** | **24m** | **4.8** | **200** | **2.3** | **46** |
| **300** | **24m** | **5.32** | **221.6** | **2.477** | **46.91** |
| **400** | **24m** | **5.52** | **230** | **2.6** | **47.23** |
| **500** | **24m** | **5.64** | **235** | **2.69** | **47.42** |
| **1k** | **24m** | **5.84** | **243.3** | **3** | **47.723** |
| **10k** | **24m** | **6.08** | **253.3** | **4** | **48.07** |
| **30k** | **24m** | **6.08** | **253.3** | **4.477** | **48.07** |
| **100k** | **24m** | **6** | **250** | **5** | **47.96** |
| **300k** | **24m** | **5.88** | **245** | **5.477** | **47.78** |
| **400k** | **24m** | **5.72** | **238.3** | **5.6** | **47.54** |
| **500k** | **24m** | **5.6** | **233.3** | **5.69** | **47.36** |
| **1M** | **24m** | **4.64** | **193.3** | **6** | **45.72** |
| **2M** | **24m** | **3.5** | **145.8** | **6.3** | **43.27** |

The plot of the gain in decibels vs log(f) can be seen in figure 8.



Figure : Frequency Response Curve

-The output amplitude depends on the frequency. At low frequencies the output amplitude is amplified by a small amount. Bypass and coupling capacitors cause this attenuation in the gain of the amplifier. At high frequencies similar effects happen to the gain as it gets attenuated. The gain is constant between 300 Hz and 489778.8 Hz. The maximum gain is 48 dB, 0.707 of that is 45 dB. This gain happens at two frequencies: 177.8 Hz and 1258925.4 Hz, these frequencies are pointed at with an arrow in figure 8. The difference between them is 1258747.6 Hz.

**III.DIFFERENTIAL AMPLIFIER:**

The circuit shown in Fig. (5.2) was connected. Using the potentiometer and the variable dc source one can set V1=V2 and measure the output voltage.



|  |  |
| --- | --- |
| **V1=V2(V)** | **Vout(V)** |
| **0** | **7.79** |
| **1** | **7.436** |
| **2** | **6.936** |
| **3** | **6.3** |
| **4** | **5.768** |
| **4.61** | **5.46** |



Figure : Common mode gain

The graph in figure 9 has a slope of -0.532. This slop represents the common mode gain. The experimental value of Ac is the slope=-0.532.

Then for the same circuit as above but with V1/=V2. The input values were changed since some values in the manual were unreachable practically!

|  |  |  |
| --- | --- | --- |
| ***V1(V)*** | ***V2(V)*** | ***Vout(V)*** |
| ***0*** | ***0*** | ***7.712*** |
| ***0.03*** | ***-0.03*** | ***7.315*** |
| ***0.1*** | ***-0.1*** | ***6.27*** |
| ***0.13*** | ***-0.13*** | ***6.002*** |
| ***0.2*** | ***-0.2*** | ***5.125*** |



Figure : Differential mode gain

The slope of the graph in figure 10 represents the differential mode gain Ad. Ad=14.928.CMRR=Ad/Ac=14.928/0.532=28

**Conclusion:**

The data obtained in this experiment coincides with expected data from a theoretical point of view. Errors were found in the experiment due to incompetence in measurement or due to uncalibrated instruments, but it was negligible. Theoretical laws were confirmed such as the multiplication of the gains when cascading amplifiers and the frequency response plot.