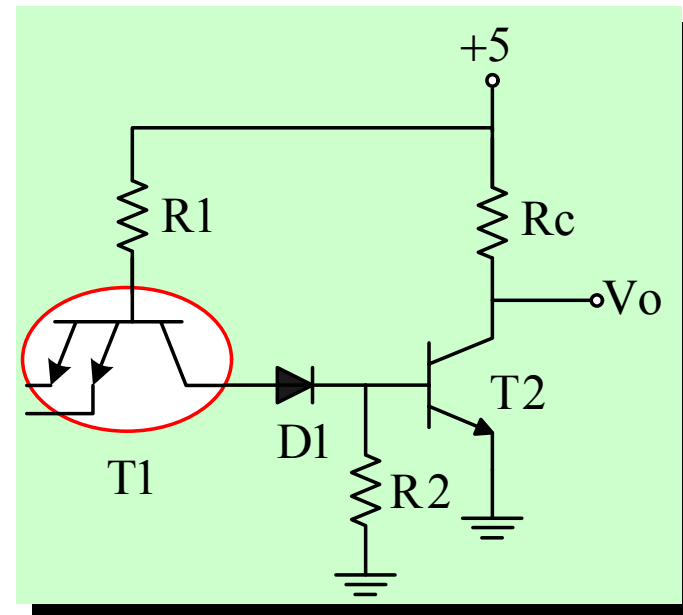


# Digital Integrated Circuit Design

## Lecture 7 – Logic Families



Adib Abrishamifar  
EE Department  
IUST

# Contents

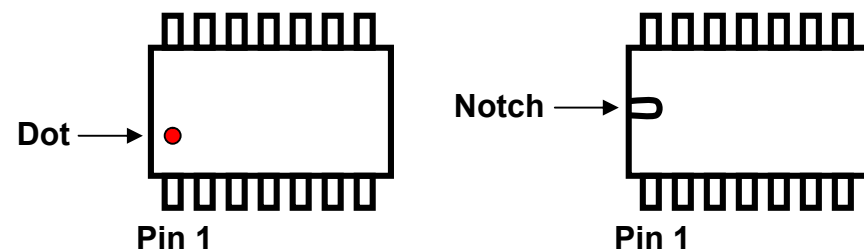
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- ▶ **Logic Families on a Glance**
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- ▶ **Compatibility of Logic Families**
- ▶ **Noise Margins of Logic Families**
- ▶ **Summary**

# Logic Families on a Glance

---

- ▶ **Based on Underlying Semiconductor Technology**
  - ▶ **Transistor-Transistor Logic: TTL**
    - Bipolar technology
    - Dual-in-line package (DIP)
    - Surface-mount technology (SMT): Smaller
  - ▶ **Metal Oxide Semiconductors: MOS**
    - Metal Oxide Semiconductor (MOS) technology
    - Very low power



# Logic Families on a Glance

---

## ▶ TTL Families

- ▶ **74**      **Standard**
- ▶ **74L**    **Low power**
- ▶ **74H**    **High speed**
- ▶ **74S**    **Schottky**
- ▶ **74LS**   **Low power Schottky**
- ▶ **74AS**   **Advanced Schottky**
- ▶ **74ALS** **Advance Low power Schottky**

# Logic Families on a Glance

---

- ▶ **Standard, 74 series** - introduced by Texas Instruments in 1964
- ▶ **Low-power, 74L series** - large resistor values reduce power dissipation
- ▶ **High-speed, 74H series** - small resistor values & Darlington pair reduce propagation delay
- ▶ **Schottky, 74S series** - Schottky barrier diode is used to reduce time delay
- ▶ **Low-power Schottky, 74LS series** - like 74S but uses larger resistor values
- ▶ **Advanced Schottky, 74AS series** - improved version of 74S
- ▶ **Advanced low-power Schottky, 74ALS** – has the lowest power-speed product

# Logic Families on a Glance

---

## ▶ CMOS Families

- ▶ 40xx/45xx      Metal-gate CMOS
- ▶ 74C            TTL-compatible CMOS
- ▶ 74HC          High speed CMOS
- ▶ 74ACT         Advanced CMOS-TTL compatible

# Logic Families on a Glance

---

- ▶ **4000/14000 series** - introduced by RCA/Motorola
- ▶ **74C series** - pin for pin and function for function compatible with TTL devices having the same number, e.g. CMOS 74C74 and TTL 7474
- ▶ **74HC series** - high speed (comparable with TTL) and higher output current
- ▶ **74HCT series** - voltage levels compatible with that of TTL devices, i.e. a TTL device can directly drive a 74HCT device
- ▶ **Compared to TTL families ; lower power dissipation and slower speed**

# Logic Families on a Glance

---

- ▶ **Advanced CMOS Logic**
  - ▶ **First-Generation Devices**
    - No output slew rate control
      - Serious noise!
  - ▶ **Second-Generation Devices**
    - Output slew rate control or TTL level output voltages
  - ▶ **Third-Generation Devices**
    - $V_{cc} : 3.3V$
    - Logic families optimized



# Logic Families on a Glance

## ▶ Advanced CMOS Logic

Logic Family	Manufactures
First Generation, 5V	
54/74 AC, ACT 54/74 AC11, ACT11 54/74FCT, FCT-A 29C800	National, Motorola, Harris Texas Instruments, Philips IDT, Cypress, Harris AMD
Second Generation, 5V	
54/74ACQ, ACTQ 54/74FCT-T, FCT-AT, FCT-CT	National IDT
Third Generation, 3.3V	
54/74LVQ 54/74FCT3 74LVC	National IDT Texas Instruments

# Logic Families on a Glance

---

- ▶ **Logic family letter designator**
  - ▶ **5V family: AC, ACT, FCT, etc**
    - With T, TTL compatible input threshold at normal TTL supply voltage levels
  - ▶ **Low-voltage: LVC, LVQ, FCT3, etc**
    - TTL compatible input threshold
- ▶ **FCT and 29C800 families**
  - ▶ **Bus interface families**
    - They are not true logic families since they don't have NANDs, NORs, etc

# Logic Families on a Glance

---

## ▶ BiCMOS Logic

### ▶ BiCMOS technology

- CMOS input structure + CMOS internal logic + Bipolar output structure
- high speed, high drive, low power

Logic family	Manufactures
54/74ABT	Texas Instruments, Philips
74BC	Motorola, Toshiba
54/74BCT	Texas Instruments
54/74LVT	Texas Instruments

# Logic Families on a Glance

## ► Simple Comparison of Logic Families

Gate / Par.	CMOS		TTL				
	74HC	4000	74	74LS	74S	74ALS	74AS
Static P.(mw/Gate)	$25 \times 10^{-6}$	$10^{-3}$	10	2	19	1	8.5
100KHz (mw/Gate)	0.17	0.1	10	2	19	1	8.5
PDT(ns)	8	50	10	10	3	4	1.5
Max Fr.(MHz)	40	12	35	40	125	70	200
S × P(Pj)	1.4	11	100	20	57	4	13
Fanout	10	4	40	20	50	20	50
Max in. Current (mA)	0.001	0.001	-1.6	-0.4	-2	-0.1	-0.5

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# Diode Logic (DL)

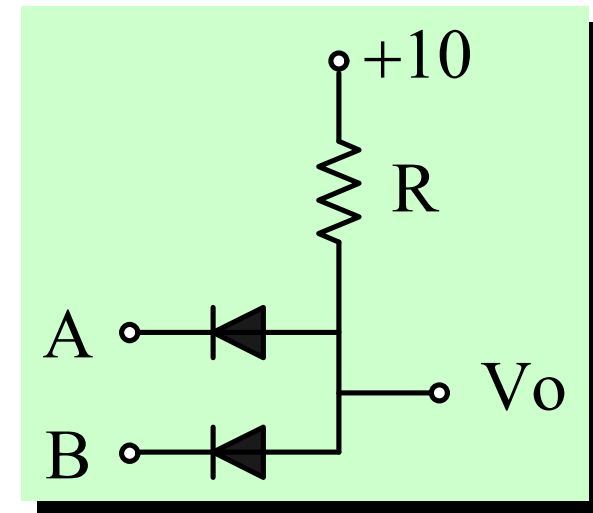
- ▶ In this lecture we assume the following parameters for a PN junction and Bipolar transistor

Parameter	Value
$V_{\gamma}$	0.7V
$V_{BEoff}$	0.5V
$V_{BEon}$	0.7V
$V_{BEsat}$	0.8V
$V_{CEsat} / \max$	0.1 / 0.2V

# DL

A	B	$V_o$
0	0	0.7
0	5	0.7
5	0	0.7
5	5	5.7

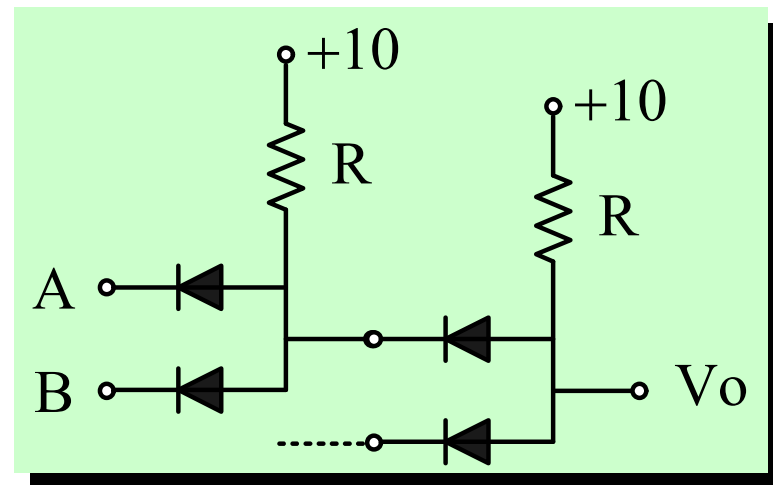
## ► AND Gate



# DL

- ▶ If we series the two equal DL sections the minimum of output voltage will be increased

$$V_{O_{\text{Min}}} = 2 \times 0.7 = 1.4$$





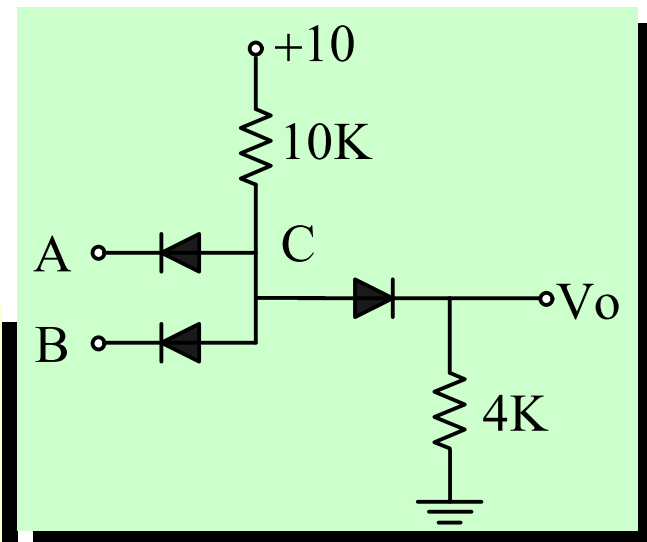
# DL

## ▶ $V_\gamma$ Canceling

$$\Rightarrow V_{O_{\text{Max}}} = \frac{10 - 0.7}{10 + 4} \times 4 = 2.66$$

$$\Rightarrow V_{C_{\text{Max}}} = 3.36$$

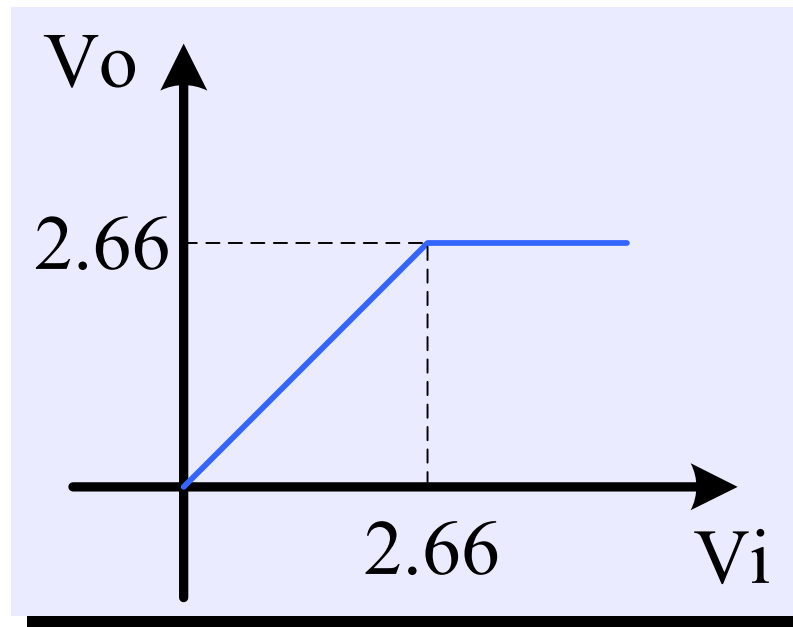
$$\Rightarrow \begin{cases} V_i \leq 2.66 \Rightarrow V_c = V_i + 0.7 \Rightarrow V_o = V_i \\ V_i \geq 2.66 \Rightarrow V_o = 2.66 \end{cases}$$



# DL

## ▶ VTC

- ▶ What is the value of  $NM=?$

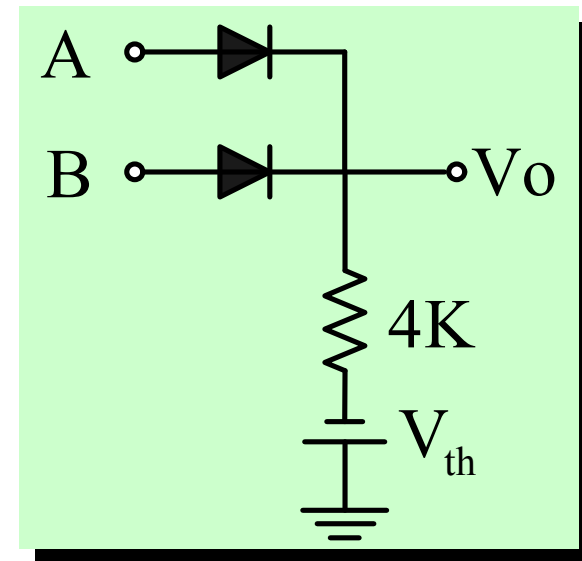


# DL

## ▶ OR Gate

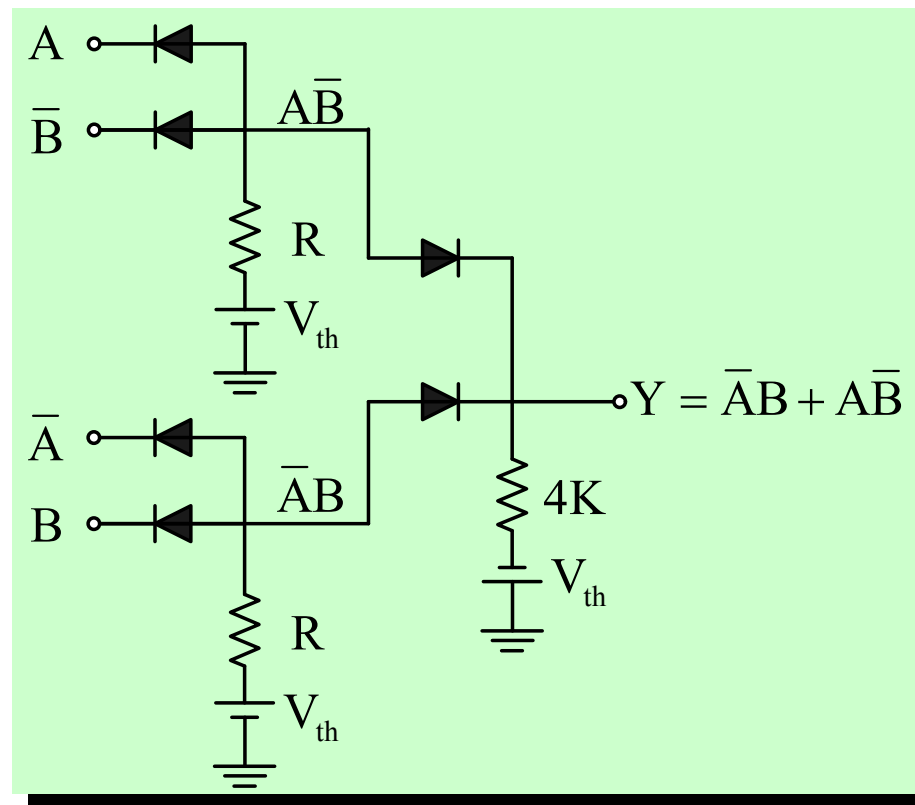
- ▶  $V_{th}$  may be selected equal to zero

A	B	$V_o$
0	0	-0.7
0	5	5-0.7
5	0	5-0.7
5	5	5-0.7



# DL

## ► XOR



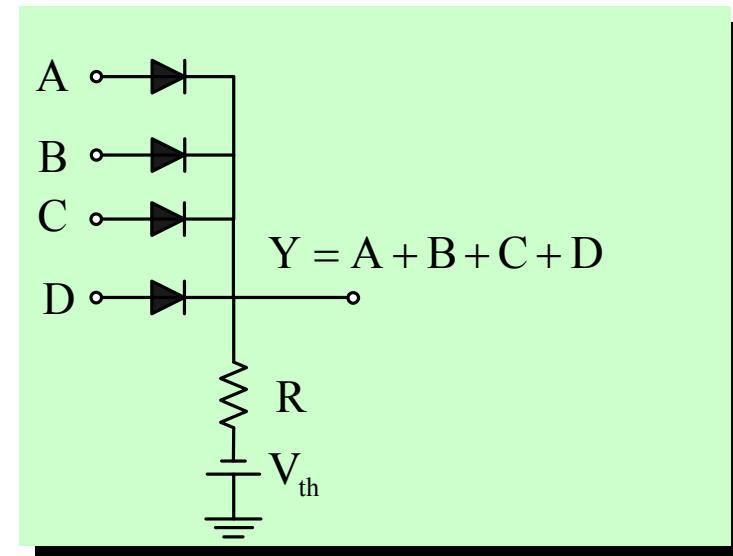
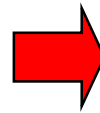
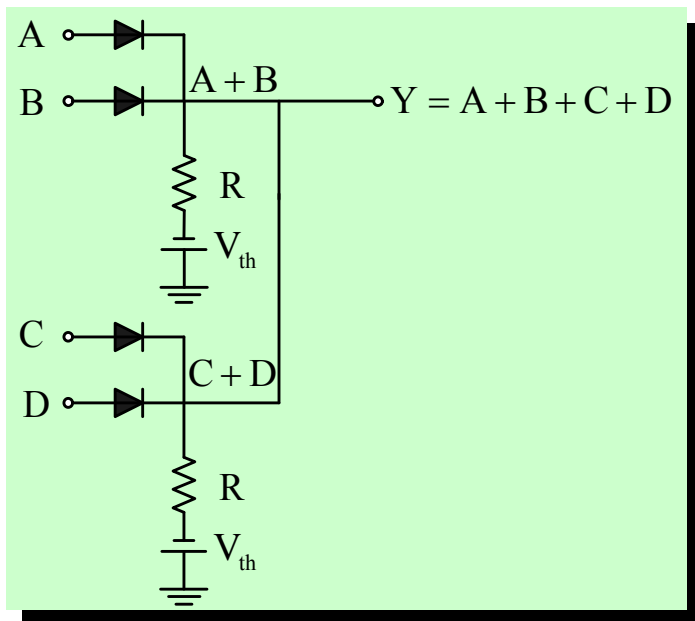
# DL

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- ▶ **Wired OR**
  - ▶ **Open (normally collector) outputs connected together to a common pull-up (or pull-down) resistor**
  - ▶ **Any collector can pull the signal line low**

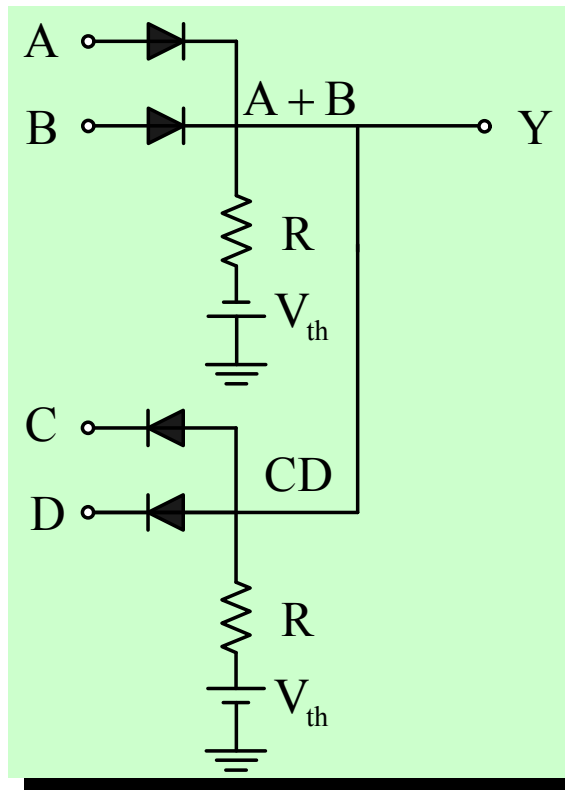
# DL

## ► Wired OR



# DL

## ► Wired AND



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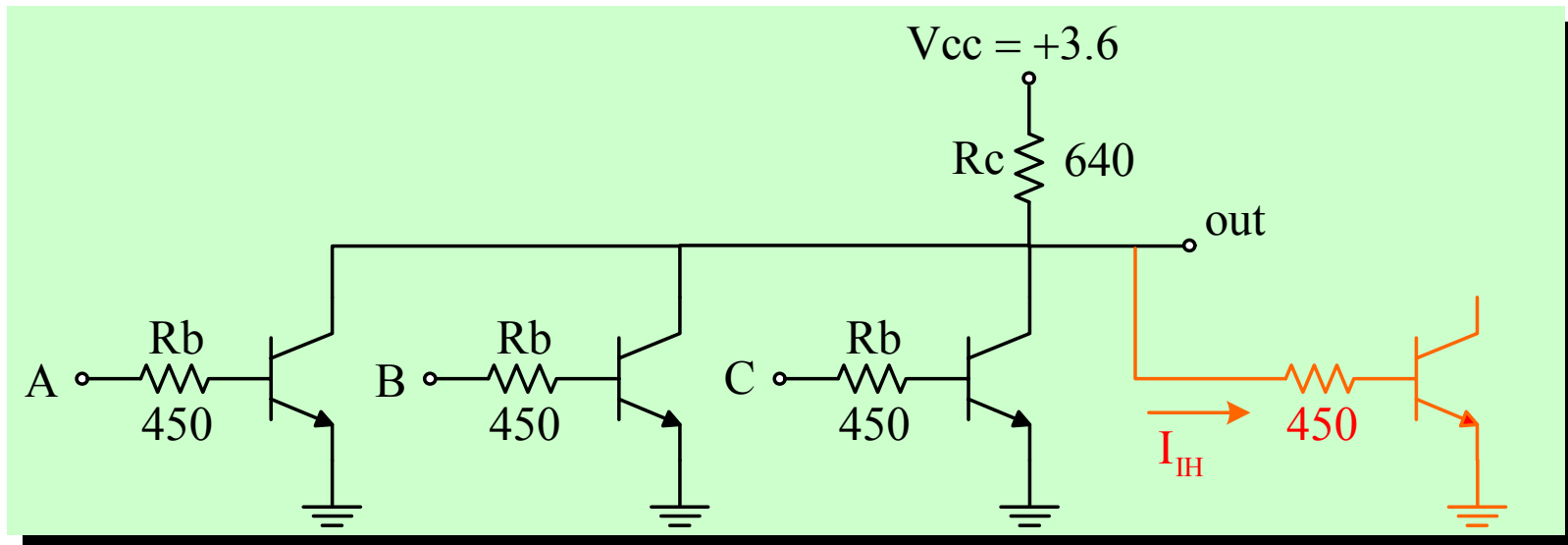
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# Resistor Transistor Logic (RTL)

- ▶ The first active Gate (NOR)



- ▶  $R_b$  for  $V_{be}$  equalization

# RTL

- ▶ It is not good for NAND Gate because the output must be only grounded when all of three transistors are activated (Thermal consideration,...)

$$I_{CS} = \frac{V_{CC} - V_{CEsat}}{R_c} = \frac{3.6 - 0.1}{640} = 5.47 \text{mA}$$

$$I_{Bsat} = \frac{I_{csat}}{\beta_{min}} = \frac{5.47}{30} = 0.182 \text{mA} \quad [10 \leq \beta_{min} \leq 50]$$

$$\Rightarrow V_{IH} = V_{BEsat} + 450^{\Omega} \times 0.182^{\text{mA}} = 0.88 \Rightarrow \underline{V_{IH}} = 0.88$$

$$V_{BEon} = 0.7 \Rightarrow \overline{V_{IL}} \approx 0.5 \quad (\text{it is not a standard but we assume})$$

$$\Rightarrow \text{NML} = \overline{V_{IL}} - \overline{V_{OL}} = 0.5 - 0.2 = 0.3$$

# RTL

- ▶ **NML is low then choose the  $V_{OH}$  for  $NMH > 0.3$**

$$NMH = \underline{V_{OH}} - \underline{V_{IH}} \Rightarrow 0.3 = \underline{V_{OH}} - 0.88 \Rightarrow \underline{V_{OH}} = 1.18V$$

- ▶ **This value is used for calculating Fan out**

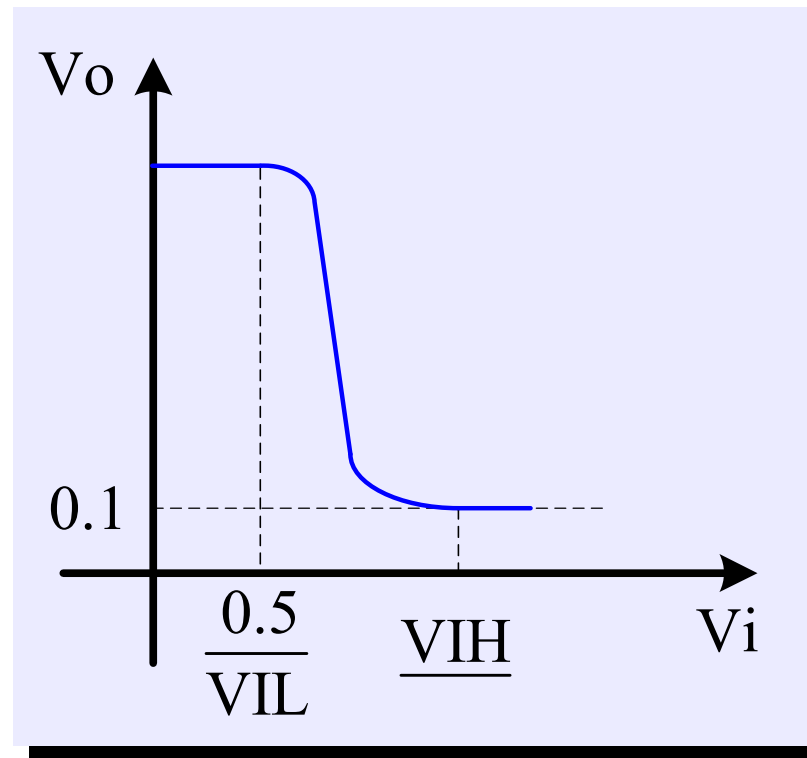
$$I_{OH} = \frac{3.6 - 1.18}{640} = 3.78mA$$

$$I_{IH} = \frac{1.18 - 0.8}{450} = 0.844mA$$

$$\Rightarrow \text{Fanout} = FO = \frac{I_{OH}}{I_{IH}} = \frac{3.78}{0.844} = 4.48 \rightarrow FO = 4$$

# RTL

## ► VTC



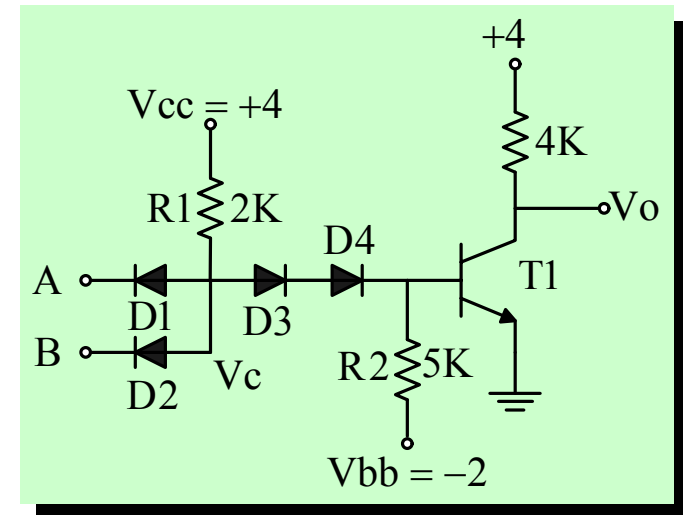
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# DTL

- ▶ **Disadvantages:**
  - ▶ Two Supplies are needed
  - ▶ One more pin is needed



NAND

- ▶ **Advantages:**
  - ▶ D3,D4 are always on  Switching and NM are good

# Diode Transistor Logic (DTL)

## ► NM

$$NML = \overline{V_{IL}} - \overline{V_{OL}}$$

$$\overline{V_{IL}} = 0.7 + 0.7 + 0.5 - 0.7 = 1.2V$$

$$\overline{V_{OL}} = 0.2 \Rightarrow NML = 1.2 - 0.2 = 1V$$

$$NMH = \overline{V_{OH}} - \underline{V_{IH}}$$

$$\overline{V_{OH}} = \underline{V_{OH}} = 4V$$

$$\underline{V_{IH}} = ?$$

$$V_c = 2 \times 0.7 + 0.8 = 2.2$$

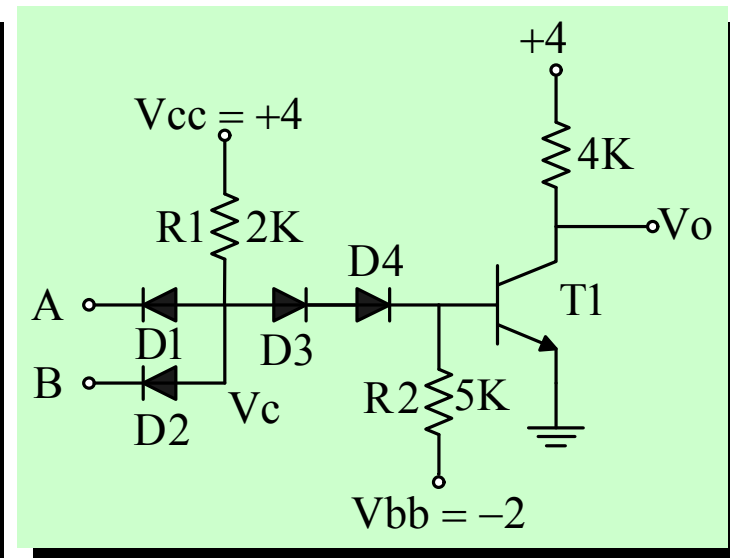
$$V_{A,B} \geq V_c - 0.7 = 1.5 = \underline{V_{IH}} \Rightarrow NMH = 4 - 1.5 = 2.5V \Rightarrow NM = 1$$

What is the min. of  $\beta$ ?

$$V_A, V_B > 1.5 \Rightarrow I_{R1} = \frac{4 - 2.2}{2K} = 0.9mA$$

$$I_{R2} = \frac{0.8 - (-2)}{5} = 0.56mA \Rightarrow I_B = 0.9 - 0.56 = 0.34mA$$

$$I_{csat} = \frac{4 - 0.1}{4} = 0.975mA \Rightarrow \beta_{min} = \frac{I_{csat}}{I_{Bsat}} = \frac{0.975}{0.34} \Rightarrow \beta_{min} = 2.9$$



NAND

# DTL

## ► Fan-Out

$$I_{IH} \approx 0 \Rightarrow FO_H = \infty$$

$FO_L$  :

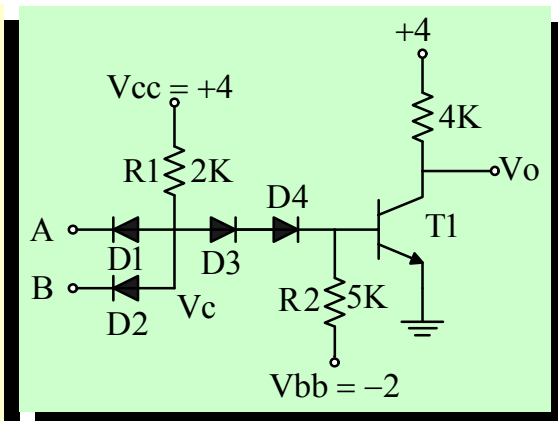
$$(V_A, V_B = 0.1) \Rightarrow I_{R1} = \frac{4 - 0.8}{2K} = 1.6mA, \quad I_{R2} = \frac{2 - 0.6}{5K} = 0.28mA$$

$$\Rightarrow I_{IL} = 1.6mA - 0.28mA = 1.32mA \text{ (out of Gate)}$$

$$I_{csat} = \beta I_{Bsat} = 30 \times 0.34^{mA} = 10.2mA$$

$$FO_L = \frac{10.2^{mA} - 0.975^{mA}}{1.32} = 7.44 \rightarrow FO_L = 7$$

$$\Rightarrow FO = 7$$



NAND



# DTL

- ▶ **P<sub>dis</sub>**
- ▶ **We have 3-state for output high (input low) and 1-state for low**

▶ **→  $P_{dis} = 3/4 P_{disL} + 1/4 P_{disH}$**

$$P_{disL} = V_{CC}I_{R1} + V_{BB}I_{R2} - V_{IL}I_{IL}$$

$$= 4 \times 1.6^{mA} + 2 \times 0.28^{mA} - 0.1 \times 1.32^{mA}$$

$$= 6.828mW$$

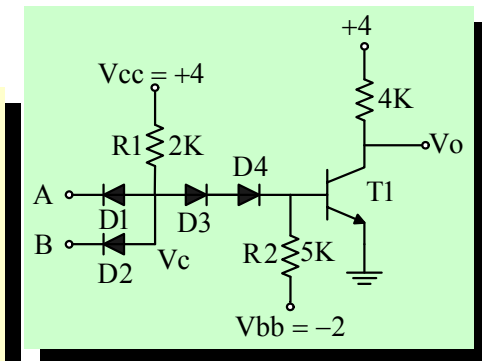
$$P_{disH} = V_{CC}(I_{R1} + I_{Rc}) + V_{BB}I_{R2}$$

$$= 4(0.975^{mA} + 0.95^{mA}) + 2 \times 0.5$$

$$= 8.8mW$$

$$\Rightarrow P_{dis} = \frac{1}{4} [3 \times 6.828 + 1 \times 8.8] = 7.321mW \rightarrow \text{Better than RTL}$$

- ▶ **V<sub>BB</sub> is needed for better switching of transistor**



NAND

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# Modified DTL (MDTL)

~~$V_{BB}$~~ , D3 → Q1

Q1, D4 = on ⇒ Q2 Charges very rapidly

In input we need the Base current ⇒ Fan-Out is increased

$V_{CC} \rightarrow +5V$

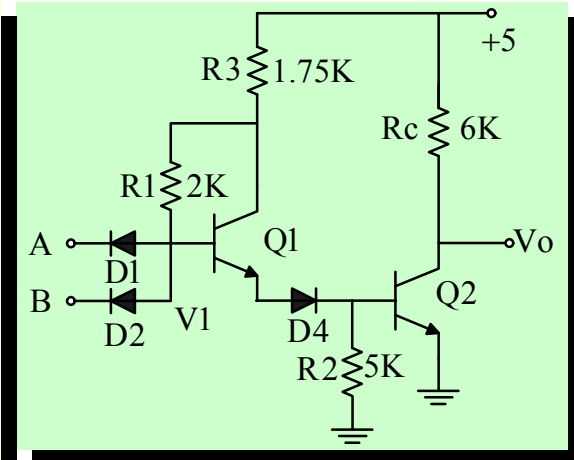
$$I_{csat} = \frac{5 - 0.1}{6K} = 0.8mA$$

Q1 is never saturated

$$V_1 = 0.7 + 0.7 + 0.8 = 2.2V \Rightarrow \underline{V_{IH}} = 2.2 - 0.7 = 1.5V$$

$$\overline{V_{IL}} = 0.5|_{Q1} + 0.7|_D + 0.5|_{Q2} - 0.7 = 1V$$

$$\overline{V_{OL}} = 0.2$$



# MDTL

$$NML = 1 - 0.2 = 0.8$$

$$V_{OH} = 5$$

$$NMH = 5 - 1.5 = 3.5 \Rightarrow NM = 0.8$$

$$V_{in} = +0.1 \Rightarrow I_{IL} = \frac{5 - 0.8}{2^K + 1.75^K} = 1.12\text{mA}$$

$$I_{BQ1} = \text{Two inputs High} = \frac{5 - 2.2}{R1 + (1 + \beta_1)R3} = \begin{cases} 25.75\mu\text{A}, & I_{B2} = (\beta_1 + 1)I_{BQ1} - \frac{0.8}{R2} \\ \beta_1 = 60 \Rightarrow I_{R3} = 1.57\text{mA} \end{cases}$$

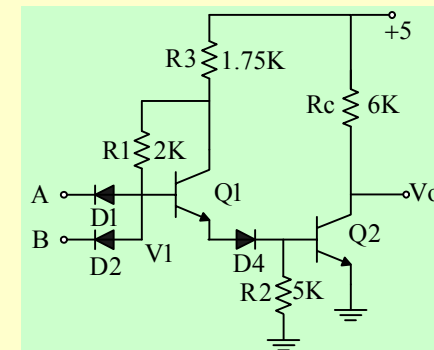
$$P_{disL} = V_{CC}I_{IL} - V_{IL}I_{IL}$$

$$= 5 \times 1.12 - 0.1 \times 1.12 = 5.488\text{mW}$$

$$P_{disH} = V_{CC}(I_{R3} + I_{Rc})$$

$$= 5(1.57 + 0.8) = 11.85\text{mW}$$

$$P_{dis} = \frac{1}{4}(3 \times 5.488 + 1 \times 11.85) \approx 7\text{mW}$$

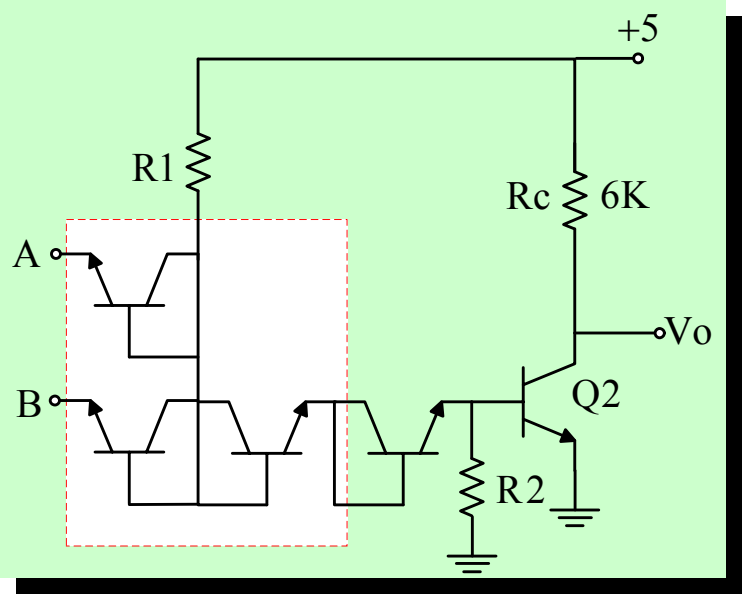


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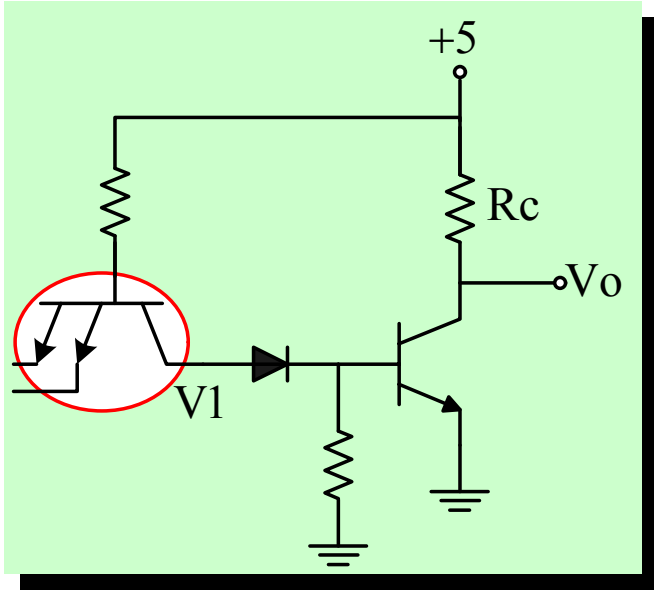
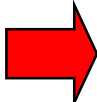
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# Transistor Transistor Logic (TTL)



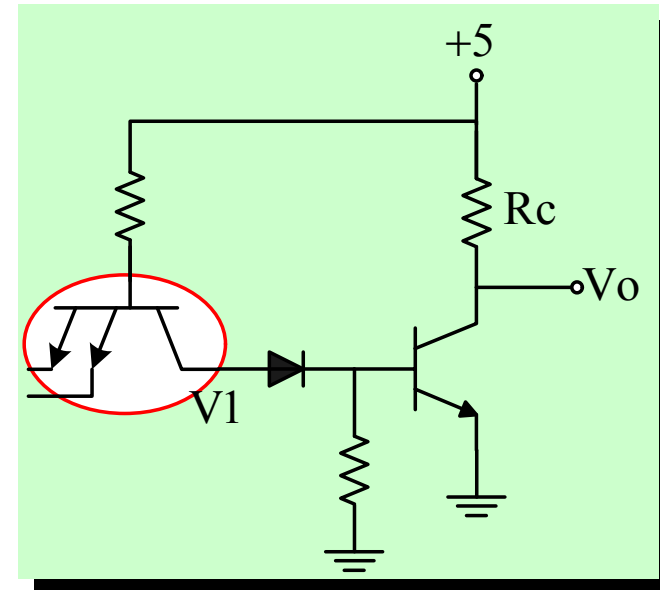
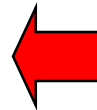
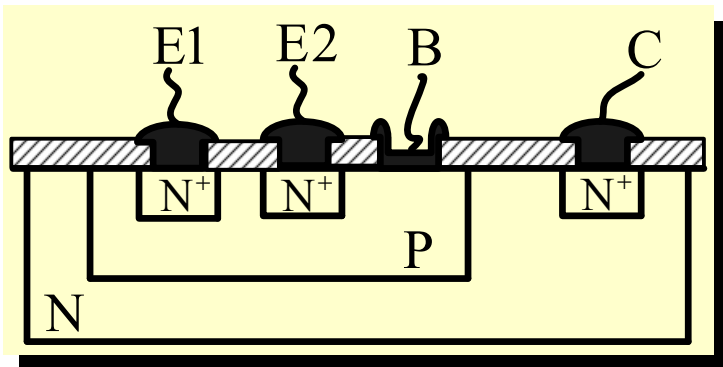
DTL



TTL

# TTL

## ► Multi Emitter Cross Section

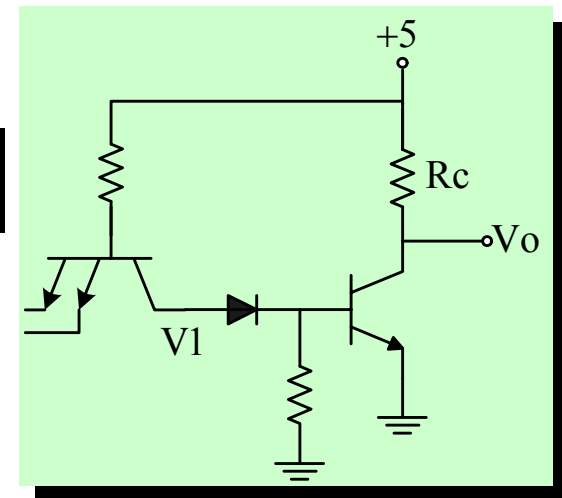


# TTL

- ▶ If input is low

$$\Rightarrow V_1 = 0.1(\text{Low}) + 0.1(V_{CEsat}) = 0.2V$$

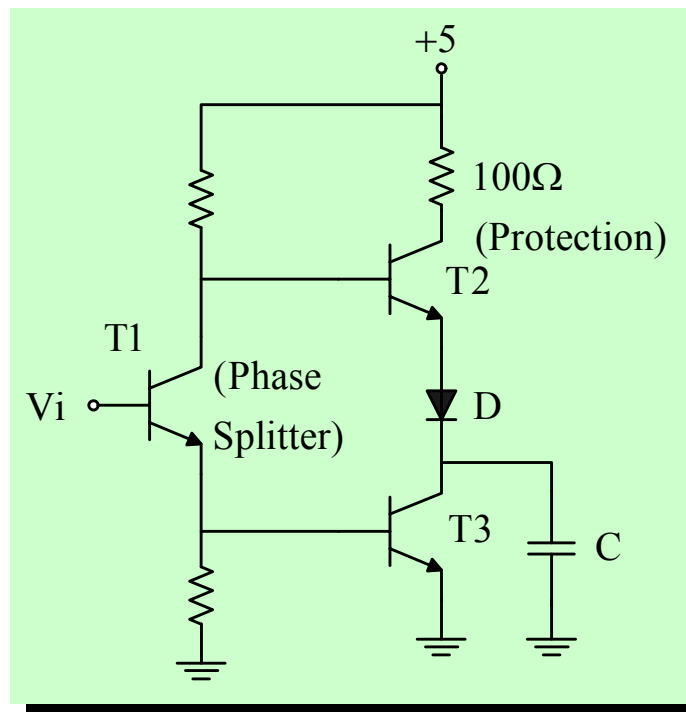
- ▶ In this configuration the pull down is very good but pull up is not, because the output configuration is **CE**
- ▶ In **CC** the situation is Reverse!
- ▶ By combining this two configurations we have a better output stage!





# TTL

## ► Totem Pole Output



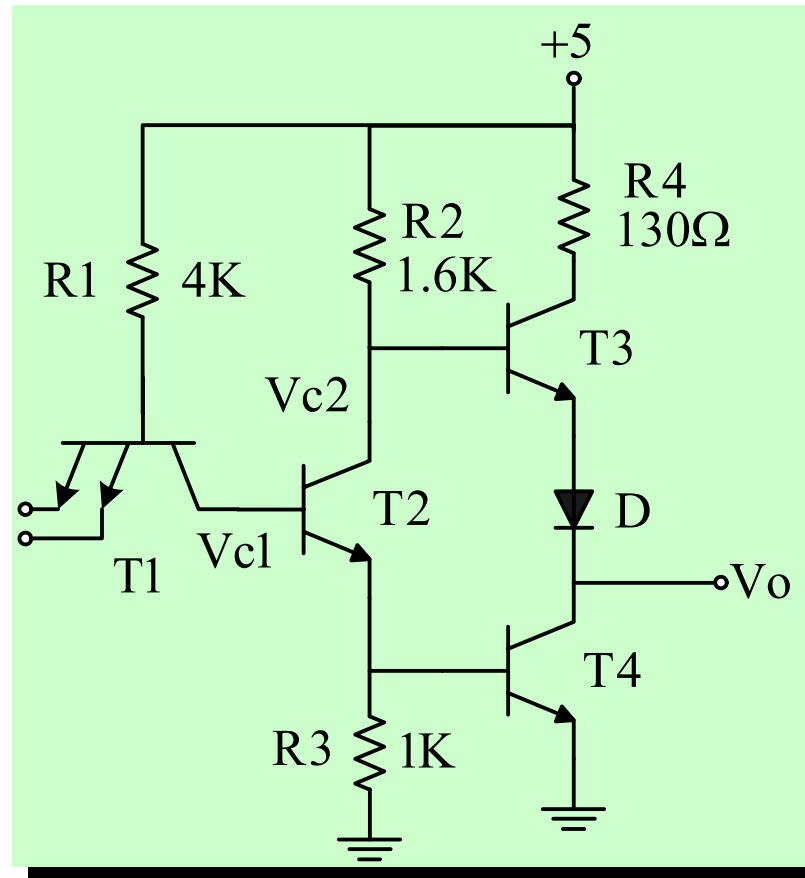
$V_i = \text{High} \rightarrow T_1 = \text{sat}, T_3 = \text{sat} \Rightarrow D$  is used for  $T_2 = \text{off}$

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# Standard TTL



# Standard TTL

## ► VTC

$V_i = 0.1V \Rightarrow V_{c1} = 0.2 \Rightarrow T_2, T_4 = \text{off}$

$\Rightarrow V_{c2} \approx 5V \Rightarrow V_{OH} = 5 - 2 \times 0.7 = 3.6V$

$V_i = 0.6V \Rightarrow V_{c1} = 0.7V \Rightarrow T_2 = \text{on} \rightarrow V_o \downarrow$

$V_i = 1.3V \Rightarrow V_{c1} = 1.4V \Rightarrow T_2, T_4 = \text{on}$

$\Rightarrow I_{E2} = (I_{B4} \approx 0) + \frac{0.7V}{1K} \approx 0.7mA$

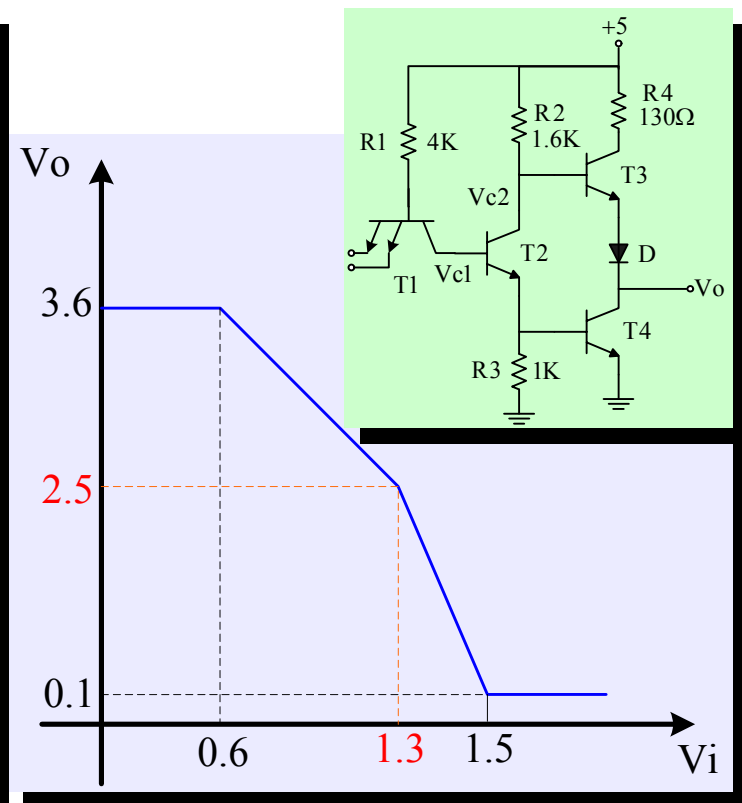
$\Rightarrow V_{R2} = 0.7mA \times 1.6K = 1.12V$

$\Rightarrow V_{c2} = 5 - 1.12 \approx 3.9V$

$\Rightarrow V_o = 3.9 - 1.4 = 2.5V$

$V_i = 1.5V \Rightarrow V_{c1} = 1.6V \Rightarrow T_2, T_4 = \text{sat}$

$\Rightarrow V_o = 0.1V$



# Standard TTL

## ► Fan (In, Out)

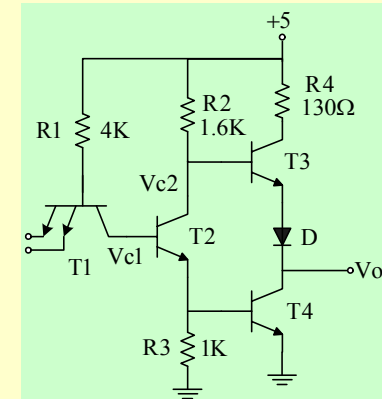
$V_i > 1.5V \Rightarrow V_{BCT1} = 0.7$  ( $V_{BET1} < 0.6$ )  $\Rightarrow$  T1 = **Reverse Mode**

$$I_E = \beta_R I_B, \quad I_C = (\beta_R + 1)I_B, \quad I_B = \frac{5 - 2.3}{4K} = 0.675\text{mA}, \quad \beta_R = 0.2$$

$$\sum N I_{E1} = \beta_R I_B$$

$$\Rightarrow I_{E1} = \frac{0.2 \times 0.675\text{mA}}{2} = 0.0675\text{mA} = 67.5\mu\text{A}$$

In DTL it was equal to  **$I_o \approx 0$**



# Standard TTL

## ► Fan (In, Out)

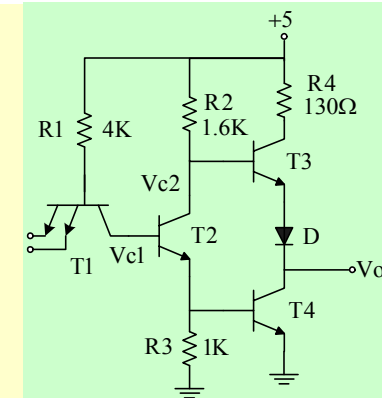
$$I_{IL} = I_E = I_B + I_C \approx I_B = \frac{5 - 0.9}{4K} \approx 1mA$$

$$I_{csat2} = \frac{5 - 0.9}{1.6K} = \frac{41}{16}, \quad I_{Bsat4} = \frac{41}{16} - \frac{0.8}{1K} = 1.76mA$$

$$I_{csat4} = \beta_{min} I_{Bsat4} = (\beta = 10) \times 1.76 = 17.6mA$$

$$\Rightarrow FO_L = \frac{17.6^{mA}}{1^{mA}} = 17, \quad FO_H = \frac{I_{R4}}{67.5\mu A} > FO_L \Rightarrow FO = FO_L = 17$$

Real FO = 10 ( $\beta_{min} = 6$ )



# Standard TTL

## ▶ NM

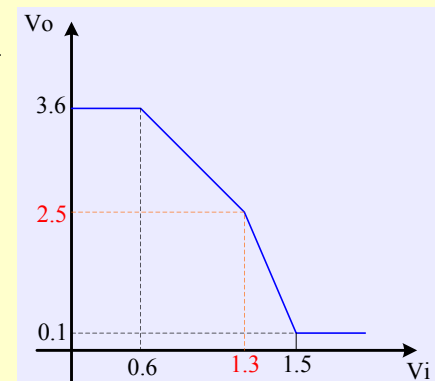
- ▶ Accept the following values because VTC has not high slope

$$\underline{V_{OH}} = 2.5V, \quad \underline{V_{IH}} = 1.5V, \quad \overline{V_{IL}} = 1.3V, \quad \overline{V_{OL}} = 0.2V$$

$$\Rightarrow NMH = \underline{V_{OH}} - \underline{V_{IH}} = 2.5 - 1.5 = +1V$$

$$NML = \overline{V_{IL}} - \overline{V_{OL}} = 1.3 - 0.2 = 1.1V$$

$$\Rightarrow NM = 1V$$



# Standard TTL

## ► Pdis

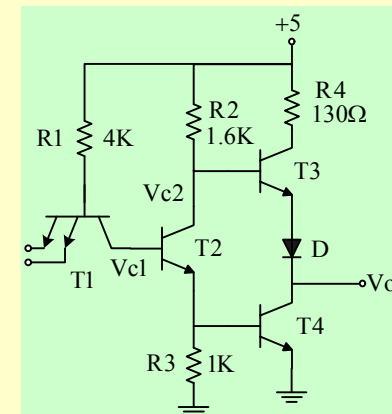
$$P_{\text{disL}} = (T2 = \text{off}) = 5^{\text{V}} \times 1^{\text{mA}} - 0.1^{\text{V}} \times 1^{\text{mA}} = 4.9\text{mW}$$

$$P_{\text{disH}} = V_{\text{Ii}} I_{\text{i}} + (I_{\text{R1}} + I_{\text{R2}}) V_{\text{CC}} + V_{\text{OL}} I_{\text{iL}} =$$

$$3.6^{\text{V}} \times 67.5^{\mu\text{A}} + (0.675^{\text{mA}} + 2.56^{\text{mA}}) \times 5^{\text{V}} + 0.1^{\text{V}} \times 1^{\text{mA}} \\ = 16.53\text{mW}$$

$$\Rightarrow P_{\text{dis}} = \frac{1}{4} (3 \times 4.9^{\text{mW}} + 1 \times 16.53^{\text{mW}})$$

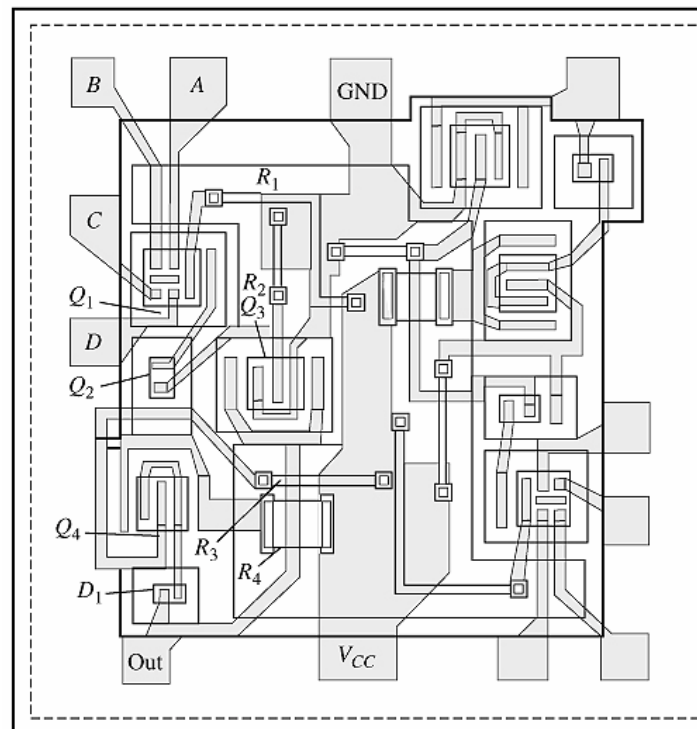
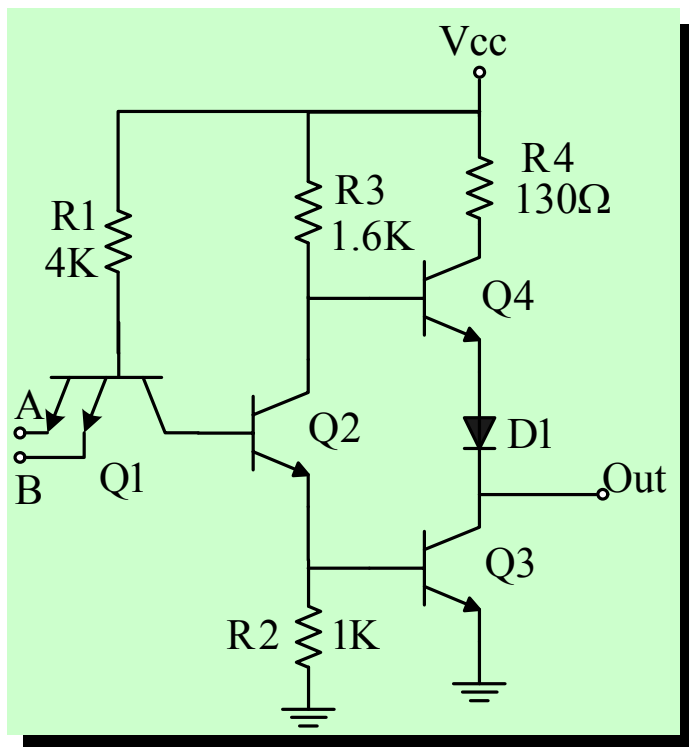
$$\approx 8\text{mW}$$





# Standard TTL

## ► Layout

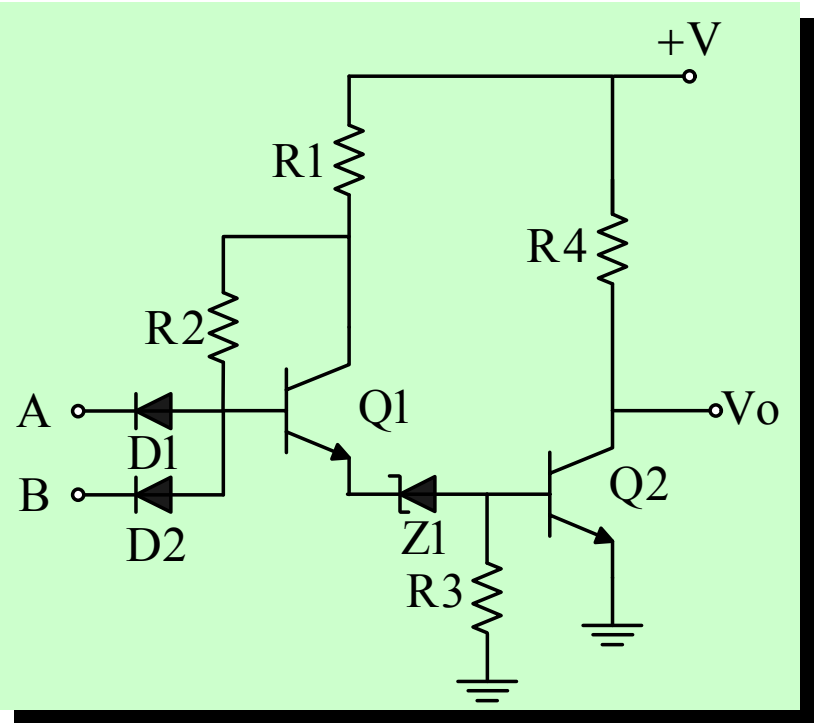


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# High Threshold Logic (HTL)



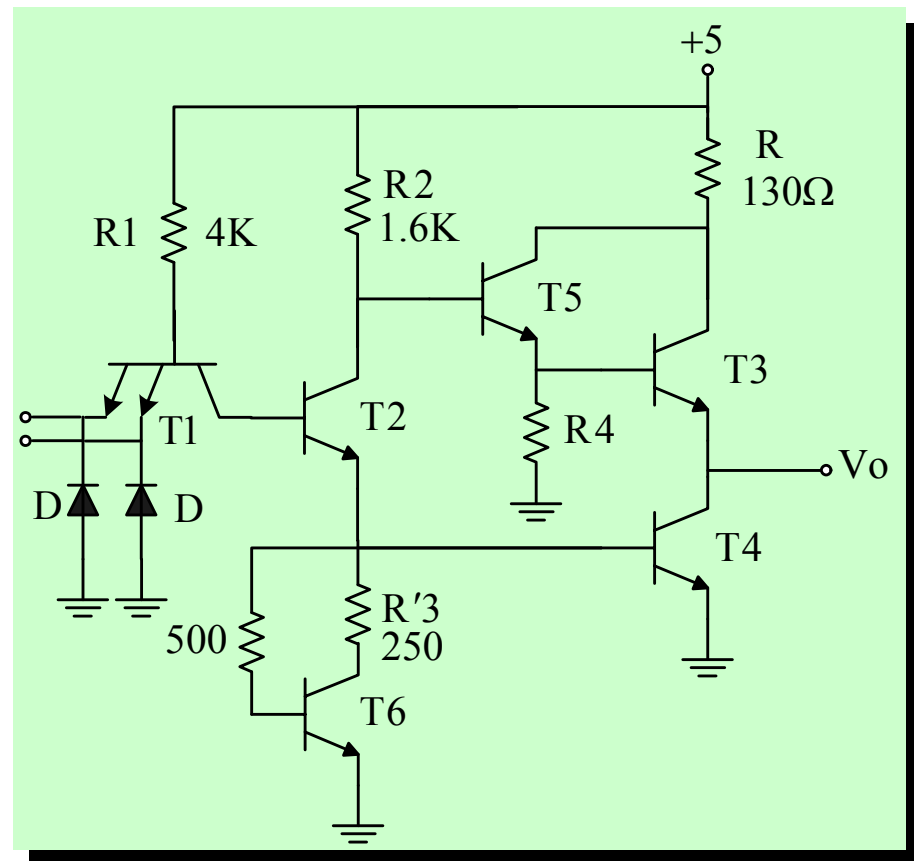
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# High Speed TTL (74HXX)

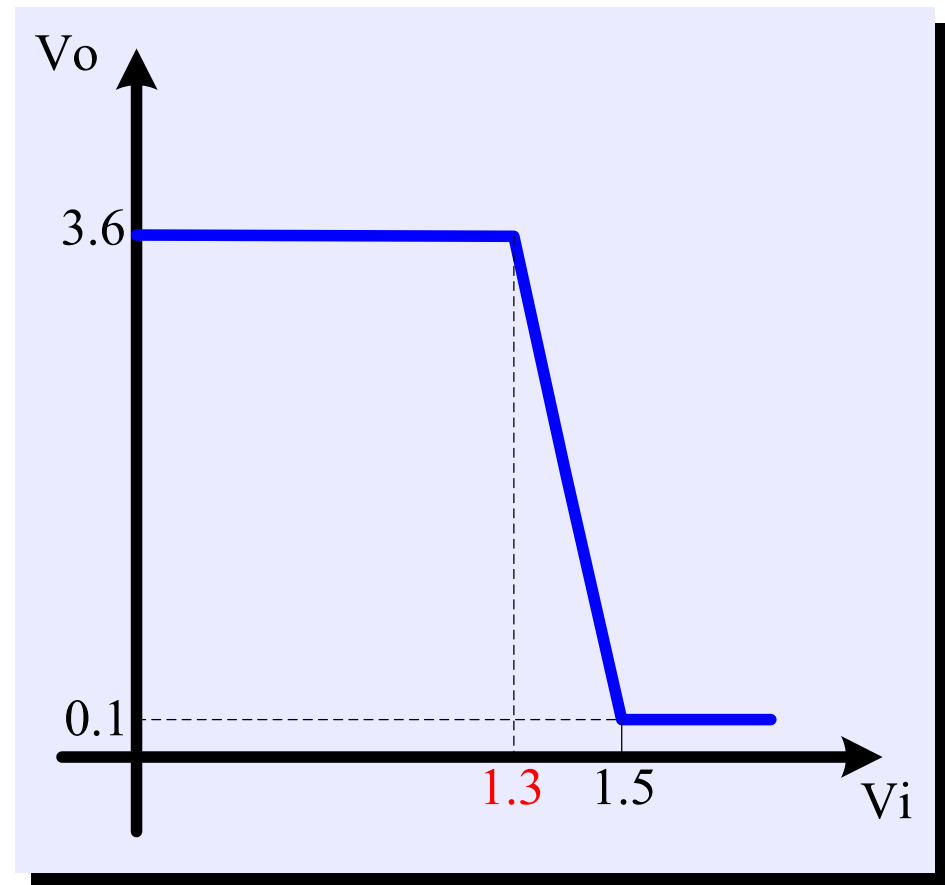
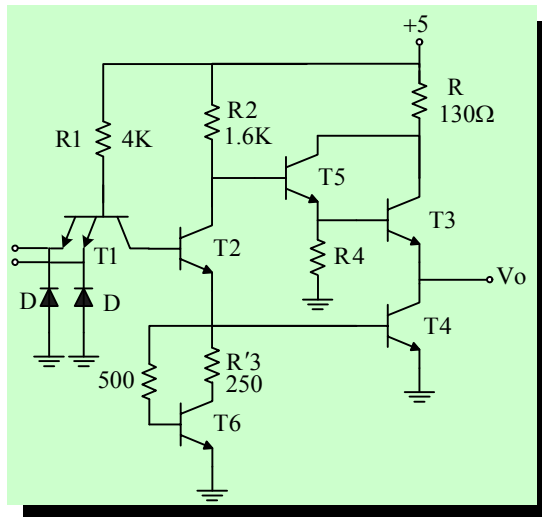
- ▶ In previous T1 , T2 , (T3) and T4 can be saturated but in this circuit T5 prevent T3 from going to saturation
- ▶ After T2=off , T6 discharges the base of T4 then the switching speed of T4 is very high
- ▶ In previous we could not decrease the R3, because the current for conducting T4 must be increased!!
- ▶ D is used for compensating the ringing



# HSTTL

## ▶ VTC

- ▶ TTL has a curvature in VTC for R3 because at first T2=on and then T4=on, but in this circuit T2,T4 must be conducted together



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# Tri-State Logic

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- ▶ **Totem-pole outputs should not be tied together**
- ▶ **Therefore, tri-state bus driver or open collector output can be used to prevent this problem**
- ▶ **Usually used to bus multiple signals on the same wire**
- ▶ **Advantage:**  
**The output of tri-state ICs can be connected together without sacrificing switching speed**



# Tri-State Logic

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- ▶ **Tri-state logic has three possible output states:**
  - ▶ high
  - ▶ low
  - ▶ high impedance (Hi-Z)
- ▶ **Tri-state logic is used as bus-driver where more than one output can be connected together**
- ▶ **There is an input controlling the output state, enable or disable**
  - Enable state:** The output operates as a conventional gate, the output level is either high or low
  - Disable state:** The output is an open circuit, it is the Hi-Z state

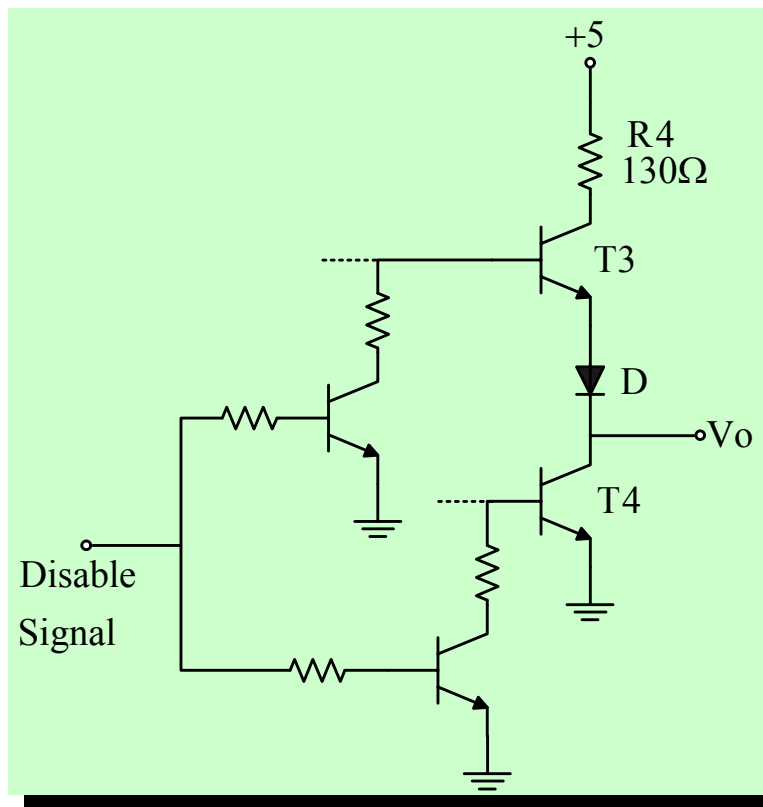
# Tri-State Logic

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- ▶ **Tri-state bus driver can be non-inverting or inverting**
- ▶ **When more than one outputs are connected to a bus, only one of them can be at enable state, the others must be disabled. Otherwise, excessive current will flows through the output stage (in case of TTL) or output will be at abnormal level (in case of CMOS)**

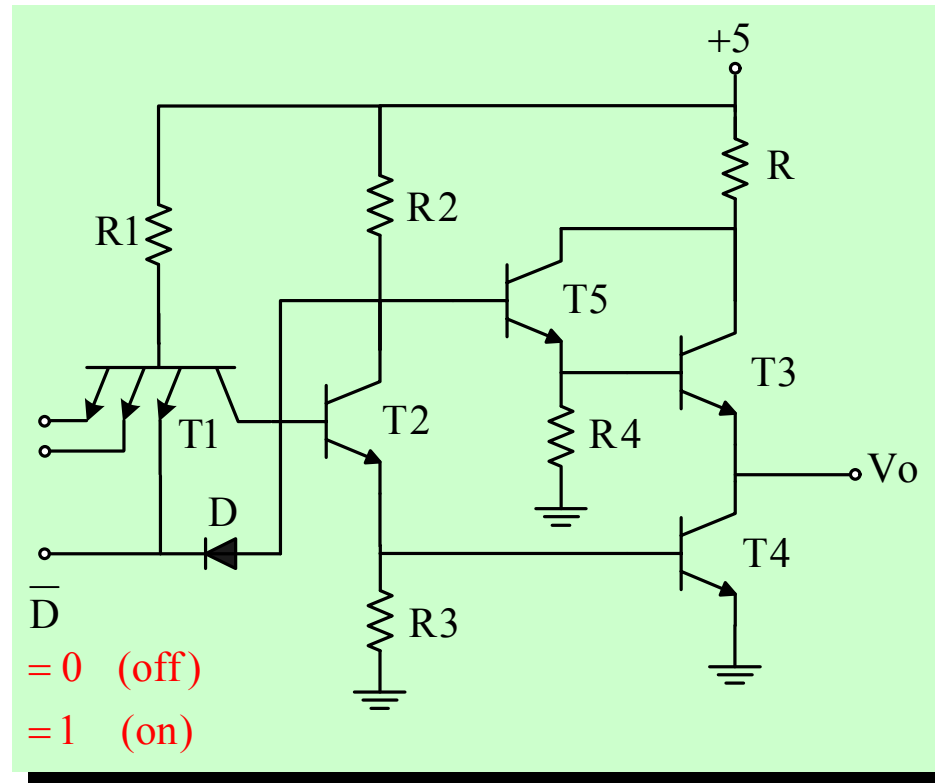
# Tri-State Logic

## ▶ Example 1



# Tri-State Logic

## ► Example2



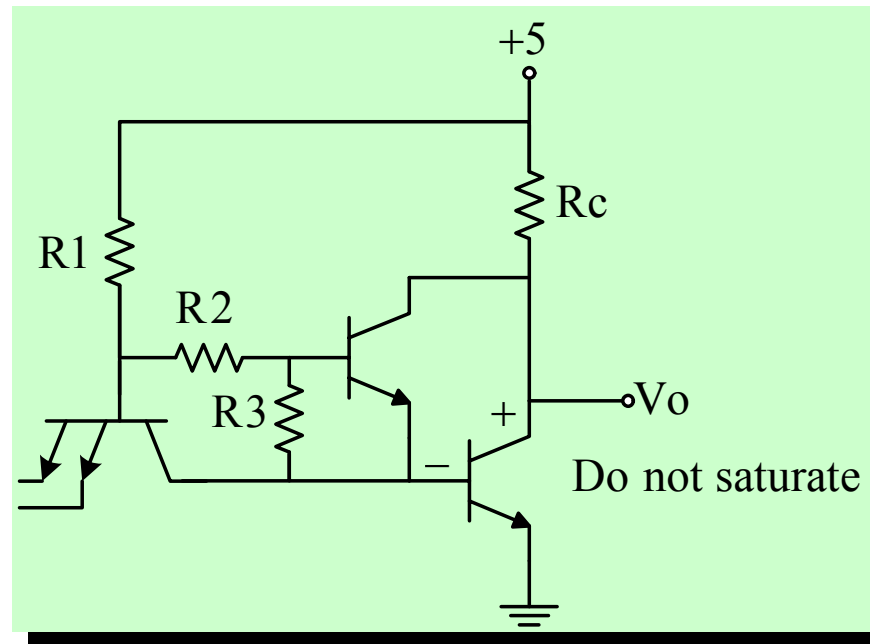
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# Storage Delay Time

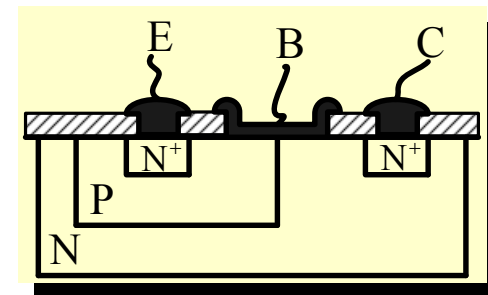
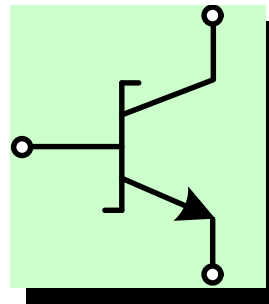
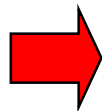
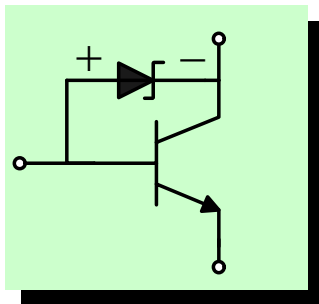
- ▶ This delay has a max respect to other therefore must be reduced
- ▶ One method for reduction is as follow



# Storage Delay Time

## ▶ Schottky Diode

- ▶ In previous method we need a large area
- ▶ Another method is using schottky transistor



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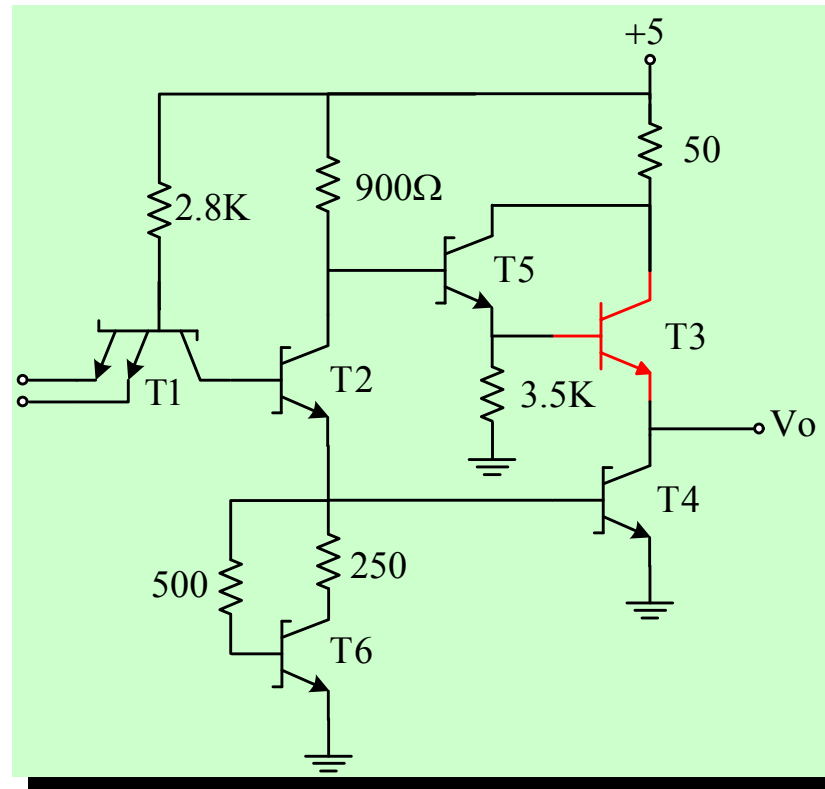
# Schottky TTL (74SXX)

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- ▶ **High speed variant of TTL**
- ▶ **Schottky transistors which have faster switching speed**
- ▶ **Schottky-barrier diode connected from base to collector to prevent transistor from going into saturation**

# Schottky TTL

- ▶ All of transistor (except T3) are replaced by schottky transistor



# Schottky TTL

## ► NM

$$V_{\text{Donsh}} = V_{\text{BConsh}} = 0.5\text{V}$$

$$V_{\text{BEsat4}} = 0.8\text{V}, V_{\text{BCon4}} = 0.5\text{V} \Rightarrow V_{\text{CEsat4}} = 0.3\text{V}$$

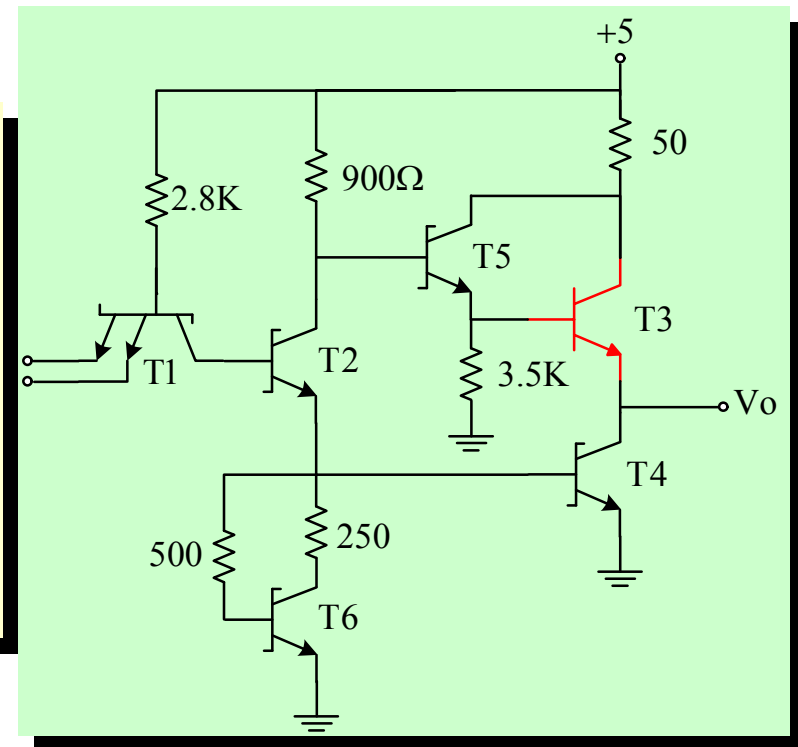
$$\Rightarrow \underline{V_{\text{OL}}} = 0.3\text{V} = \overline{V_{\text{OL}}}, \quad \overline{V_{\text{IL}}} = 0.7$$

$$\text{NM} = 0.4\text{V}$$

$$\overline{V_{\text{OH}}} = 3.6\text{V}$$

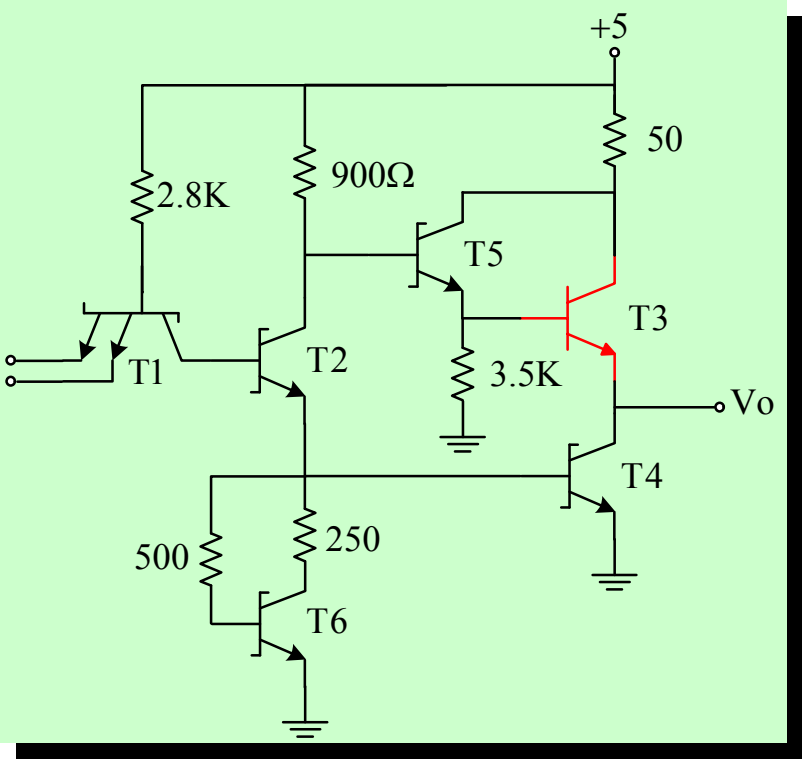
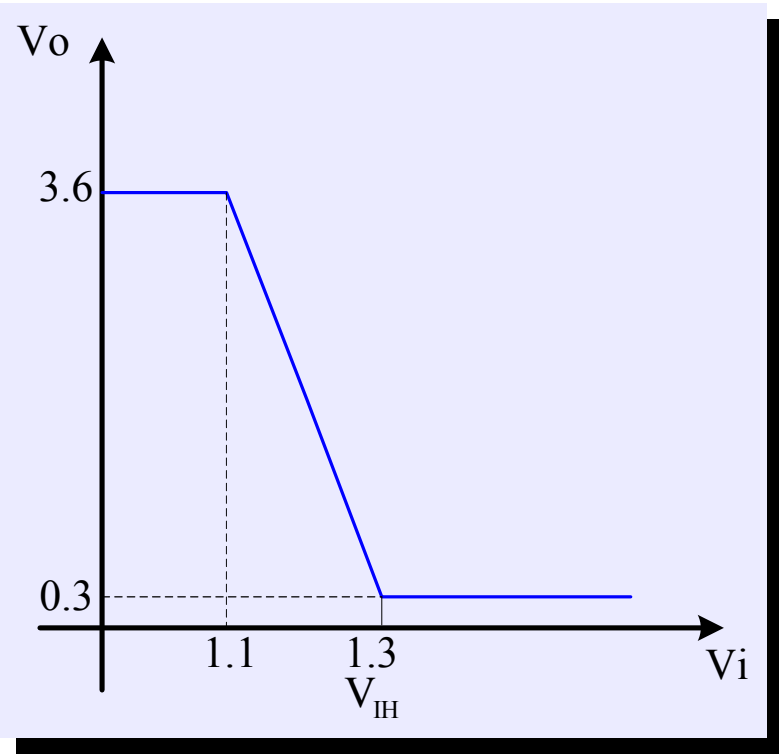
$$\underline{V_{\text{OH}}} = 5 - 1.6 = 3.4\text{V}$$

$$\underline{V_{\text{IH}}} = 1.3\text{V}$$



# Schottky TTL

## VTC



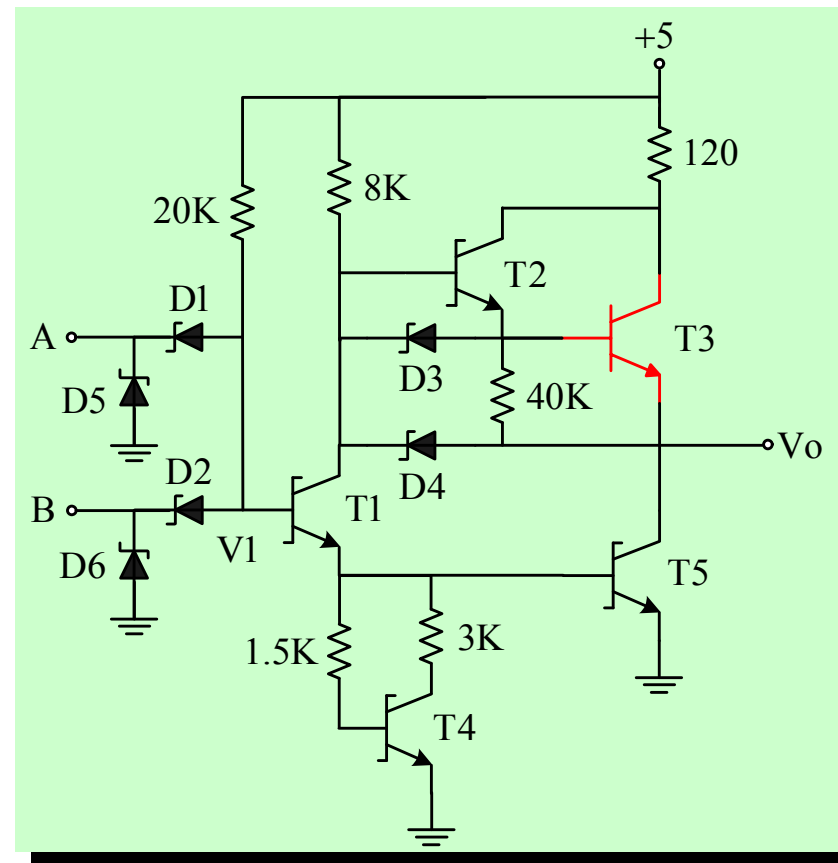
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# Low Power Schottky Clamped TTL (74LSXX)

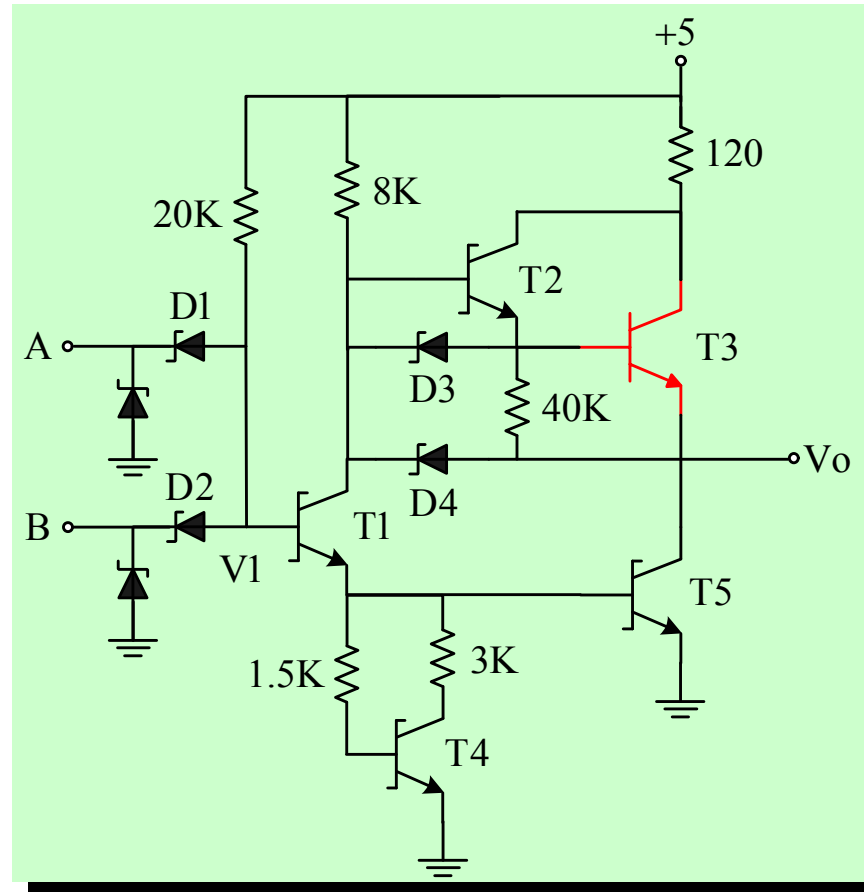
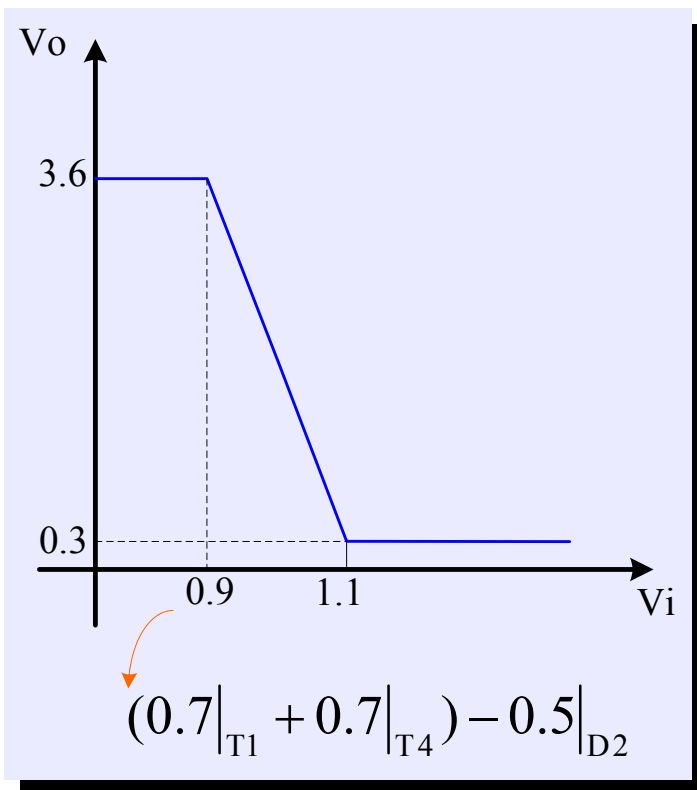
- ▶ The input do change as figure
  - ▶ Resistors are large
  - ▶ Component function
    - D1, D2: AND function
    - D5, D6: High-speed clamping of input signal excursions below ground
    - D3, D4: Stored charge removal of the base of T2 and T3 on Positive transition of the input
    - 20K $\Omega$  resistor connected to D1 and D2: Small amount of current source





# LSTTL

## ► VTC





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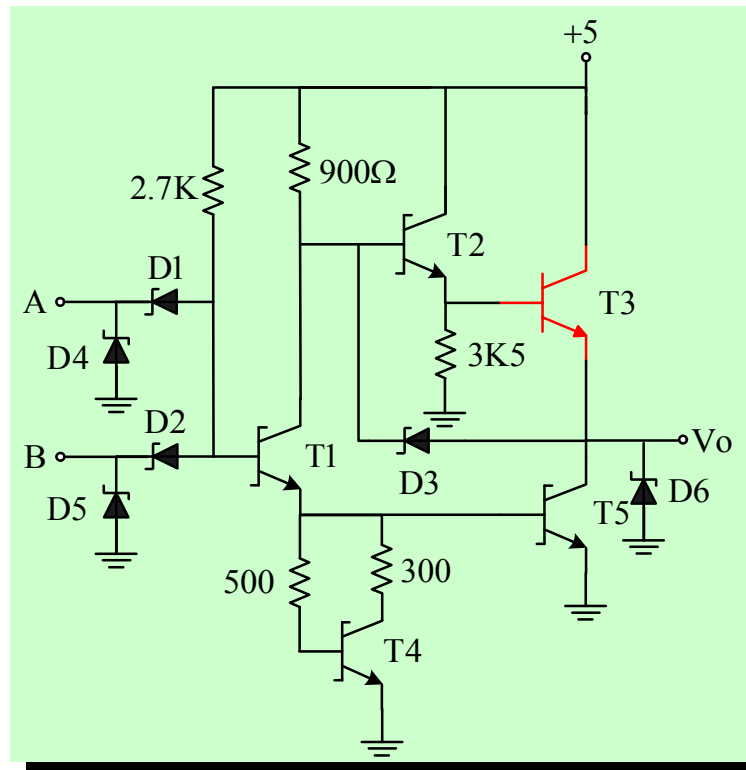
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- ▶ **Summary**

# Advanced Schottky (74ASXX)

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- ▶ **In the early to middle 1980s**
  - ▶ Discontinuing
- ▶ **Letter designator**
  - ▶ F: fast advanced Schottky TTL
  - ▶ ALS: advanced low-power Schottky TTL
  - ▶ AS: advanced Schottky TTL
- ▶ **Selection criteria of FAST vs. AS**
  - ▶ Price, availability

# Advanced Schottky (74ASXX)



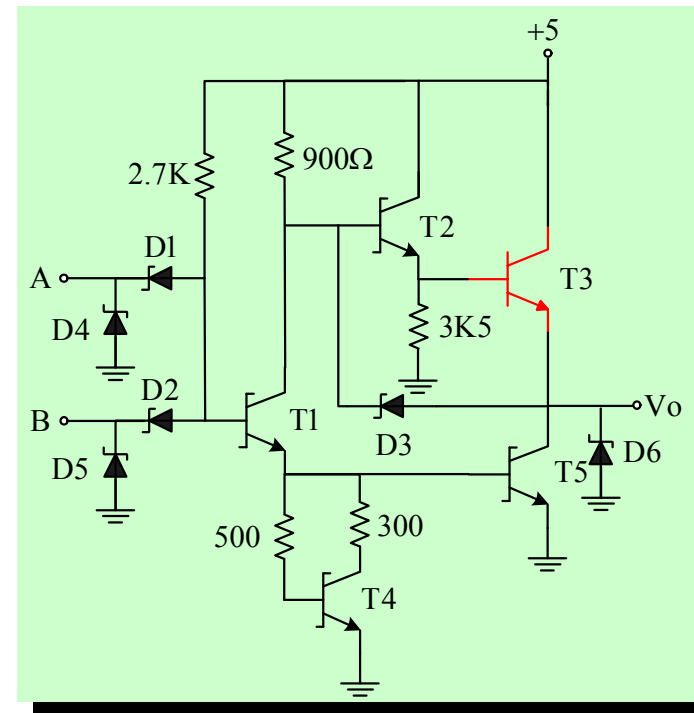
Res ↓, I ↑ ⇒ AS

# Advanced Schottky (74ASXX)

## ▶ Input circuit

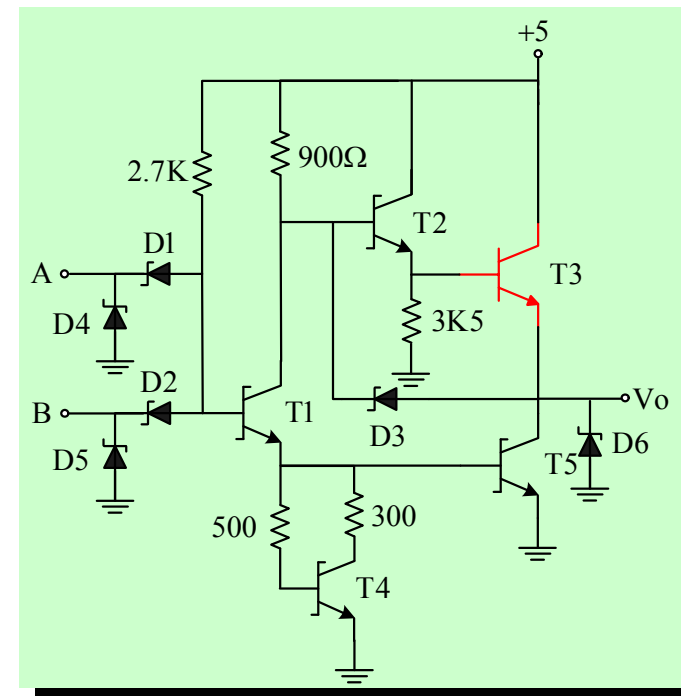
### ▶ Component function

- D1, D2: AND function
- D4, D5: High-speed clamping of input signal excursions below ground
- D3: Stored charge removal of the base of T3 in output on Positive transition of the input
- 2.7K $\Omega$  resistor connected to D1 and D2: Small amount of current source



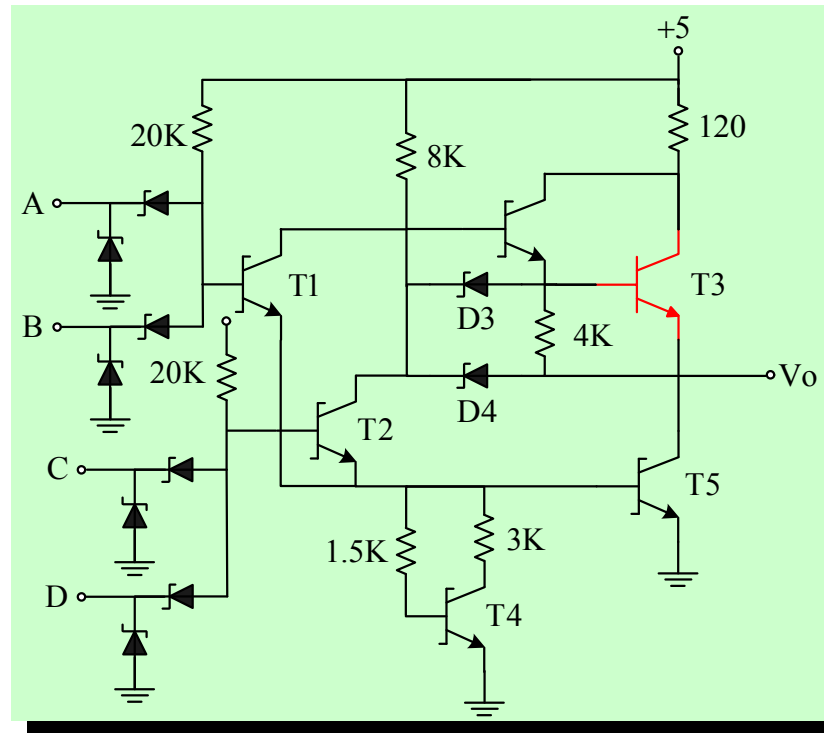
# Advanced Schottky (74ASXX)

- ▶ **Output circuit**
  - ▶ T2, T3: Darlington pair
  - ▶ D6: negative voltage excursions reductions due to reflection caused by transmission-line effects



# Advanced Schottky (74ASXX)

## ► Combination Circuit (AND + OR + Inverter)



$$Y = \overline{AB + CD}$$

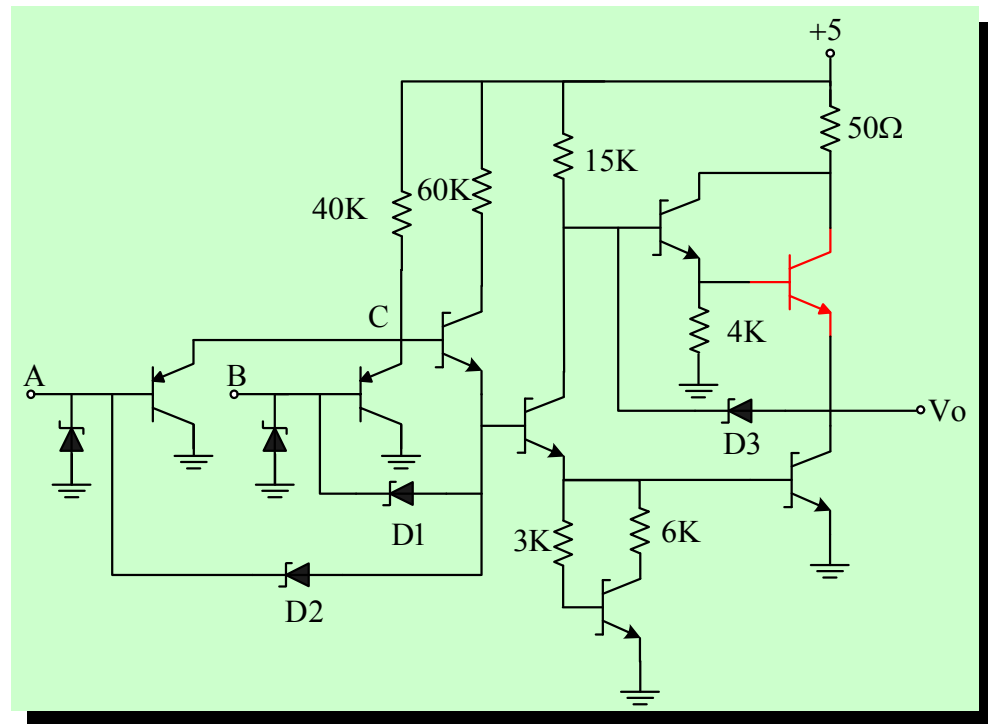
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# Advanced Low Power Schottky (74ALSXX)

- ▶ Input transistors do not have to be schottky, because they do not saturate
- ▶ If we use schottky for them, the area will be large!



Res ↑, I ↓ ⇒ ALS



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- ▶ Emitter Coupled Logic (ECL)
- ▶ I<sup>2</sup>L , MTL
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- ▶ Compatibility of Logic Families
- ▶ Noise Margins of Logic Families
- ▶ Summary

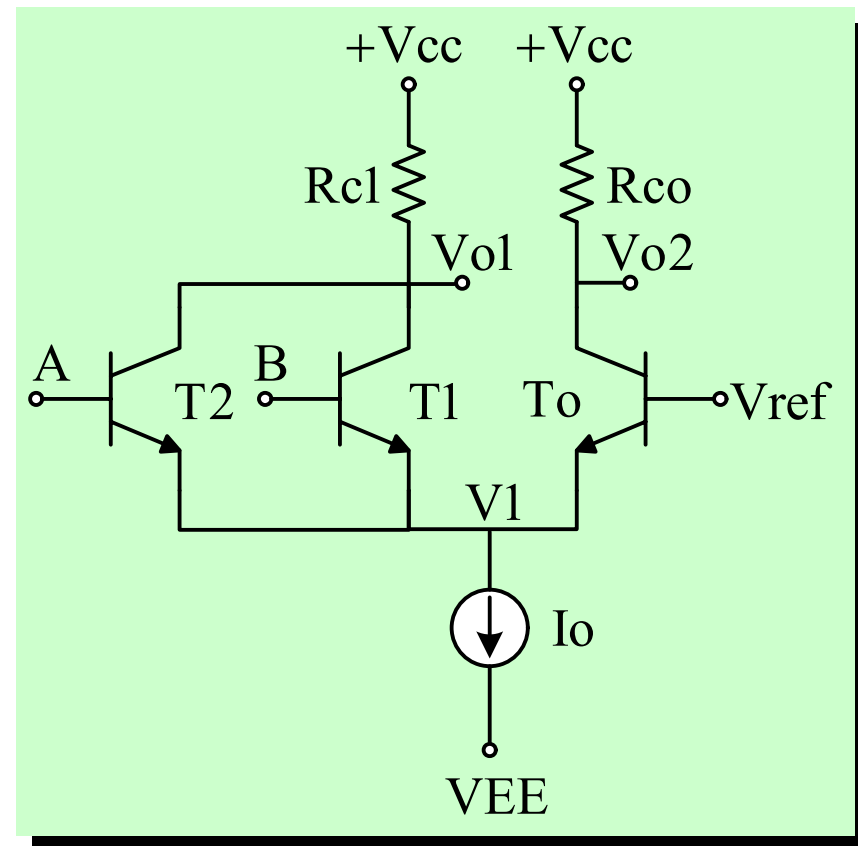
# Emitter Coupled Logic (ECL)

---

- ▶ **Current steering rather than saturating transistors to represent logic 0/1**
- ▶ **Extremely high-speed**

# ECL

- ▶ We do not saturate any transistor!



# ECL

## ► VTC

$$I_{C1} = I_S \left[ \exp\left(\frac{V_i - V_1}{V_t}\right) - 1 \right]$$

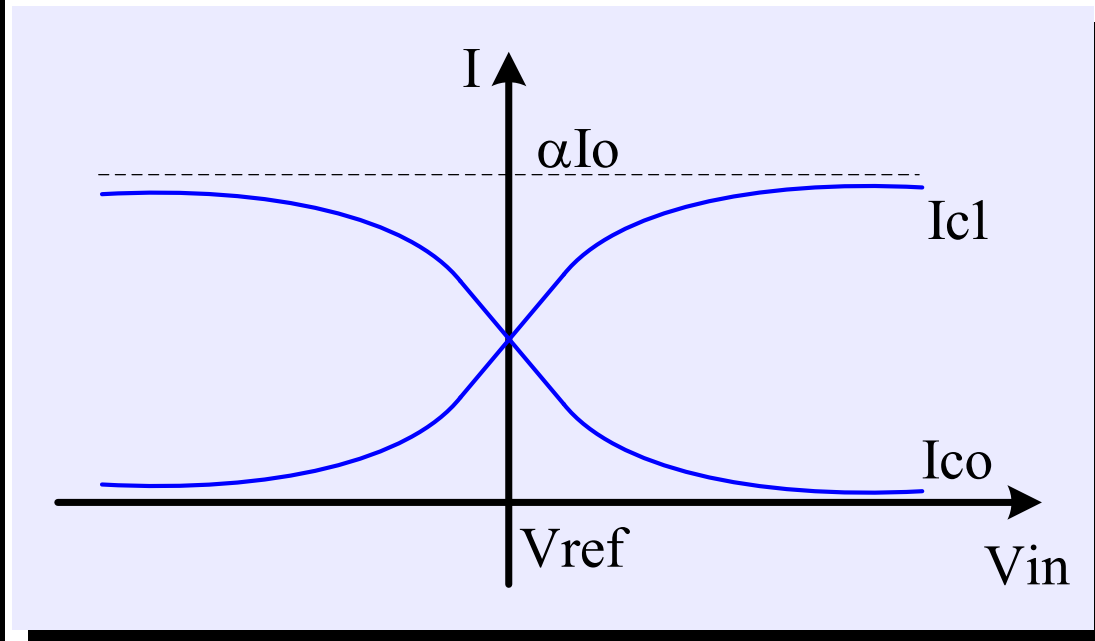
$$I_{C0} = I_S \left[ \exp\left(\frac{V_{ref} - V_1}{V_t}\right) - 1 \right]$$

$$\frac{I_{C1}}{I_{C0}} \approx \exp\left(\frac{V_i - V_{ref}}{V_t}\right) \Rightarrow$$

$$V_i - V_{ref} = V_t \ln\left(\frac{I_{C1}}{I_{C0}}\right)$$

$$I_{C1} + I_{C0} = \alpha I_o \Rightarrow$$

$$\frac{I_{C0}}{\alpha I_o} = \frac{1}{1 + \exp\left(\frac{V_i - V_{ref}}{V_t}\right)}$$



# ECL

$$I_{C1} = 100I_{C0} \rightarrow V_i - V_{ref} \approx 100mV$$

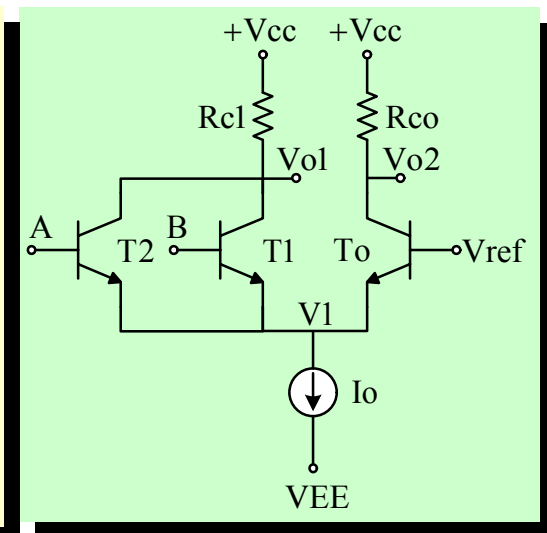
$\Rightarrow T_o \approx \text{off}, T1 \approx \text{on}$

From one output  $\rightarrow$  NOR Gate

From other output  $\rightarrow$  OR Gate

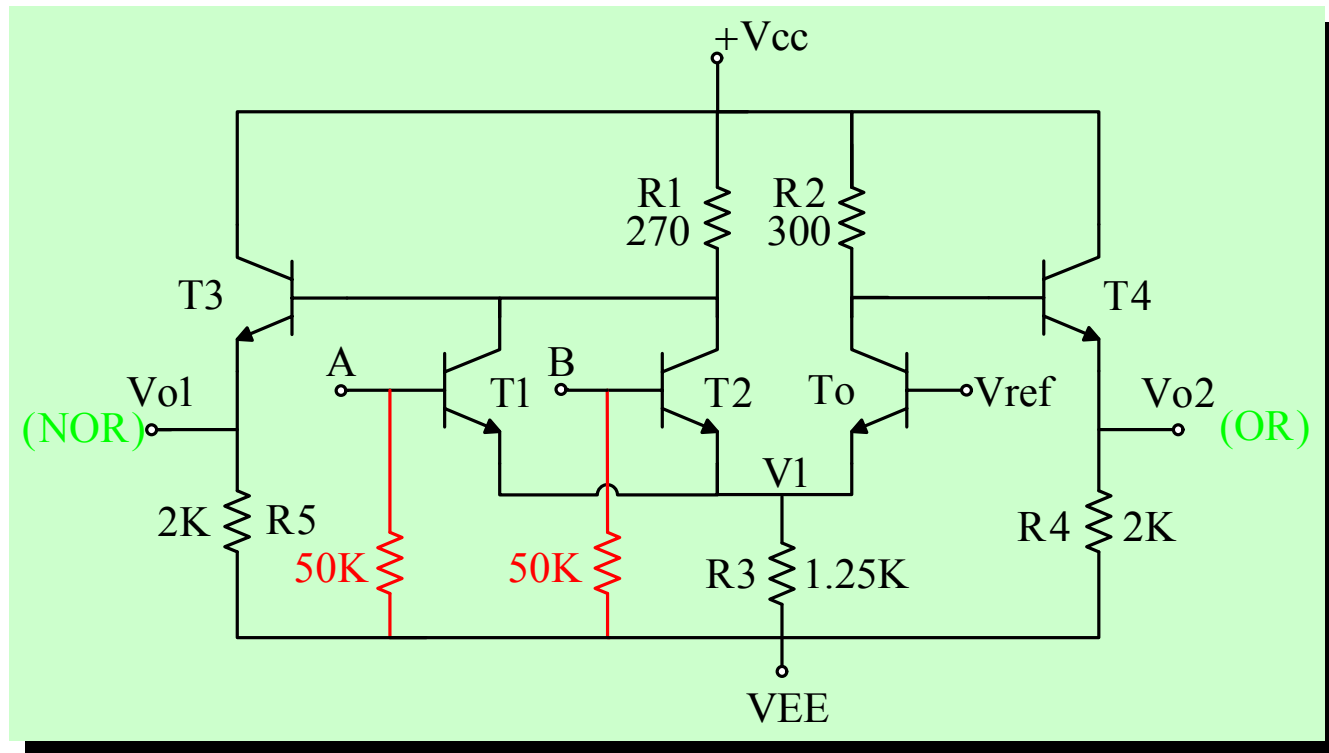
$$\text{For Similarity} \rightarrow V_{ref} = \frac{1}{2}(V_{OH} + V_{OL})$$

In ECL we need  $V_{EE} \uparrow$  and  $V_{cc} \rightarrow 0$  for noise reduction



# ECL

## ► OR + NOR



# ECL

## ► Noise Immunity

T1, T2 ≈ off ⇒

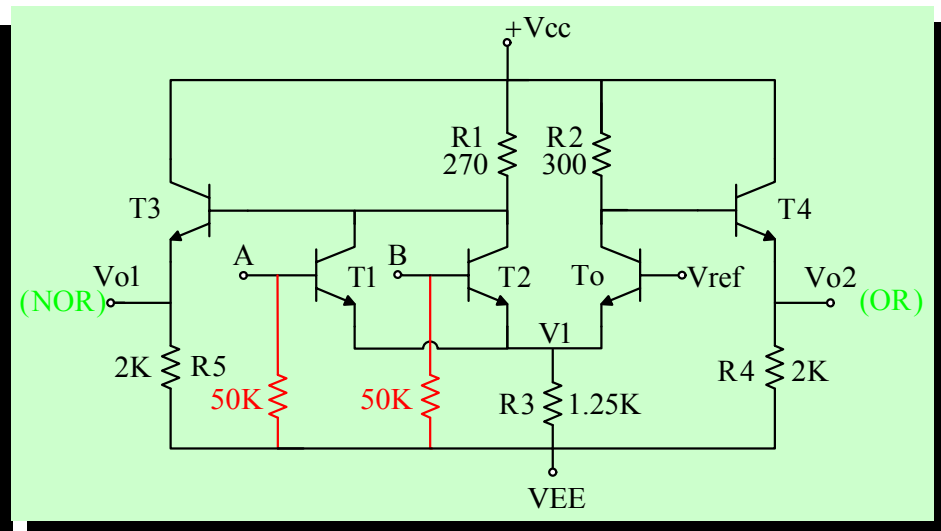
$$I_{B3} = \frac{V_{CC} - (V_{O1} + V_{BE})}{R1} = \frac{V_{O1} - V_{EE}}{R5(\beta + 1)}$$

$$\Rightarrow V_{O1} = \frac{\frac{V_{CC} - V_{BE}}{R1} + \frac{V_{EE}}{(\beta + 1)R5}}{\frac{1}{R1} + \frac{1}{(\beta + 1)R5}} \Rightarrow \frac{R1R5(\beta + 1)}{R1R5(\beta + 1)}$$

$$\left\{ \frac{\delta V_{O1}}{\delta V_{CC}} = \frac{(\beta + 1)R5}{R1 + (\beta + 1)R5} \approx 1 \right.$$

$$\left. \frac{\delta V_{O1}}{\delta V_{EE}} = \frac{R1}{R1 + (\beta + 1)R5} \approx \frac{R1}{(\beta + 1)R5} \right.$$

⇒ VEE is noise immune



# ECL

## ► Vref Circuit

$$V_B = -\frac{V_{EE} - 2V_D}{2.3^K + 0.3^K} \times 0.3^K = -0.428V$$

$$\Rightarrow V_{ref} = +V_B - 0.75 = -1.14V$$

1) A, B → Low,  $V_{cc} = 0$

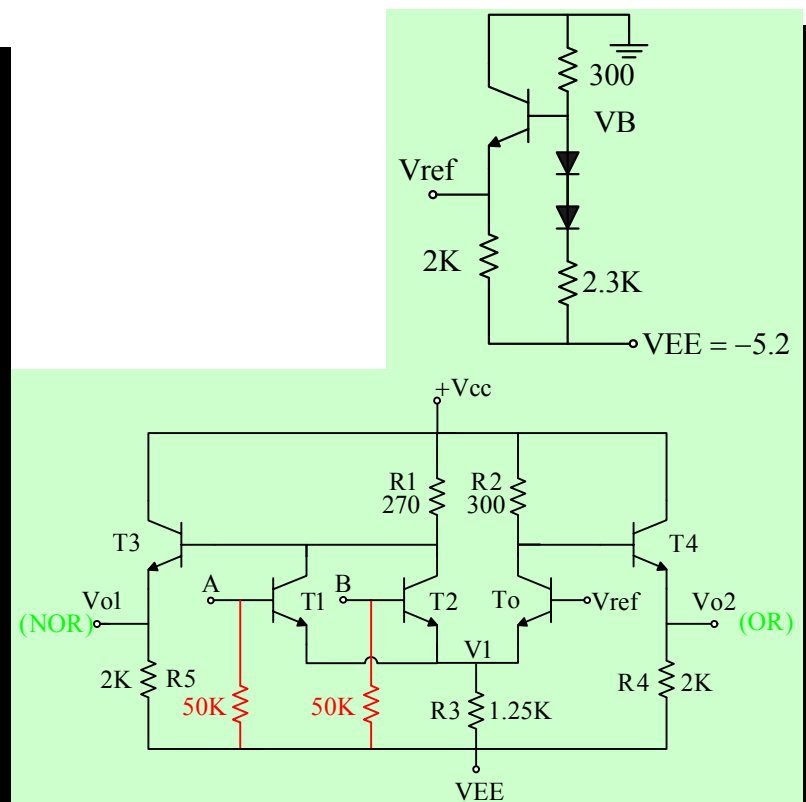
$$\Rightarrow V_{o1} = -0.75V$$

$$V_1 = V_{ref} - 0.75 = -1.9V$$

$$I_{R3} = \frac{5.2 - 1.9}{1.25^K} = 2.64mA$$

$$V_{R2} = -2.64^{mA} \times 0.3^K = -0.792V$$

$$V_{o2} = V_{R2} - 0.75 = -1.542V$$





# ECL

## ► Vref Circuit

$$V_B = -\frac{V_{EE} - 2V_D}{2.3K + 0.3K} \times 0.3K = -0.428V$$

$$\Rightarrow V_{ref} = +V_B - 0.75 = -1.14V$$

$$2) A, B \rightarrow \text{High}(-0.75V), \quad V_{cc} = 0$$

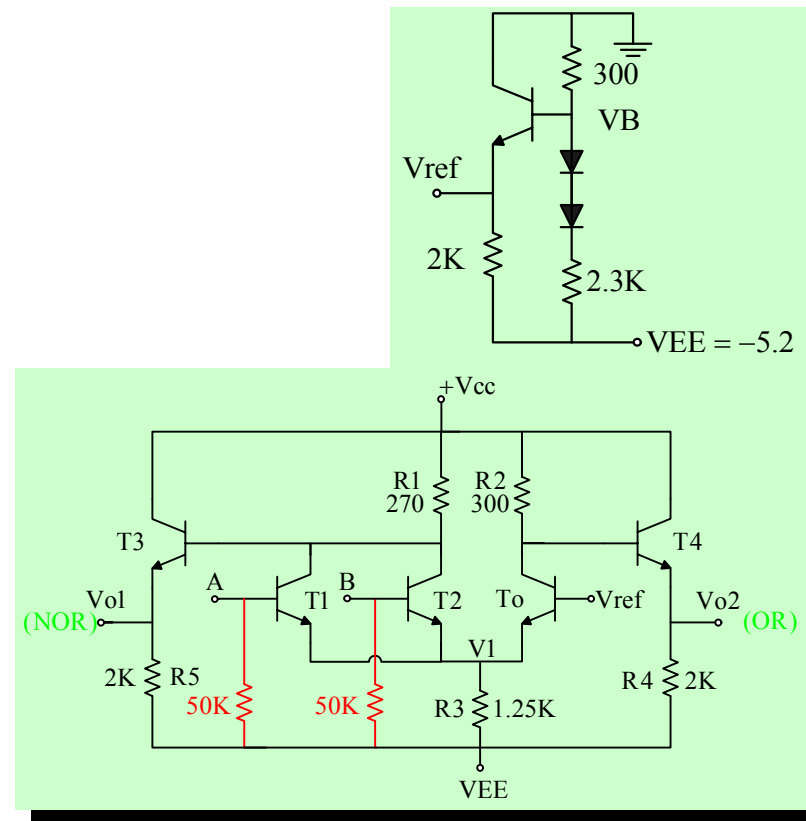
$$\Rightarrow V_{o2} = -0.75V$$

$$V_1 = -0.75V - 0.75V = -1.5V$$

$$I_{R3} = \frac{5.2 - 1.5}{1.25K} = 2.96mA$$

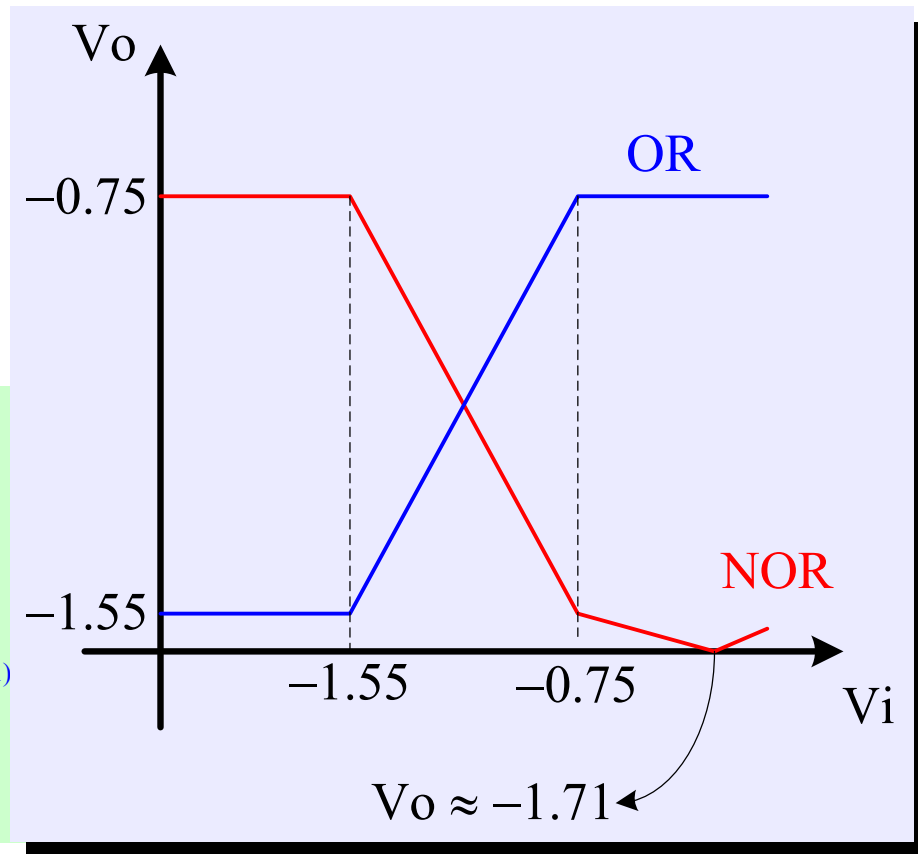
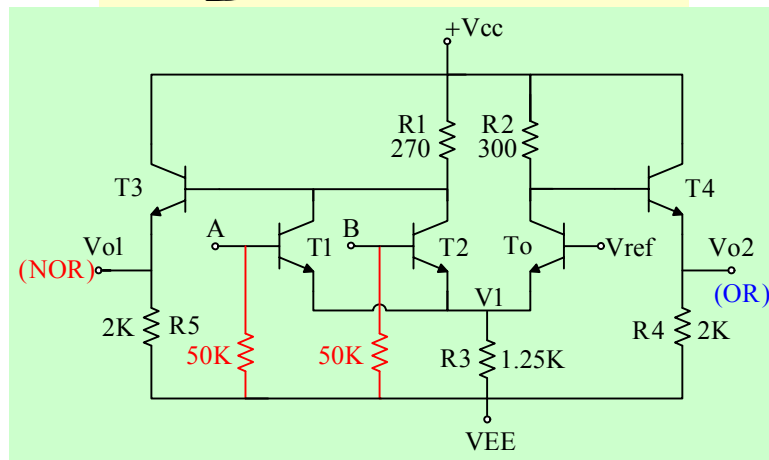
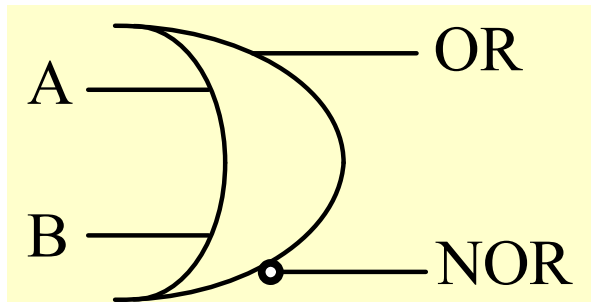
$$V_{R1} = 2.96mA \times 0.27K \approx 0.8V$$

$$V_{o1} = V_{R1} - 0.75 = -1.55V$$



# ECL

## ► Symbol and VTC



# ECL

- ▶ **VTC**
- ▶ **T1 may be saturate if R3 is used**

$$I_{c1sat} = \frac{VEE - 0.1}{1.25^K + 0.27^K} = 3.36\text{mA}$$

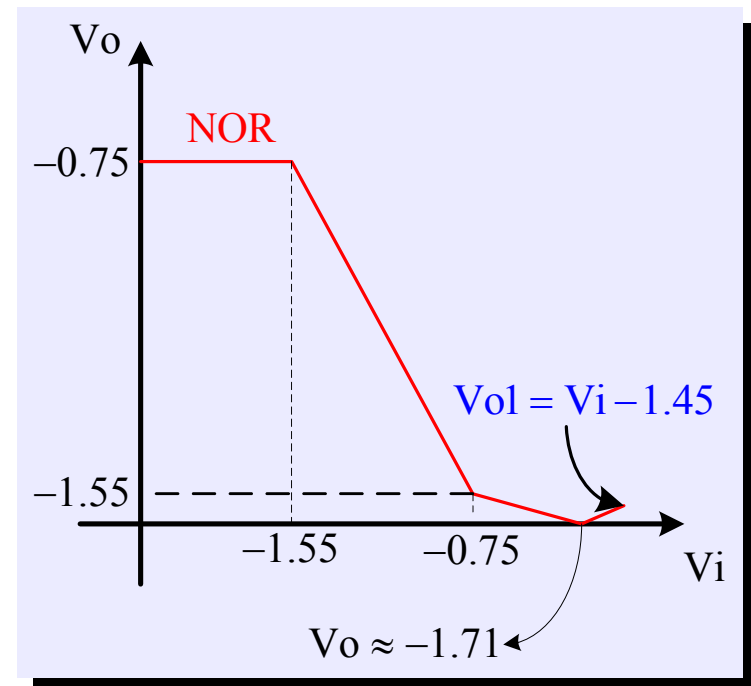
$$\Rightarrow V_{o1} = -0.8 - 3.36^{\text{mA}} \times 0.27^K$$

$$V_{o1} = -1.71\text{V} \quad (V_i = -0.25\text{V})$$

- ▶ **If  $V_i$  is increased more ( $V_i > -0.25$ )**

$$V_{o1} = V_i + V_{BCT1} + V_{BET3}$$

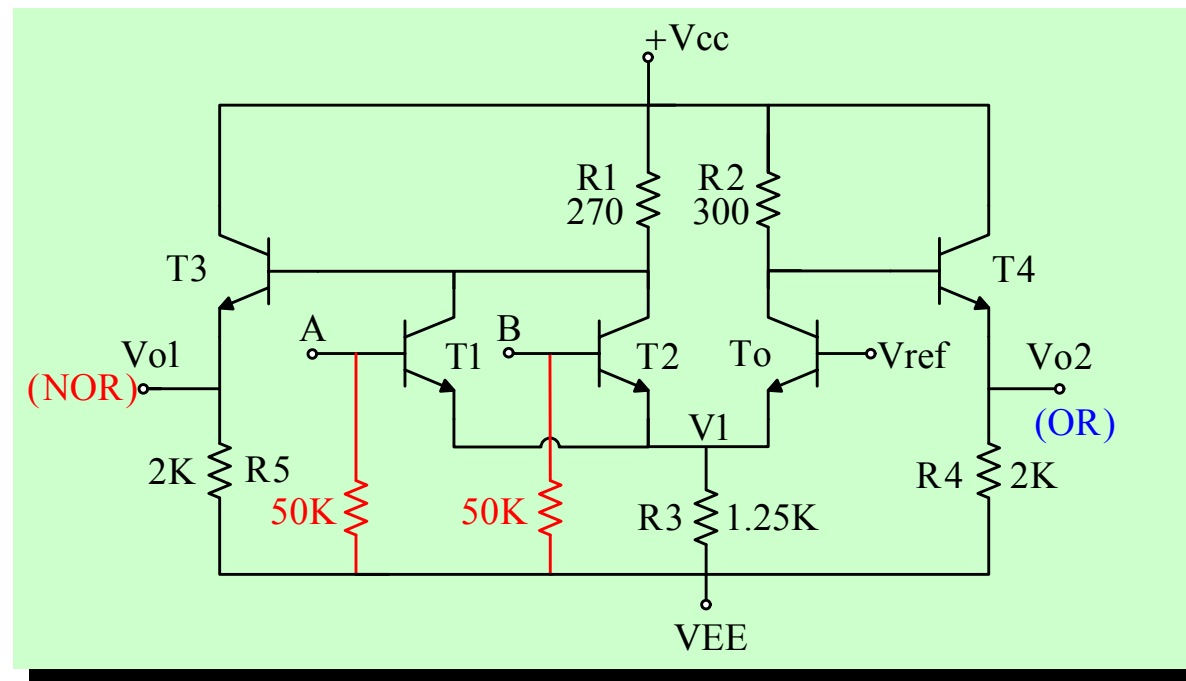
$$\Rightarrow V_{o1} = V_i - 0.7 - 0.75 \quad (\text{for NOR Gate})$$



# ECL

## ► Speed of OR, NOR ECL Gate

- $T_o$  is in CB configuration therefore **OR** is faster than **NOR**



# ECL

## ► Pdis

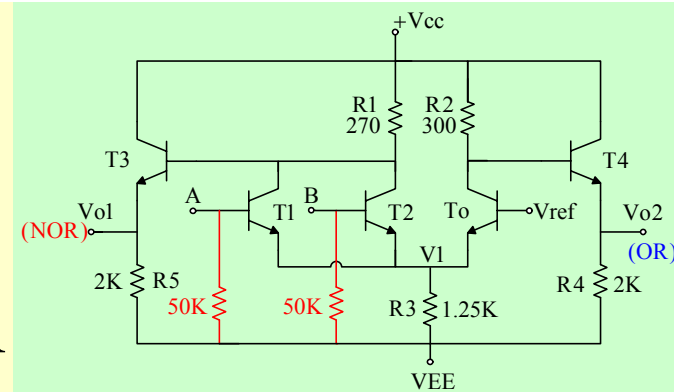
1) Input Low

$$I_{R3} = 2.64\text{mA}$$

$$I_{R5} = \frac{5.2 - 0.75}{R5} = 2.225\text{mA}$$

$$I_{R4} = \frac{5.2 - 1.55}{R4} = 1.825\text{mA}$$

$$P_{\text{dis}} = 5.2^{\text{V}} (2.64^{\text{mA}} + 2.225^{\text{mA}} + 1.825^{\text{mA}}) = 34.8\text{mW}$$



# ECL

## ► Pdis

### 2) Input High

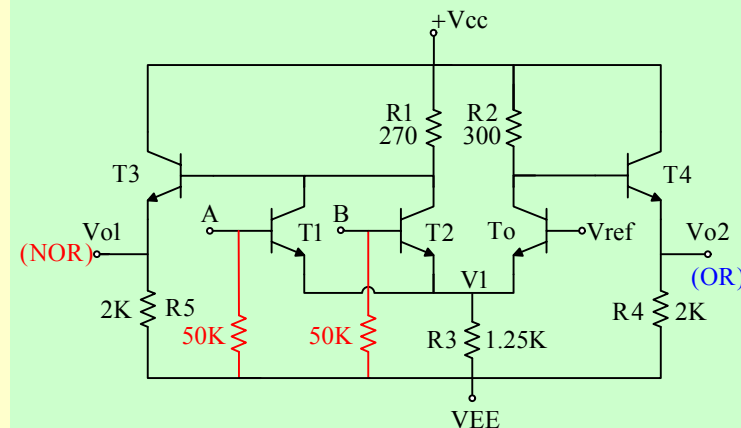
$$I_{R3} = 2.96\text{mA}$$

$$I_{R5} = 1.825\text{mA}$$

$$I_{R4} = 2.225\text{mA}$$

$$P_{\text{dis}} = 5.2^{\text{V}} (2.96^{\text{mA}} + 1.825^{\text{mA}} + 2.225^{\text{mA}}) = 36.4\text{mW}$$

$$\overline{P_{\text{dis}}} = \frac{1}{2} (36.4 + 34.8) = 35.6\text{mW}$$



# ECL

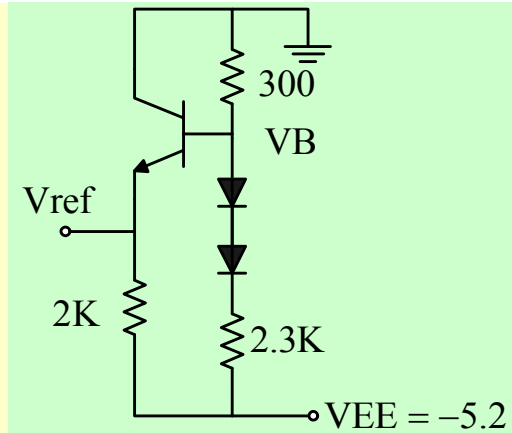
## ► Pdis (Vref)

$$I_{2K} = \frac{5.2 - 1.15}{2K} = 2.025\text{mA}$$

$$I_{2.3K} = \frac{5.2 - 1.4}{2.3K + 0.3K} = 1.46\text{mA}$$

$$P_{\text{disref}} = 5.2^V (2.025^{\text{mA}} + 1.46^{\text{mA}}) = 18.122\text{mW}$$

$$P_{\text{distot}} = 35.6^{\text{mW}} + 18.122^{\text{mW}} \approx 53.7\text{mW}$$



# ECL

## ▶ 10K Typical Characteristics

$V_{OH} / V_{OL}$	-0.9 / -1.7	FO	10
$V_{IH} / V_{IL}$	-1.2 / -1.4	Supply	-5.2V
$NM_H / NM_L$	0.3 / 0.3	PD	24mW
Logic Swing	0.8V	PDT	2n sec



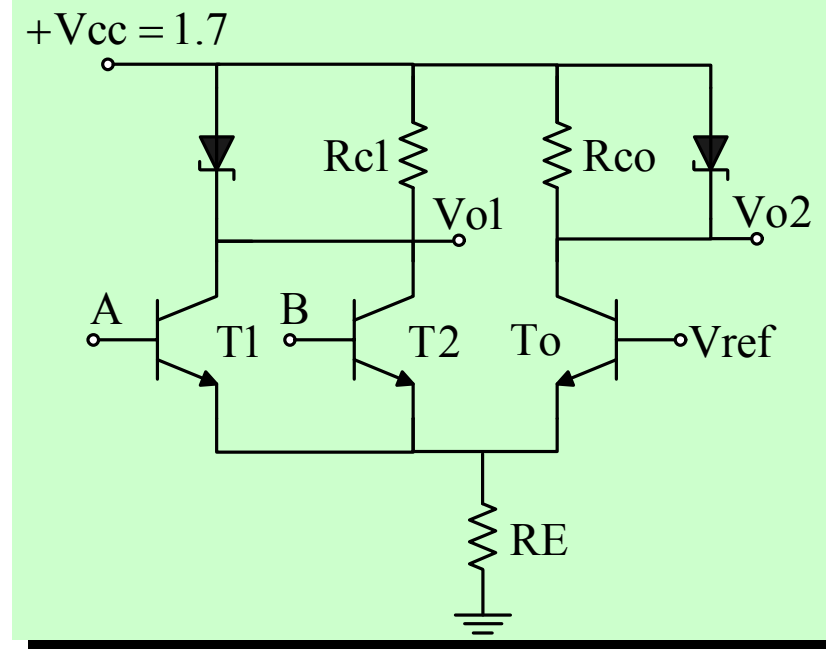
# ECL

## ► Better ECL (Positive Supply)

$$V_{OH} = 1.7V$$

$$V_{OL} = V_{CC} - 0.5 \text{V} \Big|_{\text{Platin Schottky Diode}} = 1.2V$$

$$V_{ref} = \frac{1}{2}(1.7V + 1.2V) = 1.45V$$



# ECL

---

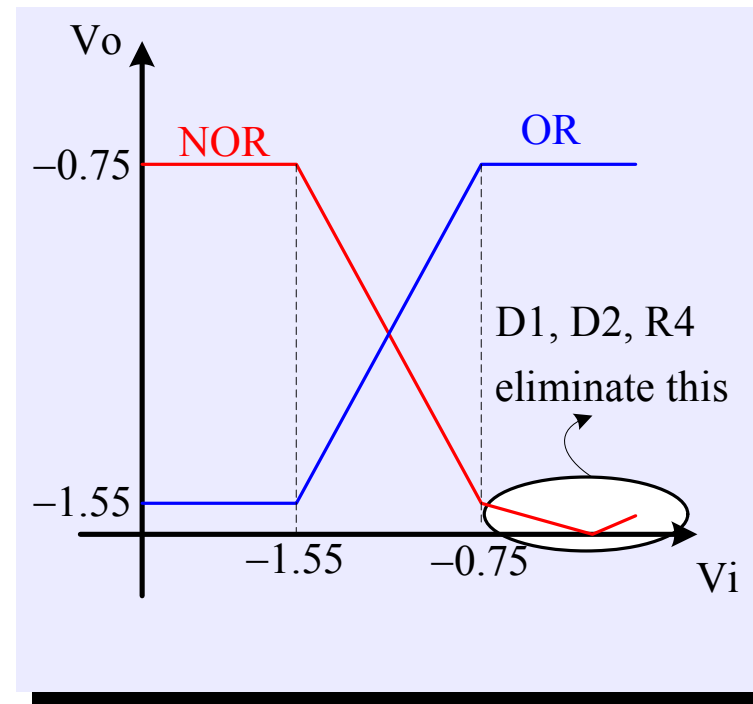
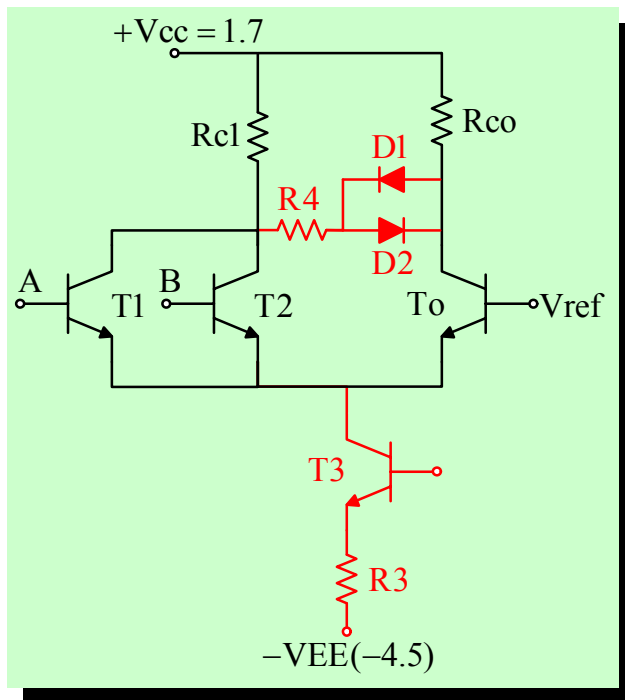
## ▶ 100K Series

- ▶ In ECL10K series the reference voltage is centered with respect to  $V_{OH}$  and  $V_{OL}$  even with changes of temperature
- ▶ However, the  $V_{ref}$  and output voltage levels do change with temperature, increasing as temperature increases
- ▶ In ECL100K series this problem is solved

# ECL

## ► 100K Series

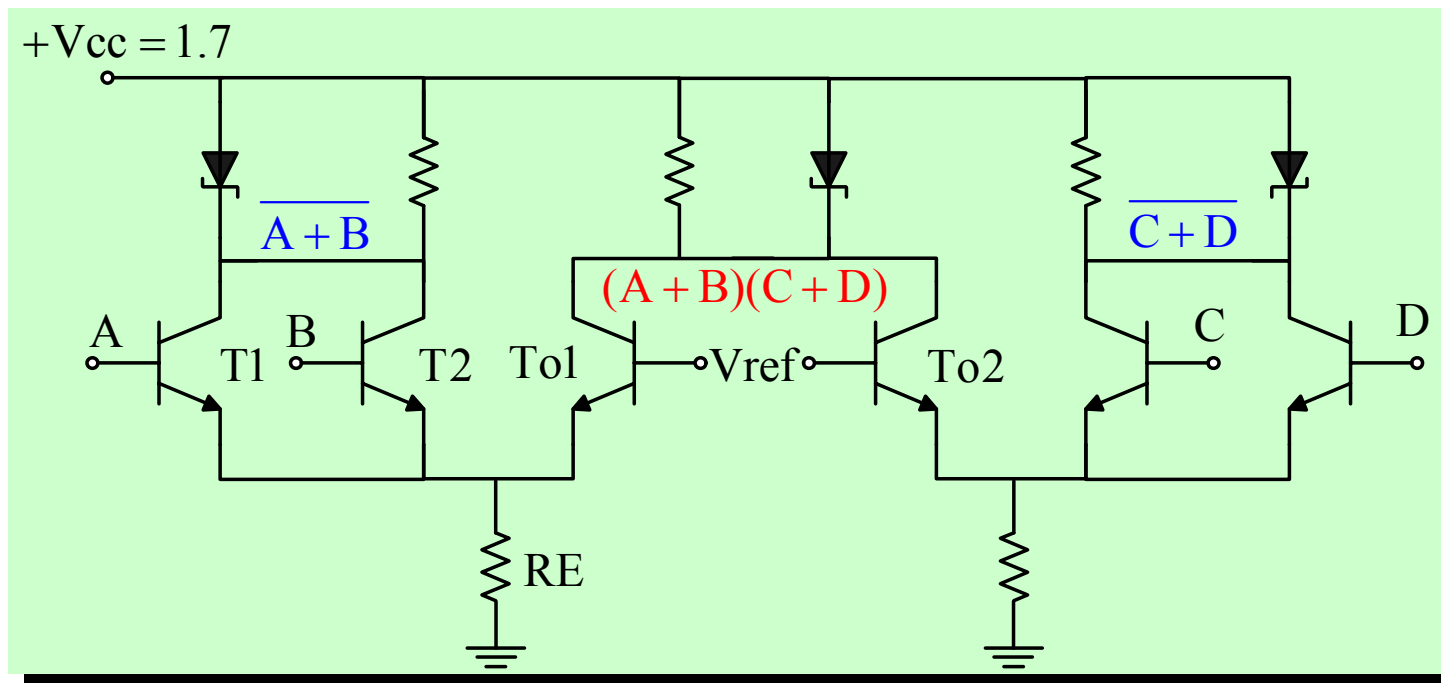
### ► D1, D2 and R4 eliminate the curvature in VTC



# ECL

## ► Combination in ECL

- To1, To2 have the same B,C therefore the area is small



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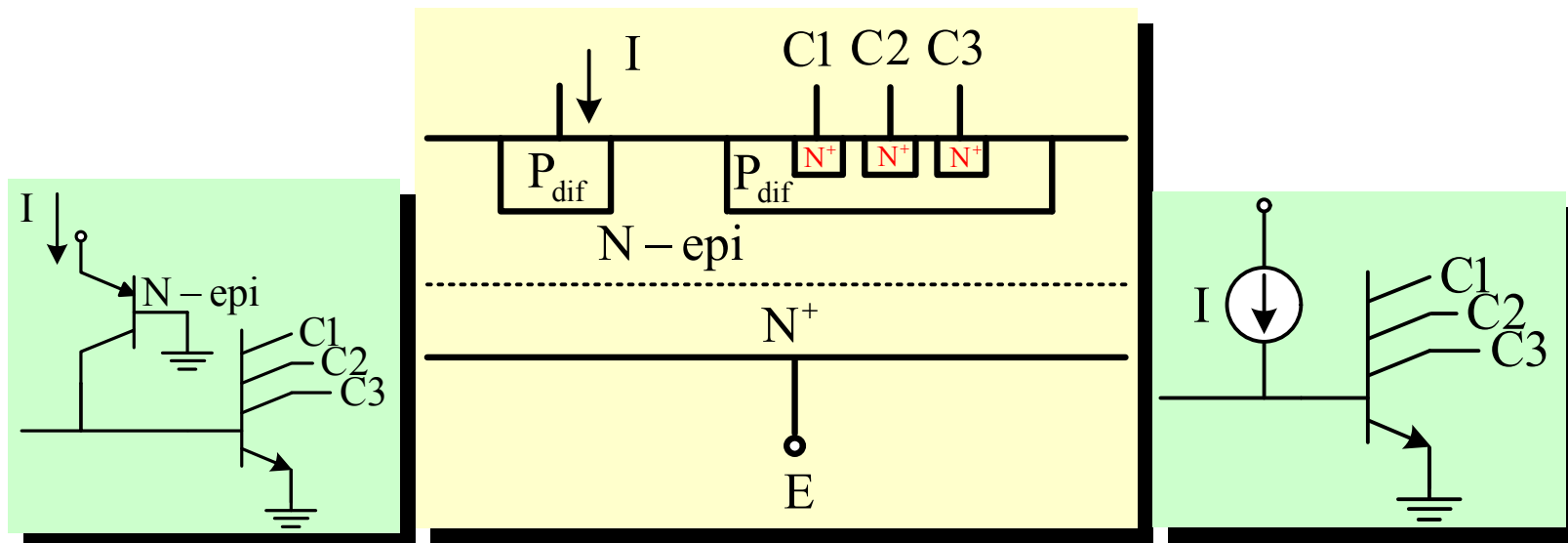
# Merged Transistor Logic

---

- ▶ **Minimal TTL Implementation to Reduce Number of Passive, Power Dissipating Components**
- ▶ **Integrated Injection Logic: I<sup>2</sup>L**
  - ▶ **Multiple collector NPN bipolar transistors**
  - ▶ **Can be “wire-or’d” to create all logic functions**

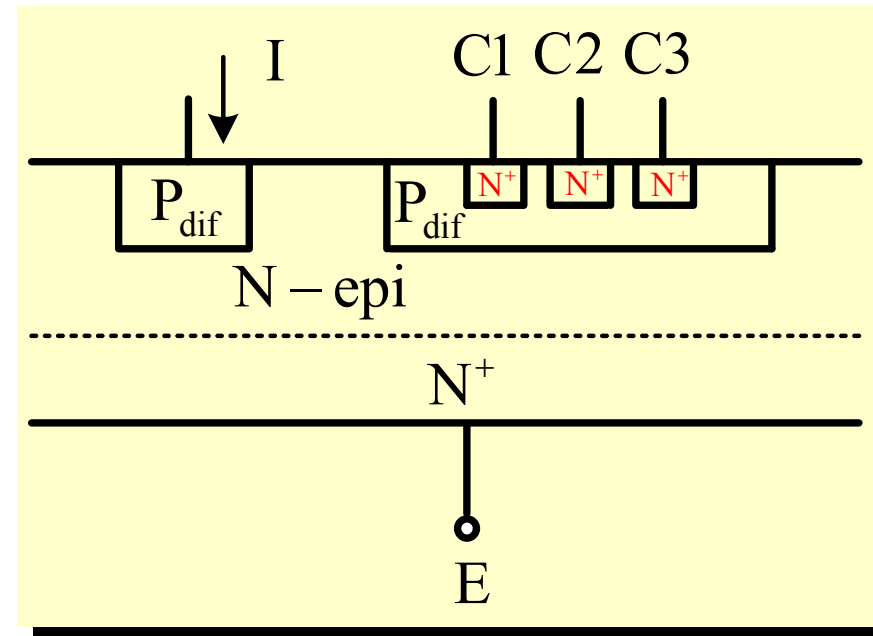
# I<sup>2</sup>L , MTL

- ▶ I<sup>2</sup>L=Integrate Injection Logic (Phillips)
- ▶ MTL=Merged Transistor Logic



# I<sup>2</sup>L , MTL

- ▶ Vertical NPN is not suitable because
- ▶ Collector N<sup>+</sup>
- ▶ Base Large
- ▶ Emitter N-epi





# I<sup>2</sup>L , MTL

## ► NM

$$0.9V \leq V_{cc} \leq 15V$$

$$\overline{V_{OH}} = \overline{V_{OH}} = 0.8V$$

$$\overline{V_{OL}} = 0.1V$$

$$\overline{V_{OL}} = 0.2V$$

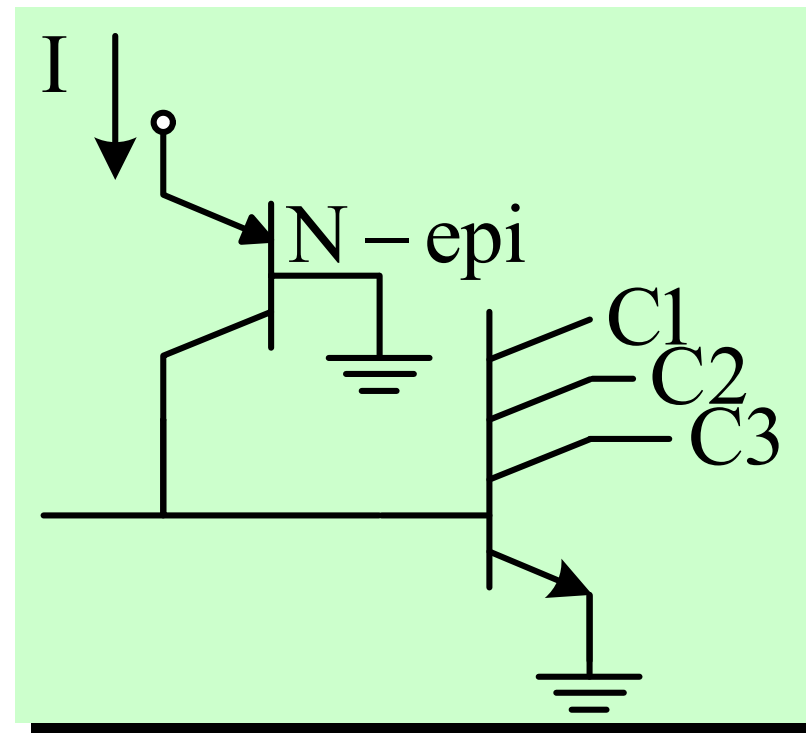
$\beta_{min}$  = is equal to no output collectors  
(for 5 outputs  $\beta_{min} = 5$ )

$$\overline{V_{IH}} = 0.7V$$

$$\overline{V_{IL}} = 0.5V$$

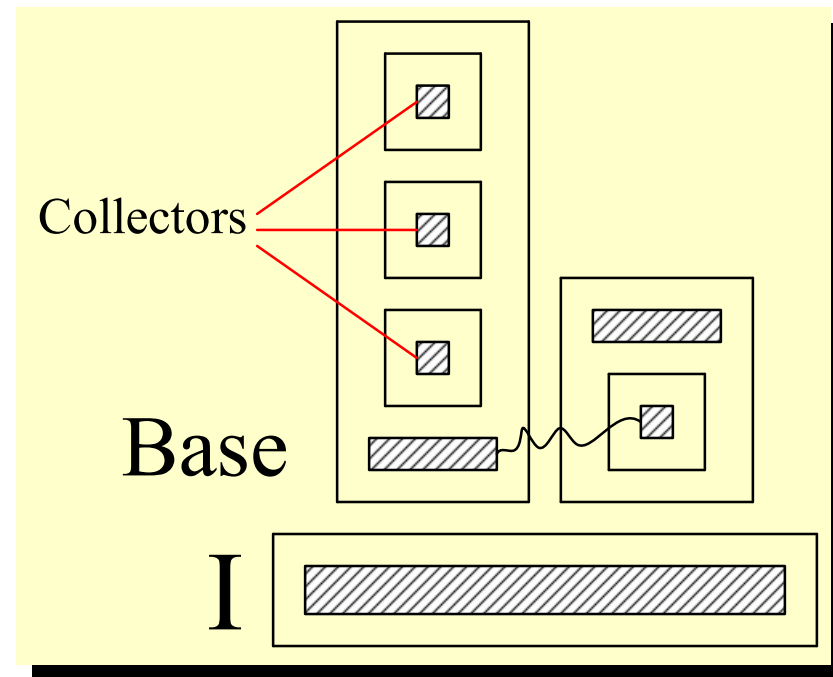
$$NML = \overline{V_{IL}} - \overline{V_{OL}} = 0.5V - 0.2V = 0.3V$$

$$NMH = \overline{V_{OH}} - \overline{V_{IH}} = 0.8V - 0.7V = 0.1V$$



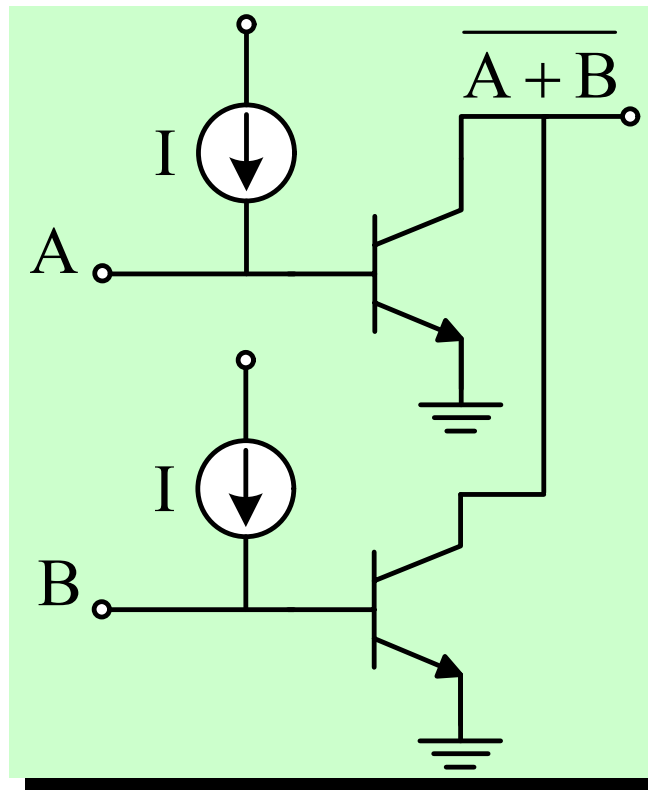
# I<sup>2</sup>L , MTL

- ▶ **Advantages:**
  - ▶ **Digital + Analog**
  - ▶ **PDP is close to CMOS**
  - ▶ **Small area**



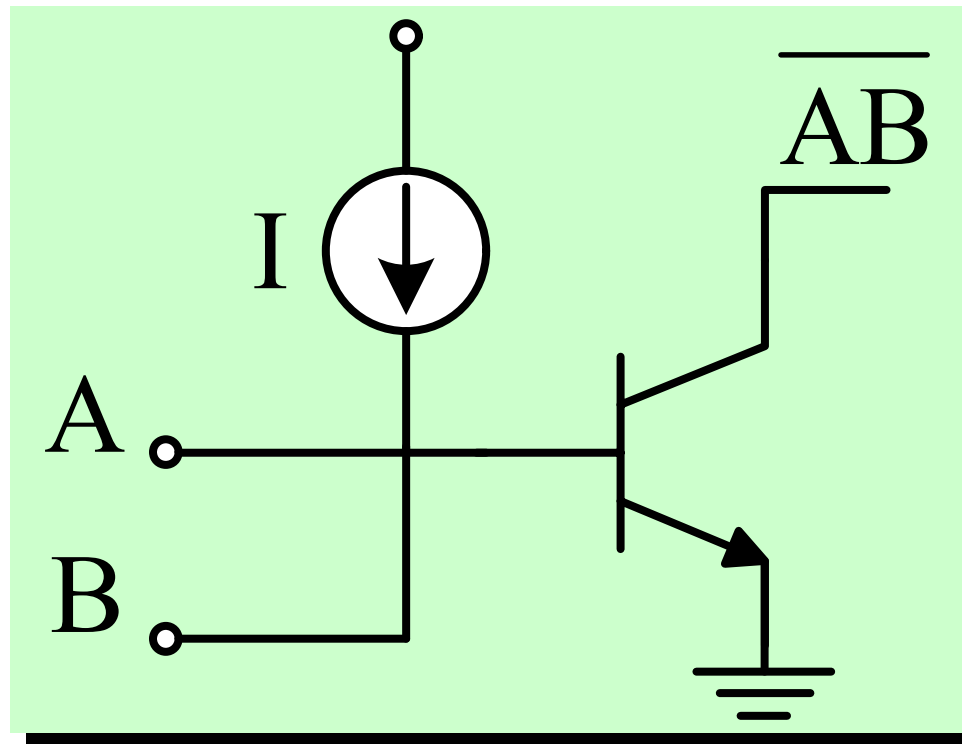
# I<sup>2</sup>L , MTL

## ► I<sup>2</sup>L NOR



# I<sup>2</sup>L , MTL

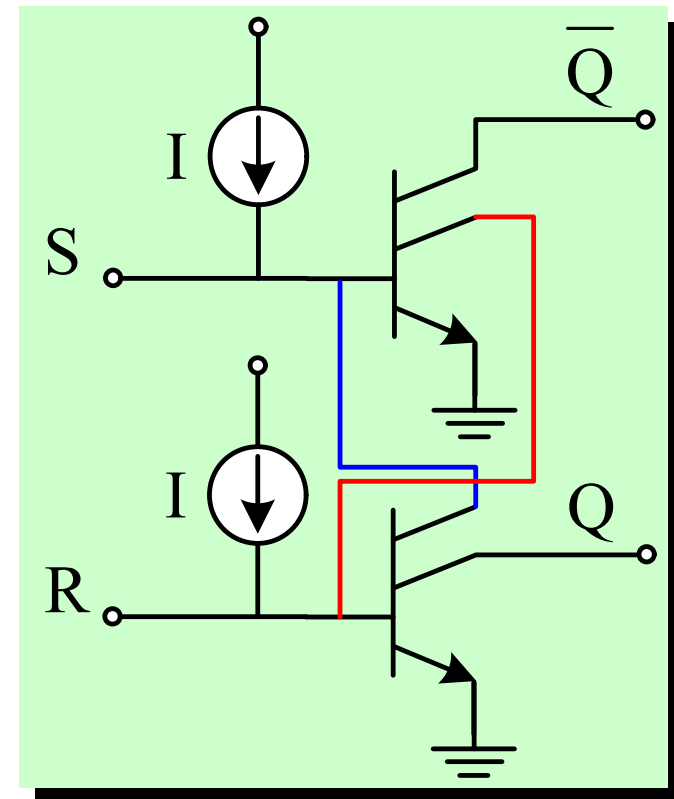
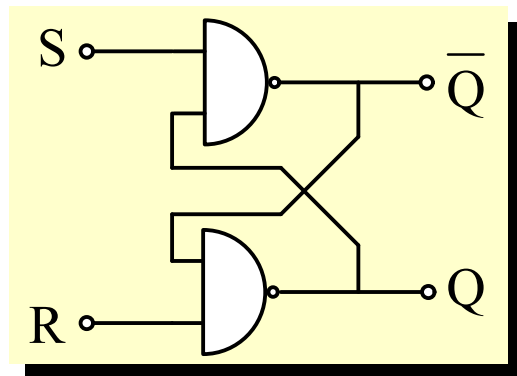
## ► I<sup>2</sup>L NAND



# I<sup>2</sup>L , MTL

## ▶ I<sup>2</sup>L FF

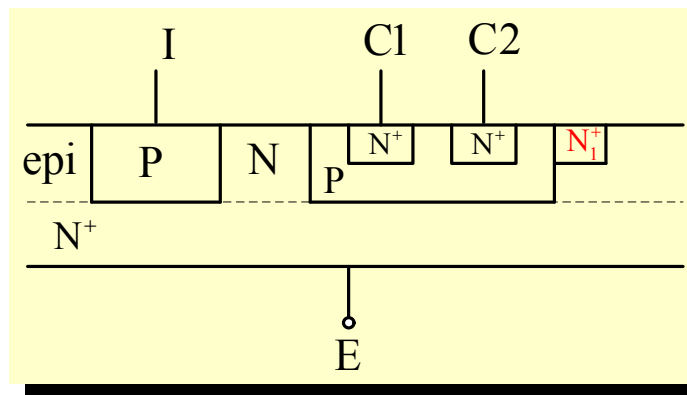
- ▶ The largest time constant is belong to Emitter (Emitter area is very large and delay is equal to time which need charge Emitter-Base cap. with I)



# I<sup>2</sup>L , MTL

## ▶ Better I<sup>2</sup>L

- ▶  $N_1^+$  is used in 3 sides (except left)
- ▶  $N_1^+$  → Increase Injection in Vertical →  $\beta \uparrow$
- ▶ We can not use schottky because we need N in collector
- ▶ I<sup>2</sup>L is slower than ECL by approximately 5

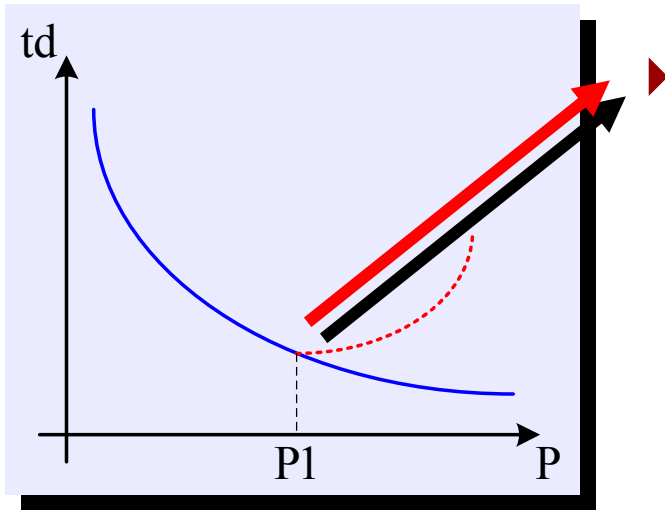


# I<sup>2</sup>L , MTL

## ► Delay Power

$$P = IV \approx IV_{BE}, \quad V_{CEsatPNP} \approx 0 \rightarrow V_{CC} \approx V_{BE}$$

$$Q = CV_{BE} = It \Rightarrow t = \frac{C}{I} V_{BE} \rightarrow Pt_d = CV_{BE}^2 = Cte$$

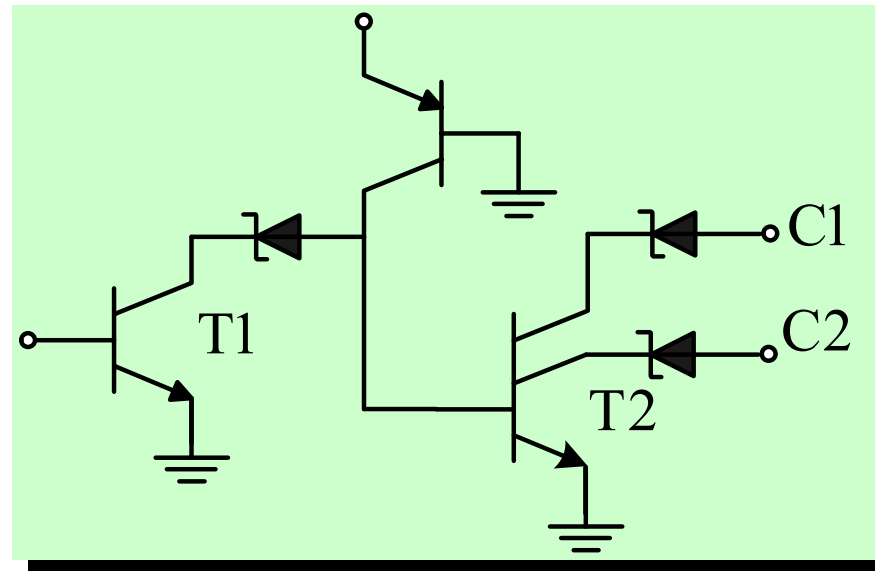


► From this point the Excess current is large then in delay calculation, the storage time must be calculated

# I<sup>2</sup>L , MTL

## ► Faster I<sup>2</sup>L

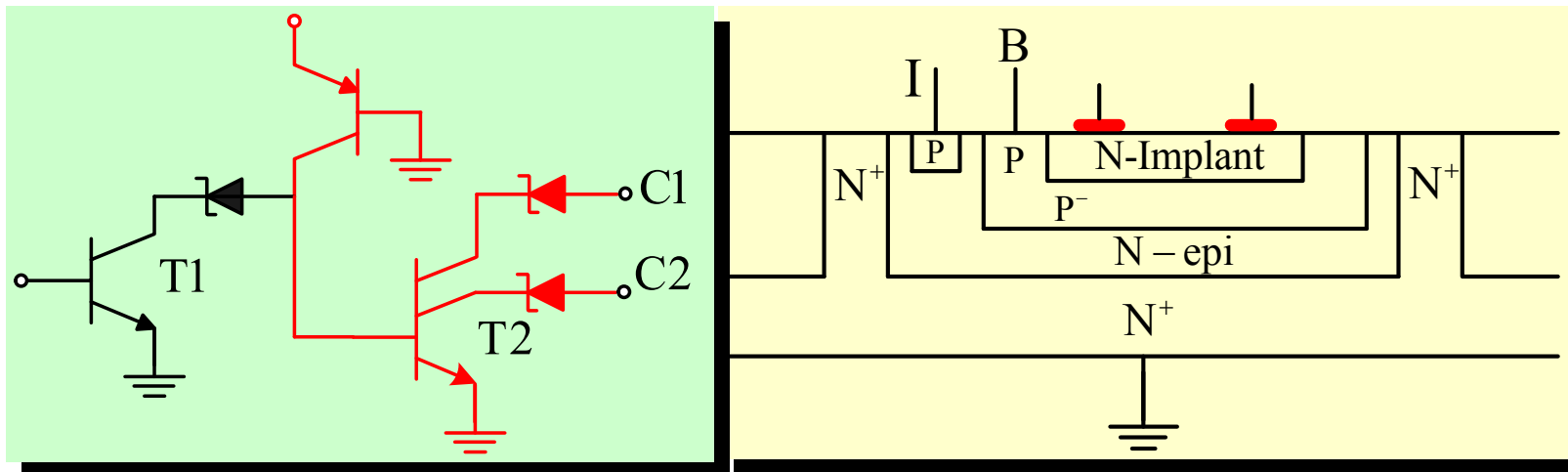
- If we change  $\Delta V_{BE}$  to a lower value the Gate become faster
- By a Schottky on collector of T1,  $\Delta V_{BE}=0.7-0.5=0.2V$
- This reduces NM





# I<sup>2</sup>L , MTL

## ► Faster I<sup>2</sup>L



# I<sup>2</sup>L , MTL

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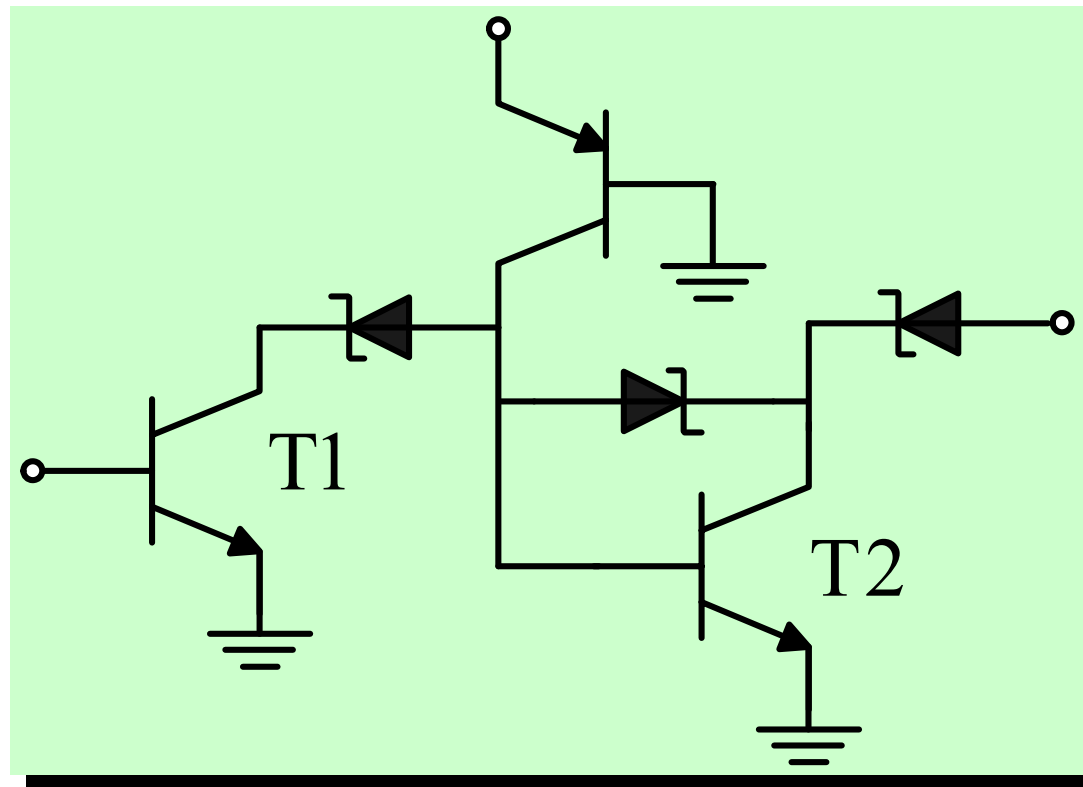
- ▶ **Faster I<sup>2</sup>L (Other Idea)**
  - ▶ Schottky is used for T2
  - ▶ We have Large  $V_{CEsat}$  and then it is very difficult to design a Gate , because  $V_D + V_{CEsat}$  not to be reached to  $V_{BE}(0.7)$
  - ▶ The Metal for schottky will be very important for reduction of barrier potential, usually the mixture of Si and Pt is used

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# Schottky Transistor Logic (STL)



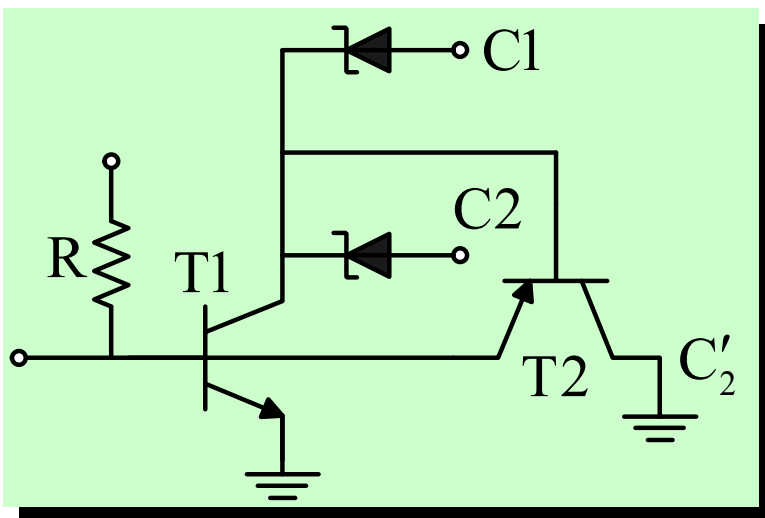
# Contents

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# Integrated Schottky Logic (ISL)

- ▶ We use resistor for PNP
- ▶ Only in this configuration the Emitter junction is on the top



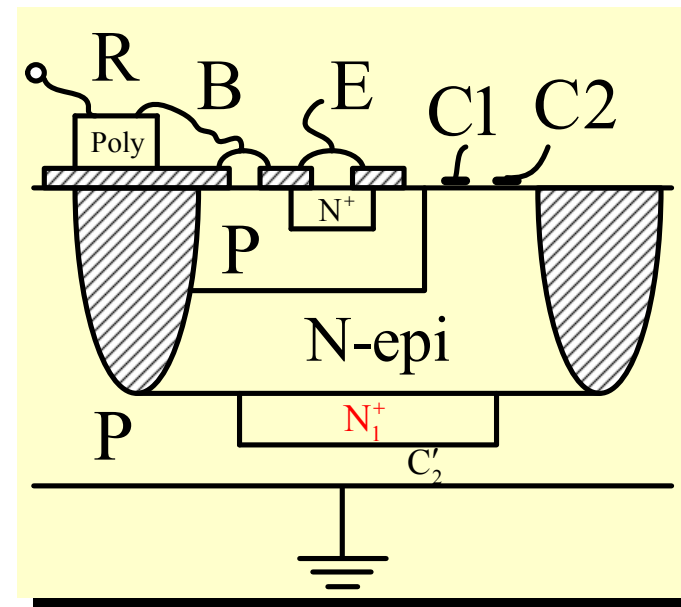
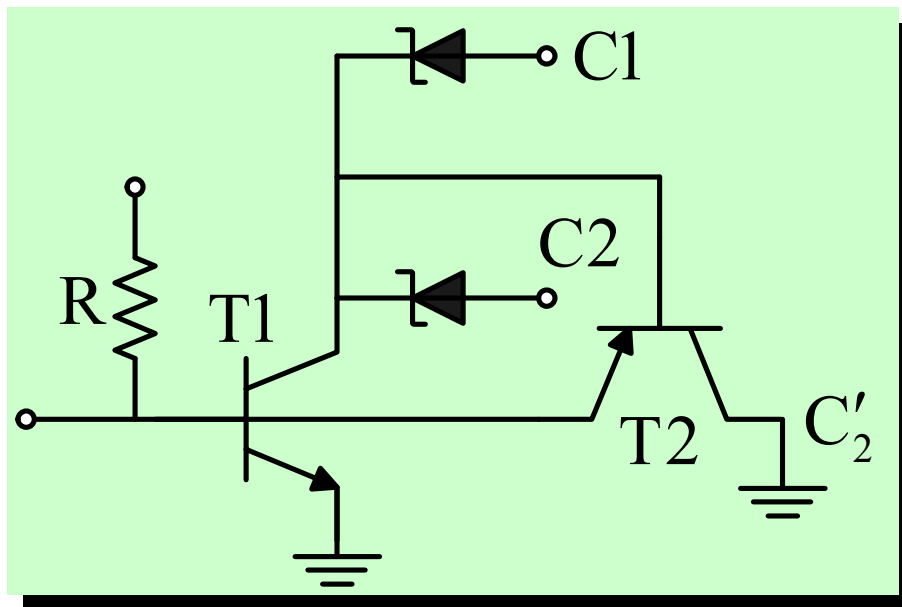
$$V_{\text{CBT1sat}} = 0.7\text{V}$$

$$V_{\text{EBT2}} = 0.6\text{V} < V_{\text{CBT1}}$$

$\Rightarrow$  { PNP  $\rightarrow$  Prevents NPN to saturate  
NPN  $\rightarrow$  Prevents PNP to saturate }  $\Rightarrow$  Higher Speed

# ISL

- ▶  $N^+_1$  is used for lowering the ohmic junction of collector
- ▶ It covers the large area of Base Then  $\beta_{PNP} \downarrow$



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# Compatibility of Logic Families

---

- ▶ **Common ground, common supply voltage, and TTL input and output levels**
- ▶ **Common ground, common supply voltage, CMOS inputs, and TTL outputs**
- ▶ **Common ground, common supply voltage, TTL inputs, and CMOS outputs**
- ▶ **Common ground, different Supply voltage levels**
- ▶ **Dynamic interface issues**

# Compatibility of Logic Families

---

- ▶ **Common GND, Different Supply Voltage**
  - ▶ **Low-voltage device for interface to TTL level I/O 5V logic devices**
    - Low voltage BiCMOS LVT, CMOS LVC, LVQ, FCT3, etc
  - ▶ **Cautions**
    - **3.3V to 5V logic interface**
      - In general, no problem
    - **5V to 3.3V logic interface**
      - Must have no **an electrostatic protection network** (a diode or diodes) at the inputs of 3.3V devices to prevent excessive current

# Compatibility of Logic Families

---

- ▶ **Dynamic Interface Issues**
  - ▶ **When logic families are mixed**
    - **Dynamic and static interface compatibility**
    - **Timing problem by mixing slow and fast devices**
      - **Holding time violation** by fast-edge to slow-edge logic interface
        - » In synchronous systems, signals originating from fast devices may go away before they can be captured by slow devices

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- ▶ Diode Logic (DL)
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- ▶ Noise Margins of Logic Families
- ▶ Summary

# Noise Margins of Logic Families

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- ▶ **What is the Noise margin?**
  - ▶ **Difference between the worst-case output levels and the worst-case input levels**
- ▶ **Static and Dynamic noise margins**
  - ▶ **Static noise margin: low-frequency safety margins**
  - ▶ **Dynamic noise margin: sensitivity of logic devices to noise spikes**
    - **It is less than that of older logic families because of designing for high-speed operation**

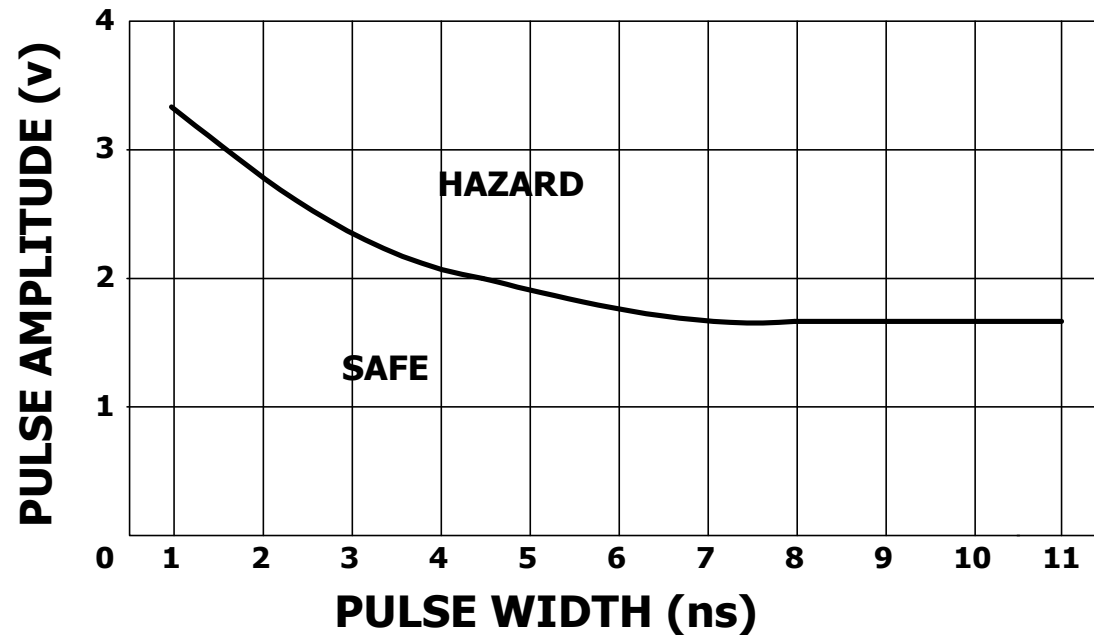
# Noise Margins of Logic Families

## ► Static Noise margin

Family	Input levels, V		Output levels, V	
	$V_{IL\ MAX}$	$V_{IH\ MIN}$	$V_{OL\ MAX}$	$V_{OL\ MIN}$
ABT	0.8	2.0	0.55	2.5
AC	1.35	3.15	0.1	4.4
ACT	0.8	2.0	0.5	3.7
AC11	1.35	3.15	0.1	4.4
ACT11	0.8	2.0	0.5	3.7
ALS	0.8	2.0	0.5	2.4
AS	0.8	2.0	0.55	2.4
FAST	0.8	2.0	0.55	2.4
FCT	0.8	2.0	0.55	2.4
FCT3	0.8	2.0	0.5	2.4
BC	0.8	2.0	0.5	2.5
BCT	0.8	2.0	0.55	2.4
LVQ	0.8	2.0	0.5	2.4
LVT	0.8	2.0	0.5	2.4

# Noise Margins of Logic Families

- ▶ Dynamic Noise margin
  - ▶ Low state pulse rejection characteristic of IDT FCT244



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# Summary

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- ▶ In this lecture the development of Digital IC specially bipolar gate circuit is described. Specially described in detail are:
  - ▶ RTL
  - ▶ DTL
  - ▶ TTL including:
    - Standard TTL
    - Schottky Clamped (S)
    - Low Power Schottky (LS)
    - Advanced Schottky (AS)
    - Advanced Low Power Schottky (ALS)
  - ▶ ECL
  - ▶ I<sup>2</sup>L
  - ▶ STL
  - ▶ ISL