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**Electrical Engineering Department**

**ENEE4104**

**ENGINEERING SIMULATION LAB**

**Experiment #1 Prelab**

**Negative feedback, Modular design and sub-circuits using Orcad**

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**Abstract:**

The aims of prelab was to simulate both circuits open loop multistage amplifier and closed loop multistage amplifier, using Orcad, determined Avmid “Gain”, Zin, Zout and Bandwidth of both circuits, repeatrd the simulation with the load values: 10kΩ to 100Ω and compared the two amplifiers’ results with both load values.

Table of figures

[Figure 1:The open loop multistage amplifier 3](#_Toc496777551)

[Figure 2:Simulation Setting 3](#_Toc496777552)

[Figure 3: The Gain of the CKT 1 4](#_Toc496777553)

[Figure 4: The Gain of the CKT 1to determine the Bandwidth 4](#_Toc496777554)

[Figure 5:The input impedance Zin for CKT1 5](#_Toc496777555)

[Figure 6:CKT 1 to find the output impedance 5](#_Toc496777556)

[Figure 7:The output impedance for CKT 1 6](#_Toc496777557)

[Figure 8:CKT 1 for repeated load values 6](#_Toc496777558)

[Figure 9:Simulation Setting2 7](#_Toc496777559)

[Figure 10:The Gains for load values: 10kΩ to 100Ω, and step 400 Ω 7](#_Toc496777560)

[Figure 11:The input impedance variable load 8](#_Toc496777561)

[Figure 12:The output impedance for variable load 8](#_Toc496777562)

[Figure 13:The closed loop multistage amplifier 9](#_Toc496777563)

[Figure 14:The Gain of the CKT 2 9](#_Toc496777564)

[Figure 15:The Gain of the CKT 2to determine the Bandwidth 10](#_Toc496777565)

[Figure 16:The input impedance Zin for CKT2 10](#_Toc496777566)

[Figure 17:CKT 2 to find the output impedance 11](#_Toc496777567)

[Figure 18:The output impedance for CKT 1 11](#_Toc496777568)

[Figure 19:The Gains for load values: 10kΩ to 100Ω, and step 400 Ω 12](#_Toc496777569)

[Figure 20:The input impedance variable load 12](#_Toc496777570)

[Figure 21:The output impedance for variable load 13](#_Toc496777571)

Part 1: **Open Loop Multistage Amplifier**

The open loop multistage amplifier was drowned and simulated using ORCAD as shown in figure 1.



Figure 1:The open loop multistage amplifier

The ORCAD was setup on AC Sweep as shown in figure 2.



Figure 2:Simulation Setting

The Gain, Zin, Zout and Bandwidth were determined for the circuit 1 as follow:

1. The Gain was determined Form the output plot as shown in figure 3

 The Gain=131.650V



Figure 3: The Gain of the CKT 1

1. To determine the Bandwidth the cut of frequency fc was found as follow:

Fc is at( $\sqrt{2}$ \* Gain)

Amp at fc =93.09 V

 The Bandwidth=176.6KHz



Figure 4: The Gain of the CKT 1to determine the Bandwidth

1. The input impedance Zin is shown in Figure 5:

Zin=Vin/Iin

Zin=8.83k Ω



Figure 5:The input impedance Zin for CKT1

1. To find the output impedance, the input voltage was shorted, and the load was replaced by the input voltage V1 as shown in figure 6.



Figure 6:CKT 1 to find the output impedance

 The output impedance is shown in Figure 7

 Zout=600 Ω



Figure 7:The output impedance for CKT 1

1. The simulation was repeated for the load values: 10kΩ to 100Ω, and step 400 Ω as shown is figures:



Figure 8:CKT 1 for repeated load values



Figure 9:Simulation Setting2

The Gains for load values: 10kΩ to 100Ω, and step 400 Ω. As we shown, when RL decrease the gain decrease, but the bandwidth doesn’t change and remain constant.



Figure 10:The Gains for load values: 10kΩ to 100Ω, and step 400 Ω

The input impedance for variable load, when RL changed the input impedance doesn’t change, remain constant Zin=8.3k Ω



Figure 11:The input impedance variable load

The output impedance for variable load, when RL changed the input impedance doesn’t change, remain constant Zout=600 Ω



Figure 12:The output impedance for variable load

Part 2: **Closed Loop Multistage Amplifier**

The closed loop multistage amplifier was drowned and simulated using ORCAD as shown in figure 13.



Figure 13:The closed loop multistage amplifier

The Gain, Zin, Zout and Bandwidth were determined for the circuit 2 as follow:

1. The Gain was determined Form the output plot as shown in figure 13

 The Gain=9.240V



Figure 14:The Gain of the CKT 2

1. To determine the Bandwidth the cut of frequency fc was found as follow:

Fc is at( $\sqrt{2}$ \* Gain)

Amp at fc =6.533 V

 The Bandwidth=3.284MHz



Figure 15:The Gain of the CKT 2to determine the Bandwidth

Zin

1. The input impedance Zin is shown in Figure 5:

Zin=Vin/Iin

Zin=116.56k Ω



Figure 16:The input impedance Zin for CKT2

1. To find the output impedance, the input voltage was shorted, and the load was replaced by the input voltage V1 as shown in figure 17.



Figure 17:CKT 2 to find the output impedance

The output impedance is shown in Figure 18.

 Zout=1.0817 Ω



Figure 18:The output impedance for CKT 1

1. The simulation was repeated for the load values: 10kΩ to 100Ω, and step 400 Ω as shown is figures:

The Gains for load values: 10kΩ to 100Ω, and step 400 Ω. As we shown,when RL decrease the gain decrease but it is smaller than in open amplifier, also the bandwidth doesn’t change,remain constant.



Figure 19:The Gains for load values: 10kΩ to 100Ω, and step 400 Ω

The input impedance for variable load, when RL changed when RL decreased the input impedance decreased.



Figure 20:The input impedance variable load

The output impedance for variable load, when RL changed the input impedance doesn’t change, remain constant Zout=1.08 Ω



Figure 21:The output impedance for variable load