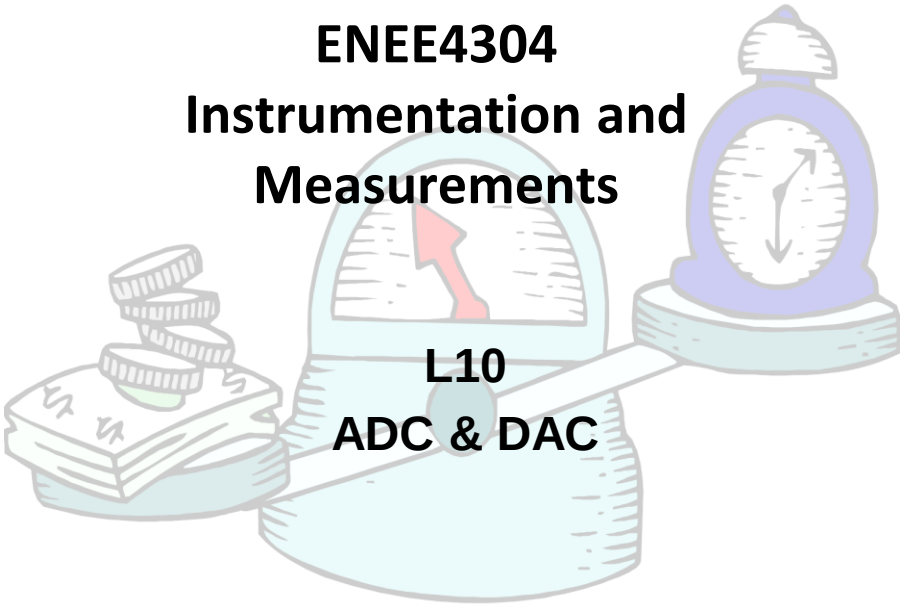
ENEE4304
Instrumentation and Measurements



L10
ADC & DAC

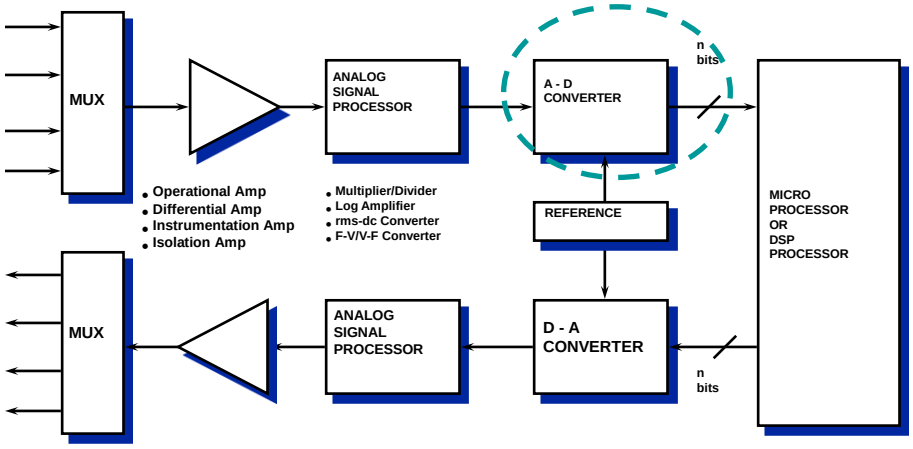
Outline

- Digital Signal Processing:
- Sampling;
- Sample and Hold;
- Analog to Digital Conversion;
- Digital to Analog Conversion.

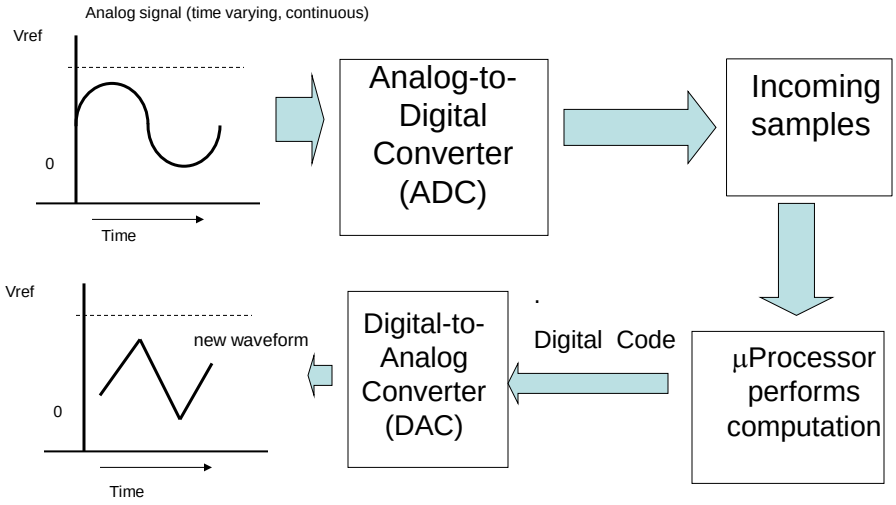
Introduction

- Most Instrumentation systems include a digital processing device (PC, Microprocessor, DSP, Microcontroller….)
- These devices require information in digital format (binary, grey code, signed 2's complement , BCD…..etc)
- This requires some form of digitizer, or *analog-to-digital converter (ADC)*
- An ADC converts real-world signals (usually voltages) into digital numbers so that a computer or digital processor can (1) acquire signals automatically, (2) store and retrieve information about the signals, (3) process and analyze the information, and (4) display measurement results.

The Measurement & Control Loop



Digital Signal Processing



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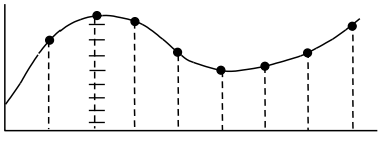
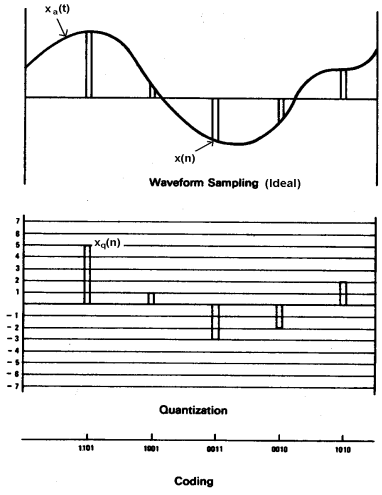
- A digitizing system can do these jobs with greater speed, reliability, repeatability, accuracy, and resolution than a purely analog system normally can.
- The two main functions of an ADC are *sampling* and *quantization*
- These two processes convert analog signals into digital numbers having discrete amplitudes, at discrete times.
- To represent changing signals at every instant in time or at every possible voltage would take an infinite amount of storage.

ADC SAMPLED AND QUANTIZED WAVEFORM



Analog, Discrete, Digital Signals

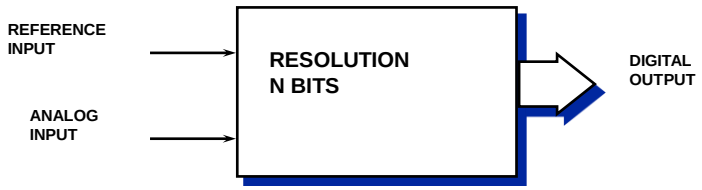


- **Analog, x(t)**
  - Continuous Amplitude
  - Continuous Time
- **Discrete, x(n)**
  - Continuous Amplitude
  - Discrete Time
- **Digital, $x_q(n)$**
  - Discrete Amplitude
  - Discrete Time

Introduction

- So for every system there is an appropriate *sampling rate* And degree of quantization (*resolution*) so that the system retains as much information as it needs about the input signals while keeping track of manageable amounts of data.
- Ultimately, the purpose of sampling and quantization is to reduce as much as possible the amount of information about a signal that a system must store in order to reconstruct or analyze it meaningfully.

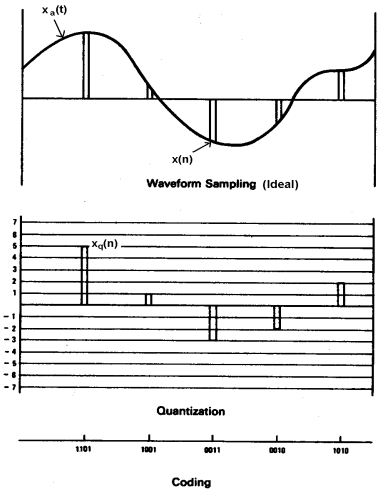
What is an Analog-Digital Converter?



- Produces a Digital Output Corresponding to the Value of the Signal Applied to Its Input Relative to a Reference Voltage
- Finite Number of Discrete Values : 2^N Resulting in Quantization Uncertainty
- Changes Continuous Time Signal into Discrete Time Sampled Representation
- Sampling and Quantization Impose Fundamental yet Predictable Limitations

Sampling & Quantization

- To prevent having to digitize an infinite amount of information, an analog signal must first be sampled.
- **Sampling is the process of picking one value of a signal to represent the signal for some interval of time.**
- Sampling can be done at regular (constant) rate or not.



Sampling

- Sampling is done by a circuit called a *sample-and-hold (S/H)* , which, at a sampling instant, transfers the input signal to the output and holds it steady, even though the input signal may still be changing.
- Most modern ADC chip has a built-in S/H or T/H, and virtually all data acquisition systems include them.
- Of course, sampling necessarily throws away some information, so the art of sampling is in choosing the right sample rate so that enough of the input signal is preserved.

Minimum sampling rate (Nyquest Rate)

- Nyquest criterion states that the sampling rate must be at least twice the highest frequency of the signal of interest:

$$f_{sampling} > 2f_{signal}$$

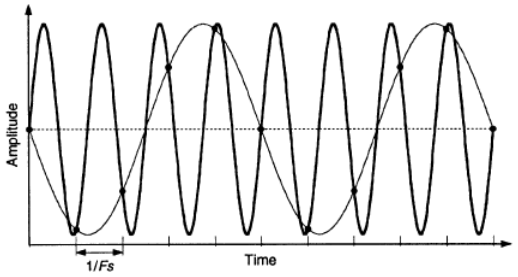
- Nyquest criterion guarantees the preservation of the frequency content of the signal, but not the time dependency
- In order to be able to reconstruct the signal in time domain, as a rule of thump , we use : fsampling > 10 f signal
- Aliasing occurs when the sampling is done at a rate less than Nyquest rate
- Sample rates are specified in samples/s, or S/s, and it is also common to specify rates in kS/s, MS/s, and even GS/s.

Minimum sampling rate (Nyquest Rate)

- Sample rates are specified in samples/s, or S/s, and it is also common to specify rates in kS/s, MS/s, and even GS/s.
- It is not always necessary to worry about aliasing.
- When an instrument is measuring slow-moving dc signals or is gathering data for statistical analysis, for instance, getting frequencies right is not important.

aliasing

- In those cases we choose the sample rate so that we can take enough data in a reasonable amount of time.



Antialias Filter

- On the other hand, if the instrument is a spectrum analyzer, where frequency does matter, or an oscilloscope, where fine time detail is needed, aliasing certainly is an issue.
- When aliased signals from beyond the frequency band of interest can interfere with measurement, an instrument needs to have an *anti-alias filter* before the S/H.
- An anti-alias filter is a low-pass filter with a gain of 1 throughout most of the frequency band of interest.
- As frequency increases, it begins to attenuate the signal; by the Nyquist frequency it must have enough attenuation to prevent higher-frequency signals from reaching the S/H with enough amplitude to disturb measurements.

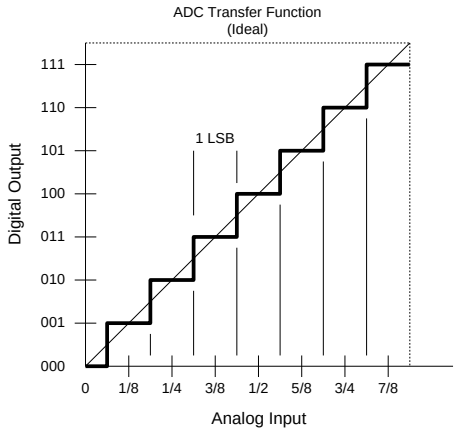
Antialias Filter

- An efficient antialias filter must attenuate rapidly with frequency in order to make most of the baseband usable.
- Popular analog filters with rapid cutoff include elliptic and Chebyshev filters, which use zeros to achieve fast cutoff, and Butterworth filters (sixth order and above), which do not attenuate as aggressively, but have very flat passband response.
- Some ADCs do not need a S/H at all.
- If the ADC is converting a slow-moving or dc signal and precise timing isn't needed, the input may be stable enough during conversion that it is as good as sampled.
- There are also *integrating ADCs* (discussed later), which average the input signal over a period of time rather than sampling it.
- However, internally they actually sample the average.

Quantization

- What sampling accomplishes in the time domain, quantization does in the amplitude domain.
- The process of digitization is not complete until the sampled signal, which is still in analog form, is reduced to digital information.

- Figure represents a three-bit quantizer, which maps a continuum of analog input values to only eight (2^3) possible output values.
- Each step in the staircase has (ideally) the same width along the *x* -axis, which we call *code width* and define as 1*LSB (least significant bit)*
- In this case 1 LSB is equal to 1/8 V. Each digital code corresponds to one of eight 1-LSB intervals making up the analog input range, which is 8 LSB (and also 1 V in this case).



ADC Specifications

1. Range: The input range of ADC is the span of voltage over which the ADC can make conversion

- The end points at the bottom and the top of the range are called *–full-scale* and *+ full-scale* , respectively.
- When –full-scale = 0 V the range is called ***unipolar***
- when **–full-scale** is a negative voltage of the same magnitude as **+full-scale** the range is said to be ***bipolar***
- When the input voltage exceeds the input range, the conversion data are certain to be wrong, and most ADCs report the code at the end point of the range closest to the input voltage.
- This condition is called an ***overrange***

- $Range = V_{FSR} = +Full\ Scale\ -(-Full\ Scale)$
- For Example : Unipolar 0 to 15 V

  Range=15-0=15V
- Bipolar : -5V to +5V

  Range =5-(-5)=10 V

ADC Specifications

2)The resolution

- **The resolution of an ADC is the smallest change in voltage the ADC can detect, which is inherently 1 LSB**.
- It is customary to refer to the resolution of an ADC by the number of binary bits or decimal digits it produces; for example, “12 bits” means that the ADC can resolve one part in 2 ^12 (= 4096).
- In the case of a digital voltmeter that reads decimal digits, we refer to the number of digits that it resolves.
- A “6-digit” voltmeter on a 1 V scale measures from

–0.999999 V to +0.999999 V in 0.000001 V steps; it resolves one part in 2 000 000. It is also common to refer to a voltmeter that measures from –1.999999 to +1.999999 as a “6 ½digit” voltmeter.

- Resolution of ADC is the smallest detectable change in voltage ; however some refer to number of bits as resolution
- $\Delta = LSB = Q = \frac{V_{FSR}}{2^n}$
- Example : 8 bit ADC with 0-2.5 V input

$\Delta = LSB = Q = \frac{2.5}{2^8} = \frac{2500mV}{256}$=9.765 mV

Or as % $\Delta = \frac{9.765}{2500} * 100\% = 0.3906\%$

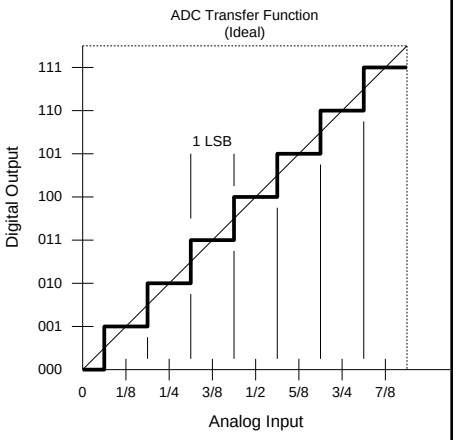
ADC Resolution vs. Quantization Parameters

Resolution, Bits (n)	2^n	LSB, mV (2.5V FS)	% Full Scale	ppm Full Scale	dB Full Scale
8	256	9.77	0.391	3906	-48.0
10	1024	2.44	0.098	977	-60.0
12	4096	0.610	0.024	244	-72.0
14	16,384	0.153	0.006	61	-84.0
16	65,536	0.038	0.0015	15	-96.0
18	262,164	0.0095	0.00038	3.8	-108.0

- Higher n gives better resolution

DC Specifications (Ideal-midtread linear type)

- 3 bit, 0-1 V range
- There are 2^3 codes.
- For this 3-bit ADC,
- 1 LSB = (1V/2^3 = 1/8th)
- Each “step” is centered on an eighth of full scale
- $ADC_{CODE} = Round\left(\frac{2^n}{V_{FSR}}.Vin\right)$



Example

- A 5 bit ADC with a 0-5V input range have a 3.127V input signal at its input,
- what is the output binary code at the output?
- Solution:
- $ADC_{CODE} = Round\left(\frac{2^5}{5}.3.127\right)$=$(20)_{10}$
- $(20)_{10}$ =$(10100)_2$

Example

- Given a sensor with 0.02 V / degree C sensitivity, choose an a suitable size ADC with V_{FSR}=2V such that to be able to measure 0-100 deg C with :

a) 1 deg C resolution

b) 0.1 $\deg C$ resolution

- **Solution:**
- A) 1 deg C => 0.02 V
- 100 deg C => 100x 0.02=2V
- We have an ADC with V_{FSR}= 2 V range
- For 1 deg C resolution , ADC resolution Δ = 0.02 V
- $\Delta = 0.02V = \frac{V_{FSR}}{2^n} = \frac{2}{2^n} \Rightarrow 2^n$=100==> n =$\log_2$(100)=6.644
- N must be an integer, so we choose n=7

Example

- B) For 0.1 deg C resolution , ADC resolution Δ = 0.002 V
- $\Delta = 0.002V = \frac{V_{FSR}}{2^n} = \frac{2}{2^n} \Rightarrow 2^n$=1000==> n =$\log_2$(1000)=9.97
- N must be an integer, so we choose n=10

- **In this example , the sensor output is matched to ADC input**

Example: ADC range 5 V

(not matched by sensor output "2V")

- **Solution:**
- 1 deg C => 0.02 V
- 100 deg C => 100x 0.02=2V
- Suppose we have an ADC with V_{FSR}= 5 V range
- For 1 deg C resolution , ADC resolution Δ = 0.02 V
- $\Delta = 0.02V = \frac{V_{FSR}}{2^n} = \frac{5}{2^n} \Longrightarrow 2^n$=250==> n =$\log_2$(250)=7.96
- N must be an integer, so we choose n=8
- For 0.1 deg C resolution , ADC resolution Δ = 0.002 V
- $\Delta = 0.002V = \frac{V_{FSR}}{2^n} = \frac{5}{2^n} \Longrightarrow 2^n$=2500==> n =$\log_2$(2500)=11.3
- N must be an integer, so we choose n=12
-

Example: ADC range 5 V

(matched by sensor output through S/C block)

- **Solution:** **S/C**
- 1 deg C => 0.02 V ===> **multiplied by 2.5 ==> 0.05 V**
- 100 deg C => 100x 0.02=2V **===> X 2.5 = 5V**
- Suppose we have an ADC with V_{FSR}= 5 V range
- For 1 deg C resolution , ADC resolution Δ = 0.02 V
- $\Delta = 0.05V = \frac{V_{FSR}}{2^n} = \frac{5}{2^n} \Longrightarrow 2^n$=100==> n =$\log_2$(250)=6.64
- N must be an integer, so we choose n=7
- For 0.1 deg C resolution , ADC resolution Δ = 0.005 V
- $\Delta = 0.005V = \frac{V_{FSR}}{2^n} = \frac{5}{2^n} \Longrightarrow 2^n$=1000==> n =$\log_2$(1000)=9.96
- N must be an integer, so we choose n=10

Conclusion about range matching

- When the ranges are not matched, higher number of bits “n” is required to achieve higher measurement resolution
- When we match the output range of the sensor to the input range of ADC, we can get better resolution of a given ADC with given number of bits

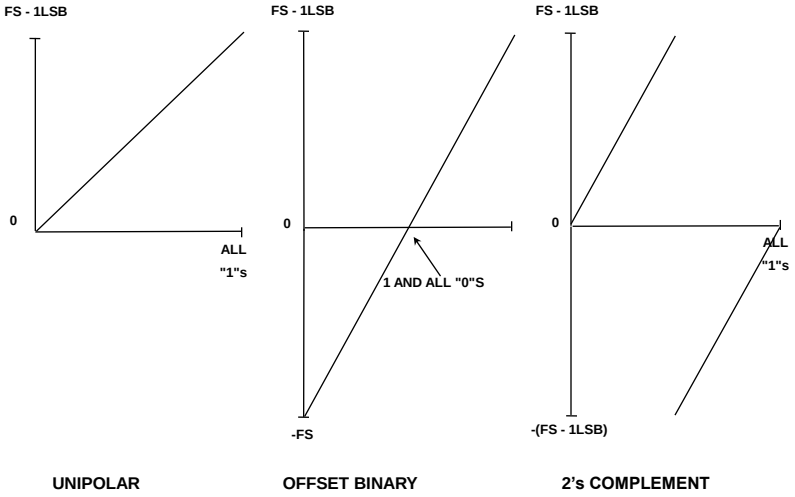
Coding Conventions

- There are several different formats for ADC output data:
- Unipolar
- Bipolar
- An ADC using *binary* coding produces all 0s (e.g., 000 for the three-bit converter) at –full-scale and all 1s (e.g., 111) at +full-scale.
- If the range is bipolar, so that –full-scale is a negative voltage, binary coding is sometimes called *offset binary* since the code 0 does not refer to 0 V.
- To make digital 0 correspond to 0 V, bipolar ADCs use *two’s complement* coding, which is identical to offset binary coding except that the *most significant bit (MSB*) is inverted, so that 100 … 00 corresponds to –full-scale, 000 … 00 corresponds to 0 V (*midscale*), and 011 … 11 corresponds to +full-scale.

Coding Conventions-BCD

- Decimal-digit ADCs, such as those used in digital voltmeters, use a coding scheme call *binary-coded decimal (BCD)*
- BCD data consists of a string of four-bit groups of binary digits.
- Each four-bit group represents a decimal digit, where 0000 is 0, 0001 is 1, and so on, up to 1001 for 9.
- The other six combinations (1010 through 1111) are invalid, or can be used for special information, such as the sign of the conversion.

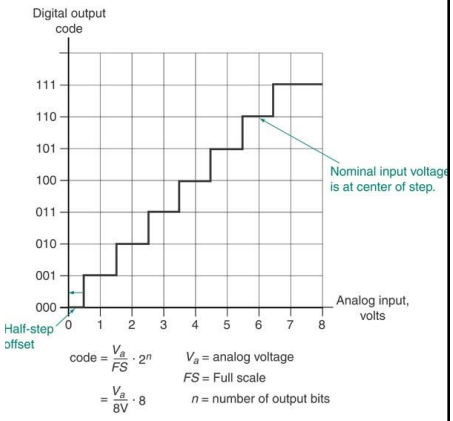
Unipolar and Bipolar Converter Codes



Unipolar ADC Code Equation

$$\text{code} = \frac{V_a}{V_{FS}} \times 2^n$$

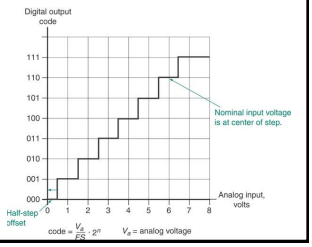
- V_a = analog input voltage to be sampled.
- V_{FS} = Full scale range of input voltage.
- n = number of bits in the output code.



Unipolar ADC Output Codes

Nominal Voltage of Input Step (volts)	Range (volts)	Output Code
0.0	0.0 - 0.5	000
1.0	0.5 - 1.5	001
2.0	1.5 - 2.5	010
3.0	2.5 - 3.5	011
4.0	3.5 - 4.5	100
5.0	4.5 - 5.5	101
6.0	5.5 - 6.5	110
7.0	6.5 - 8.0	111

$$\text{code} = \frac{V_a}{V_{FS}} \times 2^n$$

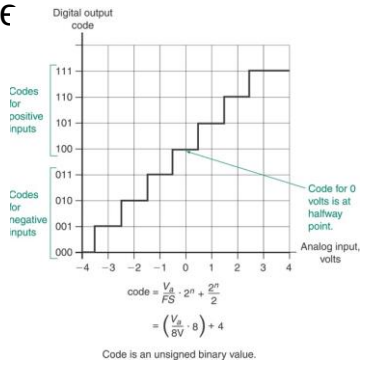


Bipolar ADC (Offset Binary Coding)

- Used to represent positive and negative input voltages.
- Output code an unsigned binary number.
- Numbers below 0 V are negative.
- Numbers above 0 V are positive

$$\text{code} = \left(\frac{V_a}{V_{FS}} \times 2^n \right) + \text{offset}$$

$$= \left(\frac{V_a}{V_{FS}} \times 2^n \right) + \frac{2^n}{2}$$

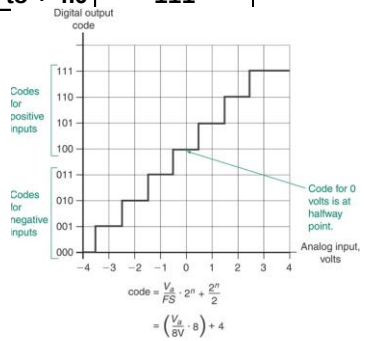


Bipolar ADC Output Codes

- 4.0	**- 4.0 to - 3.5**	**000**
- 3.0	**- 3.5 to - 2.5**	**001**
- 2.0	**- 2.5 to - 1.5**	**010**
- 1.0	**- 1.5 to - 0.5**	**011**
0	**- 0.5 to + 0.5**	**100**
+ 1.0	**+ 0.5 to + 1.5**	**101**
+ 2.0	**+ 1.5 to + 2.5**	**110**
+ 3.0	**+ 2.5 to + 4.0**	**111**

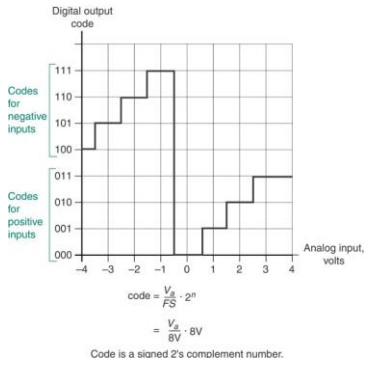
$$\text{code} = \left(\frac{V_a}{V_{FS}} \times 2^n \right) + \text{offset}$$

$$= \left(\frac{V_a}{V_{FS}} \times 2^n \right) + \frac{2^n}{2}$$



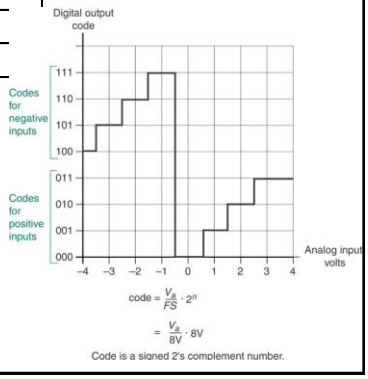
Bipolar ADC (2's Complement Coding)

- Uses a 2's complement number system.
- Most significant bit (MSB) is the sign bit.
- MSB = '1' sign negative.
- MSB = '0' sign positive.

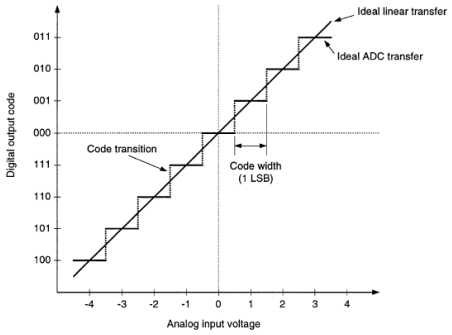


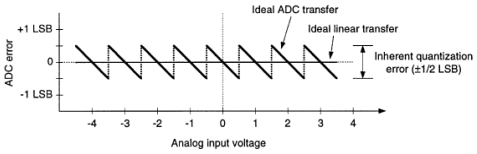
2's Complement Output Codes

Nominal Voltage of Input Step (volts)	Range (volts)	Output Code
- 4.0	- 4.0 to - 3.5	100
- 3.0	- 3.5 to - 2.5	101
- 2.0	- 2.5 to - 1.5	110
- 1.0	- 1.5 to - 0.5	111
0	- 0.5 to + 0.5	000
+ 1.0	+ 0.5 to + 1.5	001
+ 2.0	+ 1.5 to + 2.5	010
+ 3.0	+ 2.5 to + 4.0	011



- Accuracy: ADC has several sources of error
- - Quantization error $\Delta_e = \mp\frac{1}{2}LSB$

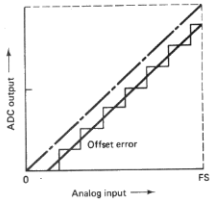




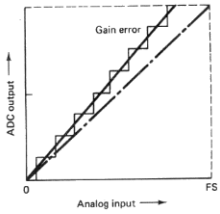
- This is a random error and can be represented by an rms noise source $e_{rms} = \frac{LSB}{\sqrt{12}} = 0.289LSB$
- This places a limit on Dynamic Range
- $DR = 20log\frac{S}{N}$
- $DR = 6.026n + 1.7609$
- $ENOB = \frac{DR-1.7609}{6.026}$
- For an ADC with DR=92dB
- ENOB= $\frac{92-1.7609}{6.026}$=14.988 bits

Summary of other ADC Errors

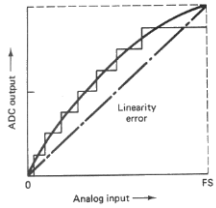
- Offset Error



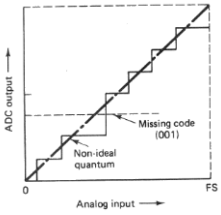
- Gain Error



- Can be eliminated by initial adjustments
- Integral Linearity Error



- Differential Linearity Error



- Nonlinear Error
  - Hard to remove

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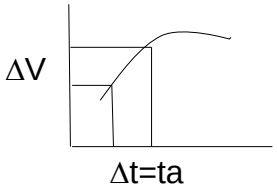
Aperture Errors

- Aperture errors have to do with the **timing of analog-to-digital conversions, particularly of the S/H.**
- *Aperture delay* characterizes the amount of time that lapses from when an ADC (S/H) receives a convert pulse to when the sample is held as a result of the pulse.

Aperture Error

- ADC conversion takes time (τ_c) which might be fixed or variable depending of ADC type
- If analog input is changing during conversion(this can also be due to clock jitter), then the converted signal will be in error known as Aperture Error
- To avoid error in digitized output, this change must be small and less than ½ Δ



Actual Sampling time uncertainty due to changing signal or clock jitter

Consider A sine wave

- Assume Vin=Vref Sin ωot
- $\left(\frac{\Delta V}{\Delta t}\right)_{max} = V_{REF}\omega_0 \Longrightarrow \Delta t = \frac{\Delta V}{V_{REF}\omega_0}$

$$let\ \Delta V = \frac{1}{2}LSB = \frac{V_{REF}}{2.2^n}$$

$$\Delta t = \frac{\frac{V_{REF}}{2.2^n}}{V_{REF}\omega_0} = \frac{1}{2.2^n\omega_0}$$

One must make sure that conversion time τ_c is less than ta

Conversion Time (τ_C)

- τ_C is the time the ADC takes to convert a single analog input voltage value to corresponding digital value
- During conversion process the input must remain constant, or if it is allowed to change, this change should be restricted to a value : $\frac{dV_{in}}{dt} < \frac{V_{FSR}}{2^n\tau_c}$

- **Example**: a 10 bit ADC with τ_c=20 μs , what is the maximum allowable rate of change (frequency) of a sinusoidal input voltage to be converted using this ADC
- Solution: $\frac{dV_{in}}{dt} < \frac{V_{FSR}}{2^n \tau_c}$
- $A\omega_o < \frac{V_{FSR}}{2^n \tau_c}$, let A=V_{FSR}

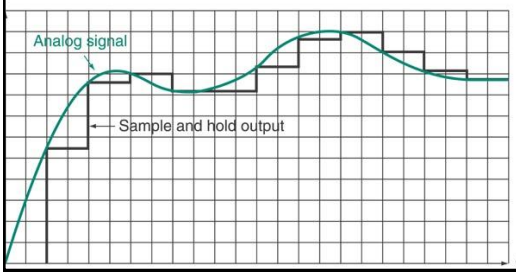
$$\omega_o < \frac{1}{2^n \tau_c}$$

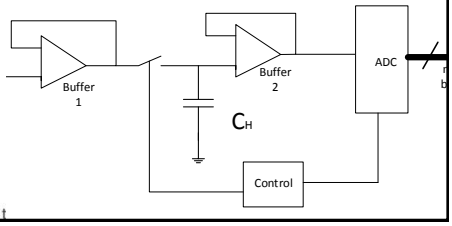
$$f_o < \frac{1}{2\pi . 2^{10} 20\mu s} = 7.75\ Hz$$

This is the maximum frequency of input to be used with this ADC>>>>> If higher frequency needed , increase n or reduce τ_c

Sample and Hold Circuit

- Sample and Hold (S& H) reduces Δt
- S&H is placed at the input of ADC, it holds the input signal at a constant level during conversion
- S&H is used to avoid errors if variations of the measurand were allowed to pass to the ADC
- Reduce uncertainty error in the converted output when input changes are fast compared to the conversion time
- Sample mode: output follows input
- Hold: Output is held constant until sample mode is resumed



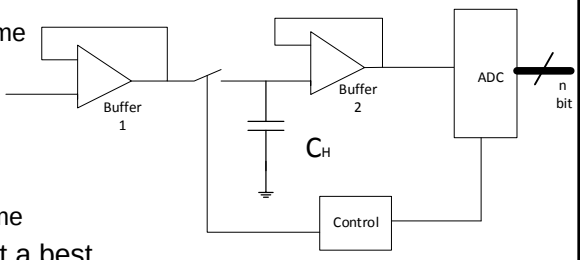


- This is low pass filter with fc as high as possible in order not to disturb the signal

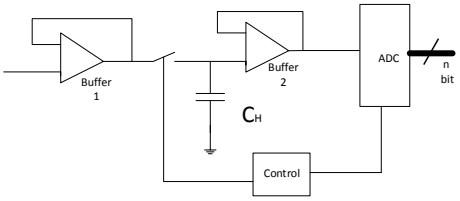
$$f_c = \frac{1}{2\pi(\sum R)C_H}$$

- Care in selecting hold capacitor C_H
  - Low Value C_H
    - Increases BW
    - Reduces acquisition time
    - Increase Droop
  - High Value C_H
    - Reduces BW
    - Minimize Droop
    - Increase acquisition time
  - Choose capacitor to get a best acquisition time while keeping the droop per conversion below 1 LSB

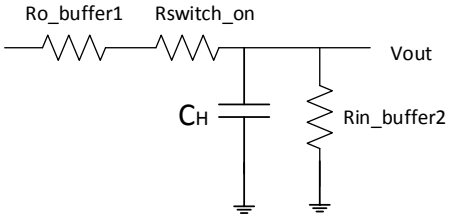
- In Multi-channel system S&H used
  - To hold a sample from one channel while multiplexer proceed to sample next one
  - Simultaneous sampling of two signal



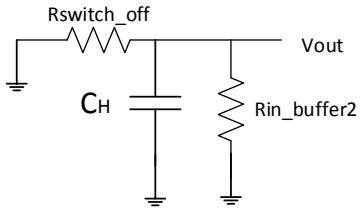
- Care in selecting hold capacitor C_H
- Choose capacitor to get a best acquisition time while keeping the droop per conversion below 1 LSB



Sample/Track Mode
For High fc , C_H must be low



Hold Mode
C_H must be low to minimize discharge of Capacitor (Droop)

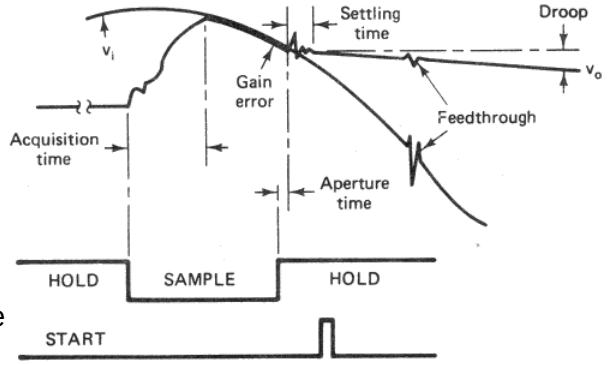


Sample and Hold Circuits

τ_{acq} – time required for the S&H circuit to acquire signal when changing from the hold mode to sample mode

τ_{ap} – aperture time, time required for switch from sample to hold state (time when output stops following the input)

or time between when the hold command is received to actual transition to actual hold mode



Converter Throughput Rate/ Frequency

- It is defined as the number of times the input signal can be sampled maintaining full accuracy
- It is calculated as the inverse of total time required for one successful conversion
- 1) For ADC's without S&H

$$f = throughput = \frac{1}{\tau_c}$$

- 2) For ADC's with S&H: other delays affect the throughput

$$f = throughput = \frac{1}{\sum \tau}$$

where $\sum \tau = \tau_c + \tau_{acq} + \tau_{ap}$

Commercially Available S/H

Device type	Manufacturers	Acquisition time	Aperature time	Settling time	Features	Price (100s)
AD582	Analog Devices	6 μs to 0.1% 25 μs to 0.01%	150 ns	0.5 μs	Monolithic, general purpose	$ 8
AD583	Analog Devices	4 μs to 0.1% 5 μs to 0.01%	50 ns	—	Monolithic, faster	16
LF398	National	4 μs to 0.1% 6 μs to 0.01%	150 ns	0.8 μs	Monolithic, general purpose	3
SHC298	Burr-Brown	9 μs to 0.1% 10 μs to 0.01%	200 ns	1.5 μs	Monolithic, general purpose	7
AD346	Analog Devices	2 μs to 0.01%	60 ns	0.5 μs	Hybrid, internal hold capacitor	—
SHC85	Analog Devices, Datel-Intersil, Burr-Brown	4 μs to 0.01%	25 ns	0.5 μs	Hybrid, internal hold capacitor, low droop rate	70
HTS0025	Analog Devices	20 ns to 0.01%	20 ns	30 ns	Hybrid, very fast	187

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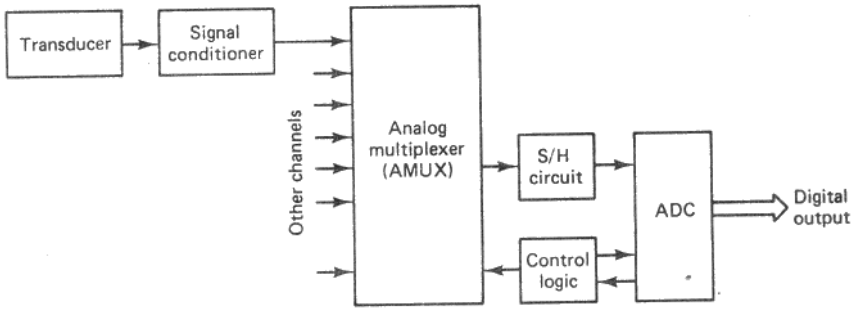
Multi-channel DAQ System



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TYPES of ADC

Flash

Integrating

SAR

Sigma-Delta

ADC Types

- Various ADC Types exist as a result of different requirements imposed instrumentation, control, audio and video applications
- Obviously speed / conversion rate is not critical in dc or slowly changing measurands
- However, resolution might be important

Types of ADCs

- Most ADC types have the following two blocks in common:
- Comparator ==> Vo= logic “1” if V(+) > V(-)
- Vo= logic “0” if V(+) < V(-)
- Precise and stable voltage reference

Direct Conversion//Flash//Parallel ADC

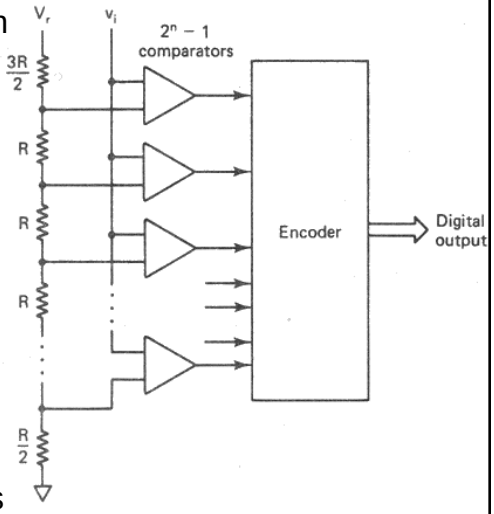
- Very High speed of conversion with sampling rate up to 1 GS/s
- For an ADC $\tau_c = \frac{1}{1\ GS/s}$=1 ns
- Resolution is limited to 8 bits due to increased number of comparators (2^n -1) and resistors (2^n)

Flash ADC

- highest speed
- large # of comparators
- large size
- large power consumption
- 8-bit maximum resolution

Parallel or Flash ADC

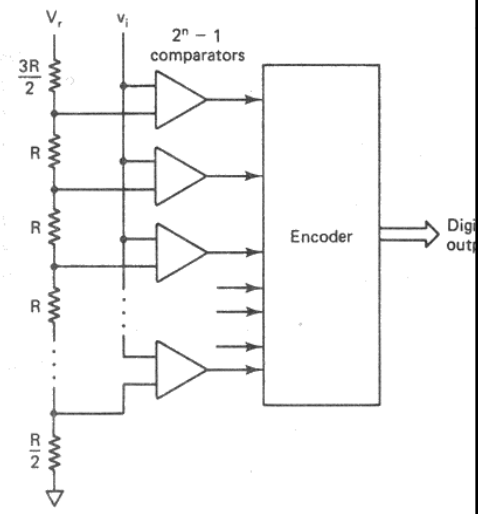
- Very High speed conversion
  - Up to 1000MHz for 8 bit resolution
  - Video, Radar, Digital Oscilloscope
- Single Step Conversion
  - 2^n –1 comparator
  - 2^n Precision Resistive Network
  - Encoder
- Resolution is limited
  - Large number of comparator and resistors in IC ==> bigger die and higher cost



Parallel or Flash ADC

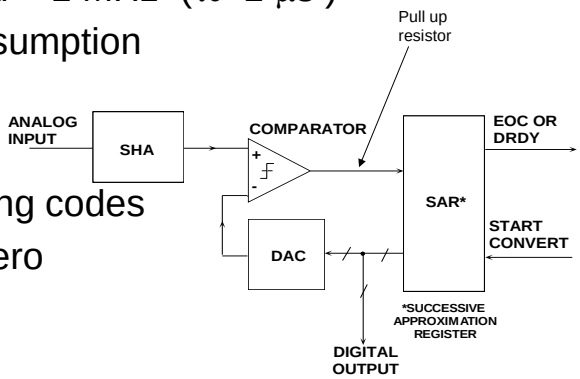
2 bit ADC
Δ=1/4
3 comparators
4 Resistors

D3	D2	D1	b2	b1
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

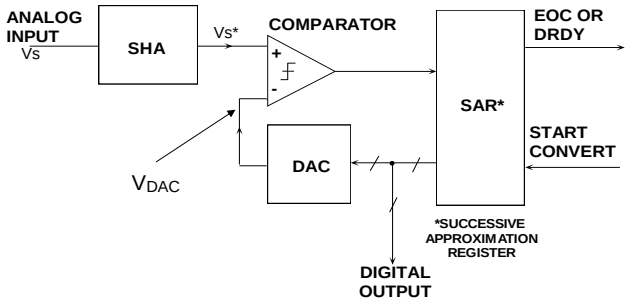


SAR ADC

- SAR – successive approximation register
- SAR ADC are probably the most widely used
- 8-16 bits ;
- Moderate speed ~ 1 MHz (τ_c=1 μs)
- Low power consumption
- Low cost
- Require S&H
- Can have missing codes
- simple to autozero



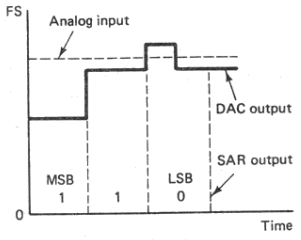
SAR ADC



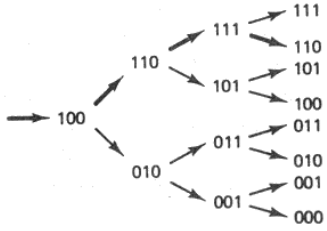
- Based on SAR Register
- DAC output "V_{DAC}" is used as a reference
- Final result is reached after n-steps,
- In each step 1 bit conversion is done

Successive Approximation ADC

- Circuit waveform



- Logic Flow (decision Tree)



- **Conversion Steps**
- 1. initially SAR provides an output corresponding to half the range (100..0)
- 2. DAC outputs an analog voltage V_{DAC} which if found greater than Vs , then MSB is set to "1", otherwise MSB=0
- 3. IF MSB is reset to 0, next bit is tried until V_{DAC} =Vs
- 4. n -conversion steps, each takes a clock period

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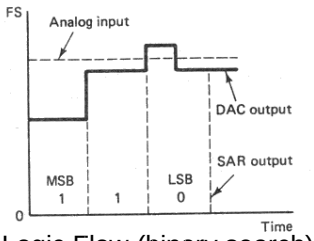
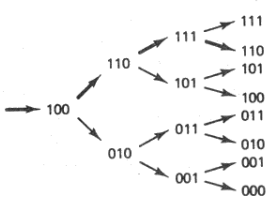
Successive Approximation ADC

- Circuit waveform



- Logic Flow (binary search)



- Conversion Time
  - n clock for n-bit ADC
  - Fixed conversion time
- Serial Output is easily generated
  - Bit decision are made in serial order

  - $\tau c = n\ Tclock$
  - $Tclock = 1/fclock$

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How a Successive Approximation A/D Converter Works

- Rising/Falling Edge of Convert Start Pulse Resets Logic
- Falling/Rising Edge Begins Conversion Process
- Bit Comparisons Made on Each Clock Edge
- Conversion Time Equals Number of Comparisons (Resolution) Times Clock Period
- The Accuracy of Conversion Depends on the DAC Linearity and Comparator Noise

Successive Approximation ADC

Advantages to SAR A/D converters

- Low Power (12-bit/1.5 MSPS ADC: 1.7 mW)
- Higher resolutions (16-bit/1 MSPS)
- Small Die Area and Low Cost
- No pipeline delay

Tradeoffs to SAR A/D converters

- Lower sampling rates

Typical Applications

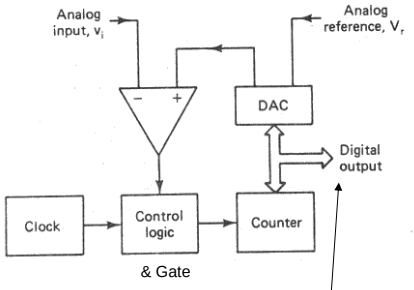
- Instrumentation
- Industrial control
- Data acquisition

Example

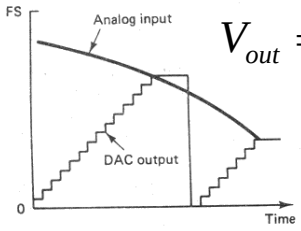
- VFSR=5V, 4 bit, SAR ADC, Vs=Vin=3.127 V, explain how conversion is done?
- Solution:
- Suppose Output is $b_1b_2b_3b_4$
- (1) let b1=1, b2=b3=b4=0
- 1000 ==> VDAC=8/2^4*VREF=2.5V
- Check VDAC > Vs ? (2.5 > 3.127? ==> NO ==> set **b1=1**
- (2) set b2=1, b3=b4=0
- 1100 ==> VDAC=10/2^4*VREF=3.75V
- Check VDAC > Vs ? (3.75 > 3.127? ==> Yes ==> Reset **b2=0**
- (3) set b3=1, b4=0
- 1010 ==> VDAC=9/2^4*VREF=3.1255V
- Check VDAC > Vs ? (3.125 > 3.127? ==> No ==> set **b3=1**
- (4) set b4=1, 1011 ==> VDAC=11/2^4*VREF=3.4375V
- Check VDAC > Vs ? (3.4375 > 3.127? ==> Yes ==> Reset **b4=0**
- **Final Result: 1010**

Counter Type ADC

- Block diagram



- Waveform



$$V_{out} = \frac{N}{2^n} \times V_{FSR}$$

- Operation
- Reset and Start Counter
  - DAC convert Digital output of Counter to Analog signal
  - Compare Analog input and Output of DAC
    - Vi < V_{DAC}
      - Continue counting
    - Vi >= V_{DAC}
      - Stop counting
  - Digital Output = Output of Counter
- Disadvantage
  - Conversion time is varied
    - 2^n Clock Period for Full Scale input

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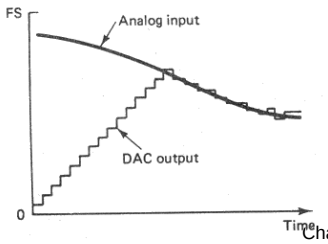
Tracking Type ADC

- Tracking or Servo Type
  - Using Up/Down Counter to track input signal continuously
    - For slow varying input



- Can be used as S/H circuit
  - By stopping desired instant
  - Digital Output
  - Long Hold Time

Chap 0

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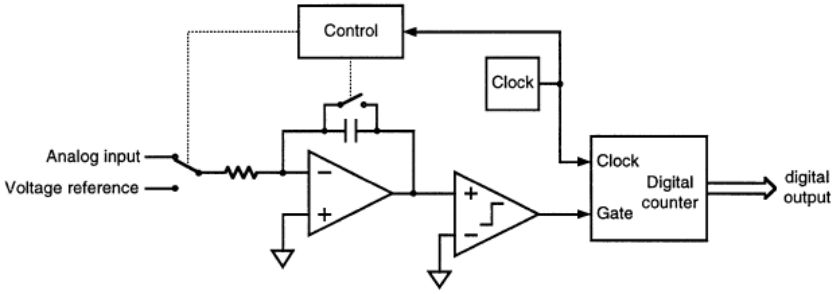
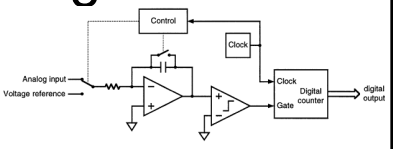
Dual Slope Integrating ADC

- *Integrating* converters are used for low-speed, high-resolution applications such as voltmeters.
- They are conceptually simple, consisting of an integrating amplifier, a comparator, a digital counter, and a very stable capacitor for accumulating charge
- The most common integrating ADC in use is the dual-slope ADC



Dual Slope Integrating ADC

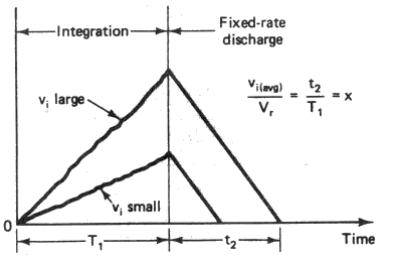


- Initially, the capacitor is discharged and so has no voltage across it.
- At time 0, the input to the integrator is switched to the analog input and the capacitor is allowed to charge for an amount of time, T1, which is fixed.
- Its rate of charging and thus its voltage at T1 are proportional to the input voltage.
- At time T1 the input switch flips over to the voltage reference, which has a negative value so that the capacitor will begin to discharge at a rate proportional to the reference.
- The counter measures how long it takes to discharge the capacitor completely.

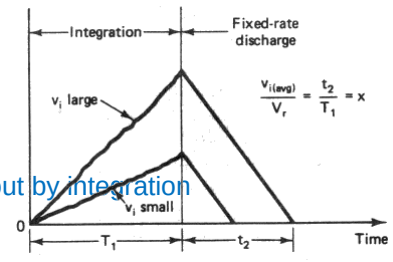
- If the capacitor is of high quality, the ratio of the discharge time to the charge time is proportional to the ratio of the input voltage to the voltage reference, and so the counter output represents the analog input voltage.
- An elaboration of the dual-slope ADC is the *multislope* integrating ADC. It achieves even higher resolution than the dual-slope ADC by discharging the capacitor at several progressively slower rates. At each rate, the counter is able to resolve finer increments of accumulated charge.

- Operation
  - Integrate $\int_0^{T_1} v_i dt$
  - Reset and integrate $\int_0^{t_2} V_r dt$
  - Thus $T_1 V_{i(AVG)} = t_2 V_r$
  - →
- Applications $V_{i(AVG)} = V_r \frac{t_2}{T_1}$
  - DPM(Digital Panel Meter), DMM(Digital Multimeter), …

$t_2 = Count * Tclock$

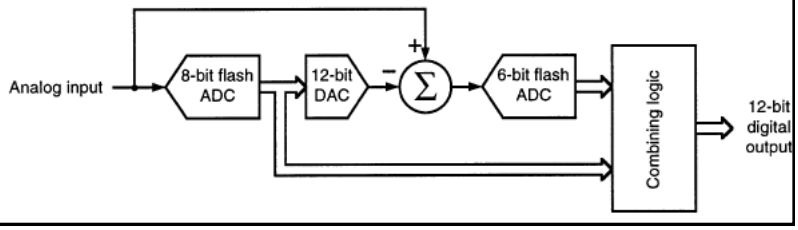


- Integrating converters do not sample the voltage itself; they *average* the voltage over the integration period and *then* they sample the average that is accumulated on the capacitor.
- This tends to reject noise that conventional sampling cannot, especially periodic noises. Most integrating ADCs operate with an integration period that is a multiple of one AC line period (1/60 or 1/50 s) so that any potential interference from stray electric or magnetic fields caused by the power system is canceled.
- Low speed
- High resolution and low cost
- Very stable
- Excellent Noise Rejection
  - High frequency noise cancelled out by integration
  - Proper T_1 eliminates line noise
  - Easy to obtain good resolution

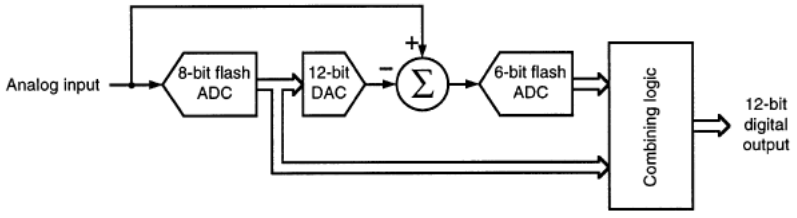


Pipeline "Subranging or Multistage" ADC

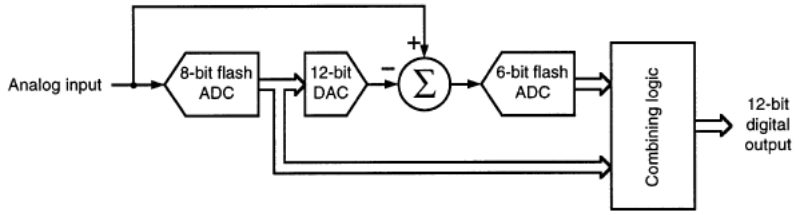
- To achieve higher sample rates than SAR ADCs at resolutions of 10 to 16 bits, *multistage* ADCs (sometimes called *subranging* or *multipass* ADCs) use the iterative approach of SAR ADCs but reduce the number of iterations in a conversion.
- Instead of using just a comparator, the multistage ADC uses low-resolution flash converters (4 to 8 bits) as building blocks.
- An example of a 12-bit two-stage ADC built out of two flash ADCs and a fast DAC.



- The 6-bit flash ADC converts the residual error of the 8-bit flash ADC. The two digital outputs are combined to produce a 12-bit conversion result.
- If each flash ADC has a T/H at its input, then each stage can be converting the residual error from the previous stage while the previous stage is converting the next sample.
- The whole converter then can effectively operate at the sample rate of the slowest stage.
- Without the extra T/Hs, a new conversion cannot start until the residues have propagated through all the stages. This variation of the multistage ADC is called a *pipelined* ADC.

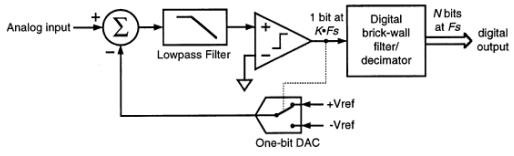


- An example of a 12-bit multistage ADC built out of two flash ADCs and a fast DAC.
- The 8-bit flash ADC takes a first “guess” at the input signal and the 6-bit flash ADC converts the error in the guess, called the “residue.”
- The 12-bit DAC actually needs to have only 8 bits, but it must be accurate to 12 bits.
- If the 8-bit flash ADC were perfect, the second flash ADC would only need 4 bits. But since the first flash actually may have some error, the second flash has 2 bits of “overlap.

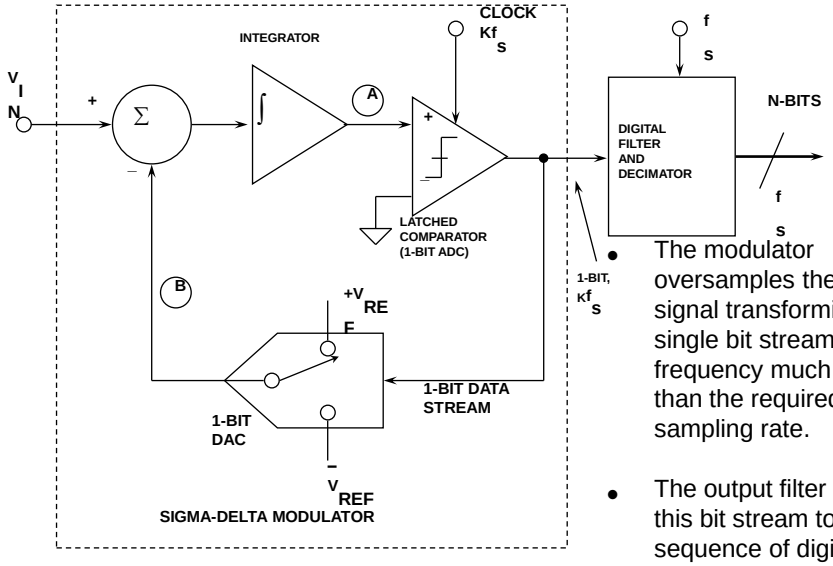


SIGMA-DELTA $(\sum -\Delta)$ ADC

- Two major Blocks: DAC & Digital Filter
- Used more and more for audio applications
- Resolution 16-24 bits
- Sample rate around 100 kS/s
- Low noise and low cost



FIRST-ORDER SIGMA-DELTA ADC



- The modulator oversamples the input signal transforming it to a single bit stream with frequency much higher than the required sampling rate.
- The output filter converts this bit stream to a parallel sequence of digital words at the sampling rate

SIGMA-DELTA ADCs

Advantages to Sigma-Delta A/D converters

- High resolutions and accuracy (24-bits)
- Excellent DNL and INL performance
- Noise shaping capability

Tradeoffs in Sigma-Delta A/D converters

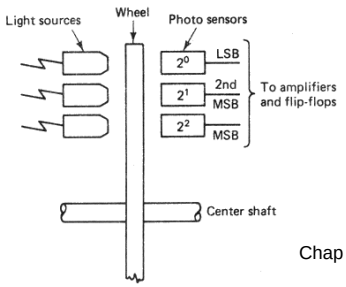
- Limited input bandwidth
- Slower sampling rates

Typical Applications

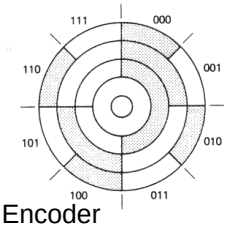
- Precision data acquisition and measurement
- Medical instrumentation

Shaft Encoder

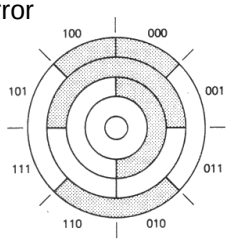
- Electromechanical ADC
  - Convert shaft angle to digital output
- Encoding
  - Optical or Magnetic Sensor
- Applications
  - Machine tools, Industrial robotics, Numerical control



- Binary Encoder
  - Misalignment of mechanism causes large error
    - Ex: 011 → 111 (180deg)



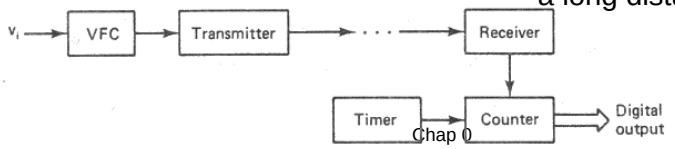
- Gray Encoder
  - Misalignment causes 1 LSB error



Voltage to Frequency ADC

- VFC (Voltage to Frequency Converter)
  - Convert analog input voltage to train of pulses
- Counter
  - Generates Digital output by counting pulses over a fixed interval of time

- Low Speed
- Good Noise Immunity
- High resolution
  - For slow varying signal
  - With long conversion time
- Applicable to remote data sensing in noisy environments
  - Digital transmission over a long distance



- END ADC