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Generation of high voltages

- Types of generated high voltages
  - *Direct voltages*
  - *Impulse voltages*
  - *Alternating voltages*

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Generation of high voltages ‘Direct Voltage’

- In h.v. technology direct voltages are mainly used for pure scientific research work and for testing equipment related to HVDC transmission systems.
- There is still a main application in tests on HVAC power cables of long length, as the large capacitance of those cables would take too large a current if tested with a.c. voltages.

Generation of high voltages ‘Direct Voltage’

- High d.c. voltages are even more extensively used in
  - Applied physics (accelerators)
  - Electro-medical equipment (X-rays),
  - Industrial applications (precipitation and filtering of exhaust gases in thermal power stations)
  - Communications electronics (TV, broadcasting stations).

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Generation of high voltages ‘Direct Voltage’

- The value of a direct test voltage is defined by its arithmetic mean value, which will be designated as V. Therefore, this value may be derived from

$$\overline{V} = \frac{1}{T}\int_0^T v(t)dt$$

where T equals a certain period of time if the voltage $v(t)$ is not constant, but periodically oscillating with a frequency of $f = 1/T$.

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Generation of high voltages
'Direct Voltage'

- Test voltages as applied to test objects then deviate periodically from the mean value. This means that a ripple is present.
- The amplitude of the ripple, δV, is defined as half the difference between the maximum and minimum values, or

$$\delta V = 0.5\left(V_{\max} - V_{\min}\right)$$

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Generation of high voltages ‘Direct Voltage’

- The ripple factor is the ratio of the ripple amplitude to the arithmetic mean value, or

$$RF = \frac{\delta V}{\overline{V}}$$

- For test voltages this ripple factor should not exceed 3% unless otherwise specified by the appropriate apparatus standard or be necessary for fundamental investigations.

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Generation of high voltages ‘Direct Voltage’

- Circuits to generate high d.c. voltages:
  - ➢Simple rectifier circuits
    - Half wave circuit
    - Full wave circuit
  - ➢Voltage doubler circuits
    - Simple voltage doubler circuit
    - Cascaded doubler circuit
  - ➢Voltage multiplier circuits
    - Cockcroft Walton circuit
    - The ‘Engetron’ or (Deltatron) circuit

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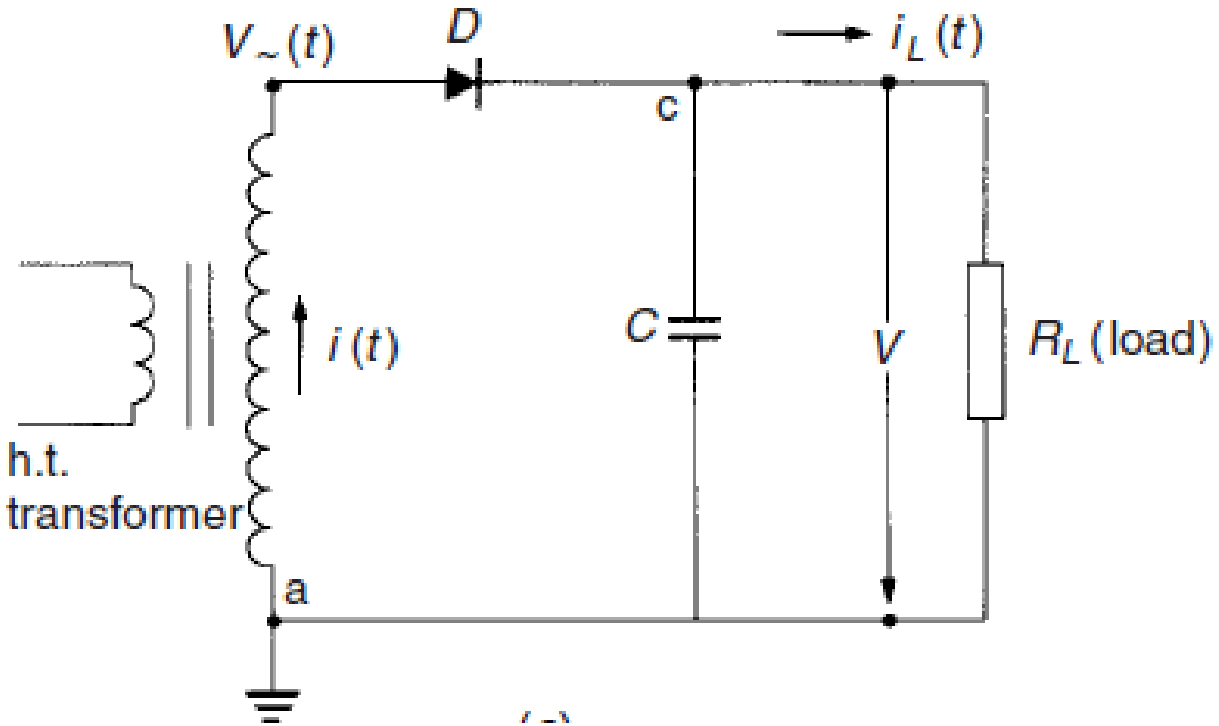
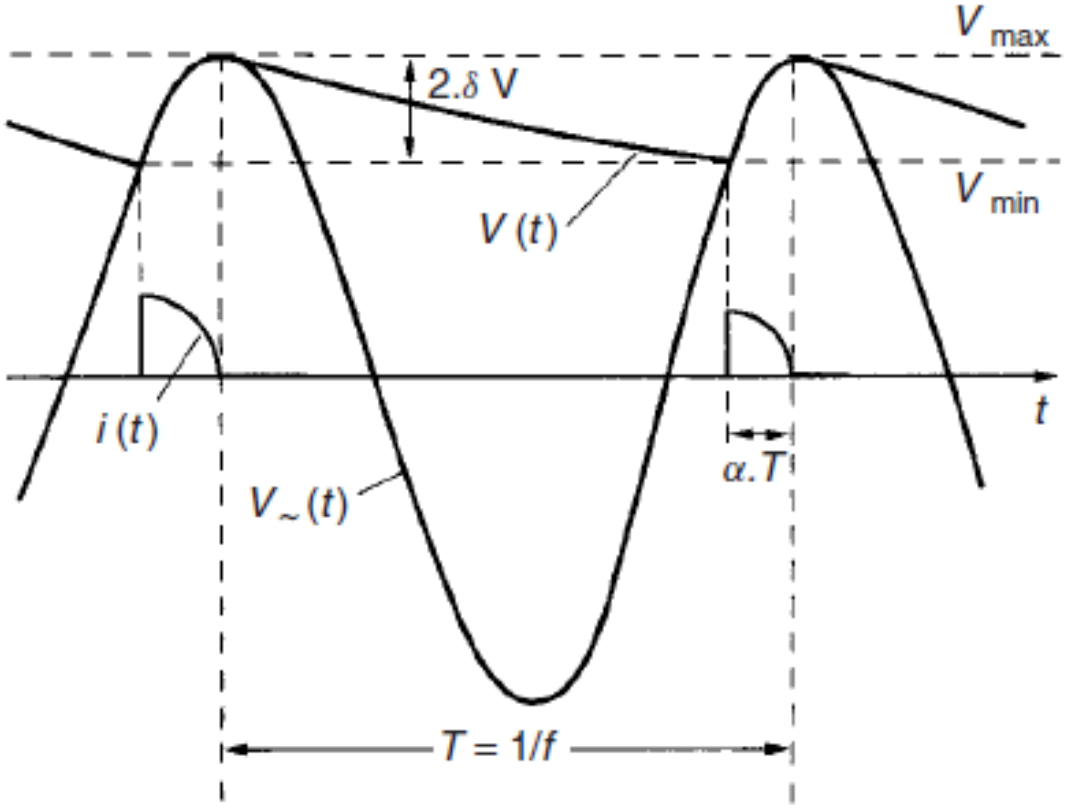
Generation of high voltages
'Direct Voltage, half wave circuit'

Simple rectifier circuits (Half wave)





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Generation of high voltages
'Direct Voltage, half wave circuit'

- If we neglect the leakage reactance of the transformer and the small internal impedance of the diodes during conduction
- The smoothing capacitor C is charged to the maximum voltage $+V_{max}$ of the a.c. voltage $V_{\sim}(t)$ of the h.t. transformer, when D conducts.
- If $I = 0$, i.e. the output load being zero $R_L = \infty$, the d.c. voltage across C remains constant $+V_{max}$, whereas $V_{\sim}(t)$ oscillates between $\pm V_{max}$.
- The diode D must be dimensioned, therefore, to withstand a peak reverse voltage of $2V_{max}$.

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Generation of high voltages
'Direct Voltage, half wave circuit'

- The output voltage V does not remain any more constant if the circuit is loaded.
- During one period, $T = 1/f$ of the a.c. voltage a charge q is transferred to the load R_L, which is represented as

$$q = \int_T i_L(t)dt = \frac{1}{R_L}\int_T V(t)dt = IT = \frac{I}{f}$$

where

I is the mean value of the d.c. output $i_L(t)$

$V(t)$ is the d.c. voltage which includes a ripple.

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Generation of high voltages
'Direct Voltage, half wave circuit'

- The charge q is also supplied from the transformer within the short conduction time $t_c = \alpha T$ of the diode D during each cycle. Therefore, q equals also to:

$$q = \int_{\alpha T} i(t)dt = \int_{T} i_L(t)dt$$

- As $\alpha T << T$, the transformer and diode current is pulsed and is much bigger amplitudes than the direct current $i_L(t) = I$.

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Generation of high voltages
'Direct Voltage, half wave circuit'

- The ripple δV could be calculated exactly for this circuit based upon the exponential decay of $V(t)$ during the discharge period $T\,(1-\alpha)$.
- We may assume that $\alpha = 0$. Then δV is easily found from the charge q transferred to the load, and therefore

$$q = 2\delta V\, C \Rightarrow \delta V = \frac{q}{2C} = \frac{IT}{2C} = \frac{I}{2\,fC}$$

- Ripple frequency equals the supply frequency in the case of half wave rectifier.

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Generation of high voltages
‘Direct Voltage, half wave circuit’

- The ripple δV depends on:
  - The supply voltage frequency f
  - The capacitance C
  - The load current I
  - The reactance of the h.t transformer

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Generation of high voltages
'Direct Voltage, half wave circuit'

- The single phase half-wave rectifier circuits have the following disadvantages:

  (*i*) The size of the circuits is very large if high and pure d.c. output voltages are desired.

  (*ii*) The h.t. transformer may get saturated if the amplitude of direct current is comparable with the nominal alternating current of the transformer.

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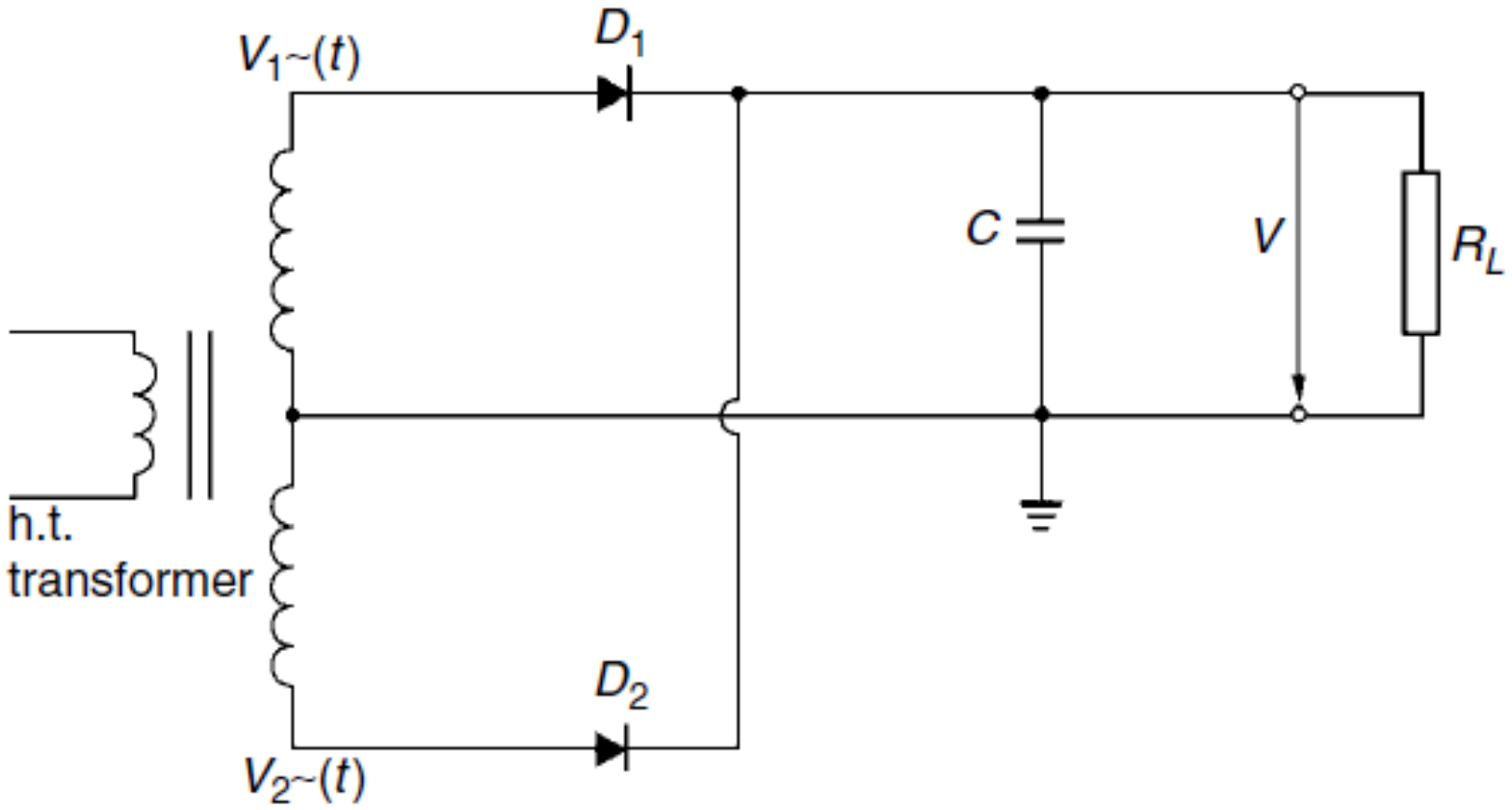
Generation of high voltages ‘Direct Voltage, full wave circuit’

Simple rectifier circuits (Full wave)



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Generation of high voltages
'Direct Voltage, full wave circuit'

- With reference to the frequency f during one cycle, now each of the diodes D_1 and D_2 is conducting for one half-cycle with a time delay of $T/2$.
- The ripple factor is therefore halved and given by:

$$\delta V = \frac{I}{4fC}$$

- Ripple frequency equals twice the supply frequency in the case of full wave rectifier.

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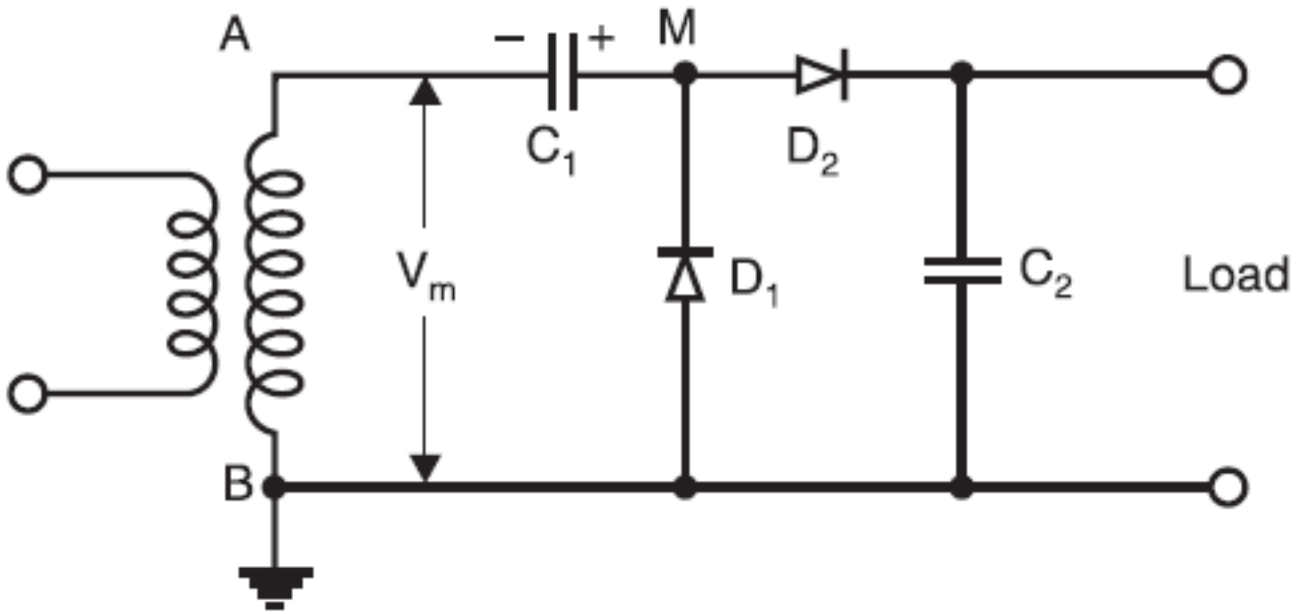
Generation of high voltages ‘Direct Voltage, doubler circuit’

- Both full wave and half wave rectifiers produce a dc voltage less than the maximum ac voltage.
- Therefore a voltage doubler circuits are used to produce higher dc voltage
- Types of voltage doubler circuits:
  - Simple voltage doubler circuit
  - Cascaded doubler circuit

Generation of high voltages
'Direct Voltage, Greinacher doubler circuit'

Greinacher voltage doubler circuit



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Generation of high voltages
'Direct Voltage, Greinacher doubler circuit'

- Suppose B is more positive with respect to A and the diode D_1 conducts thus charging the capacitor C_1 to V_{max}.
- During the next half cycle terminal A of the capacitor C_1 rises to V_{max} and hence terminal M attains a potential of $2V_{max}$.
- Thus, the capacitor C_2 is charged to $2V_{max}$ through D_2.
- Normally the voltage across the load will be less than $2V_{max}$ depending upon the time constant of the circuit C_2R_L.

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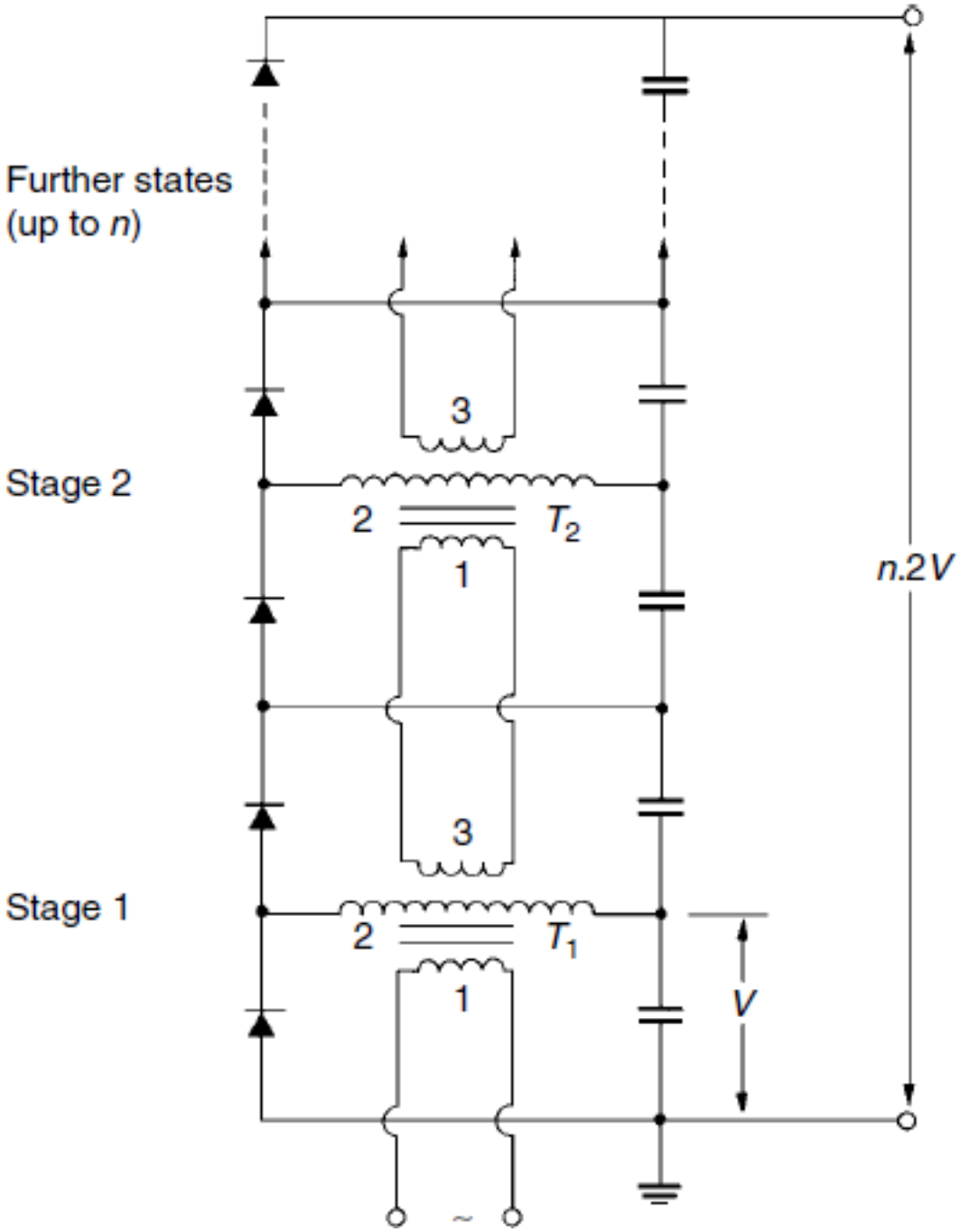
Voltage doubler circuit with cascaded transformers



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Generation of high voltages
'Direct Voltage, cascaded doubler circuit'

- Every transformer per stage consists of an l.v. primary (1), h.v. secondary (2), and l.v. tertiary winding (3) except the last stage.
- The tertiary winding (3) in the first stage excites the primary winding of the next upper stage.
- As none of the h.v. secondary windings is on ground potential, a d.c. voltage insulation within each transformer (T1, T2, etc.) is necessary, which can be subdivided within the transformers.
- Every h.v. winding feeds two half-wave rectifiers to produce a dc voltage equals $2V$/stage

Generation of high voltages
‘Direct Voltage, cascaded doubler circuit’

- Although there are limitations as far as the number of stages is concerned, as the lower transformers have to supply the energy for the upper ones, this circuit, excited with power frequency, provides an economical d.c. power supply for h.v. testing purposes with moderate ripple factors and high power capabilities.

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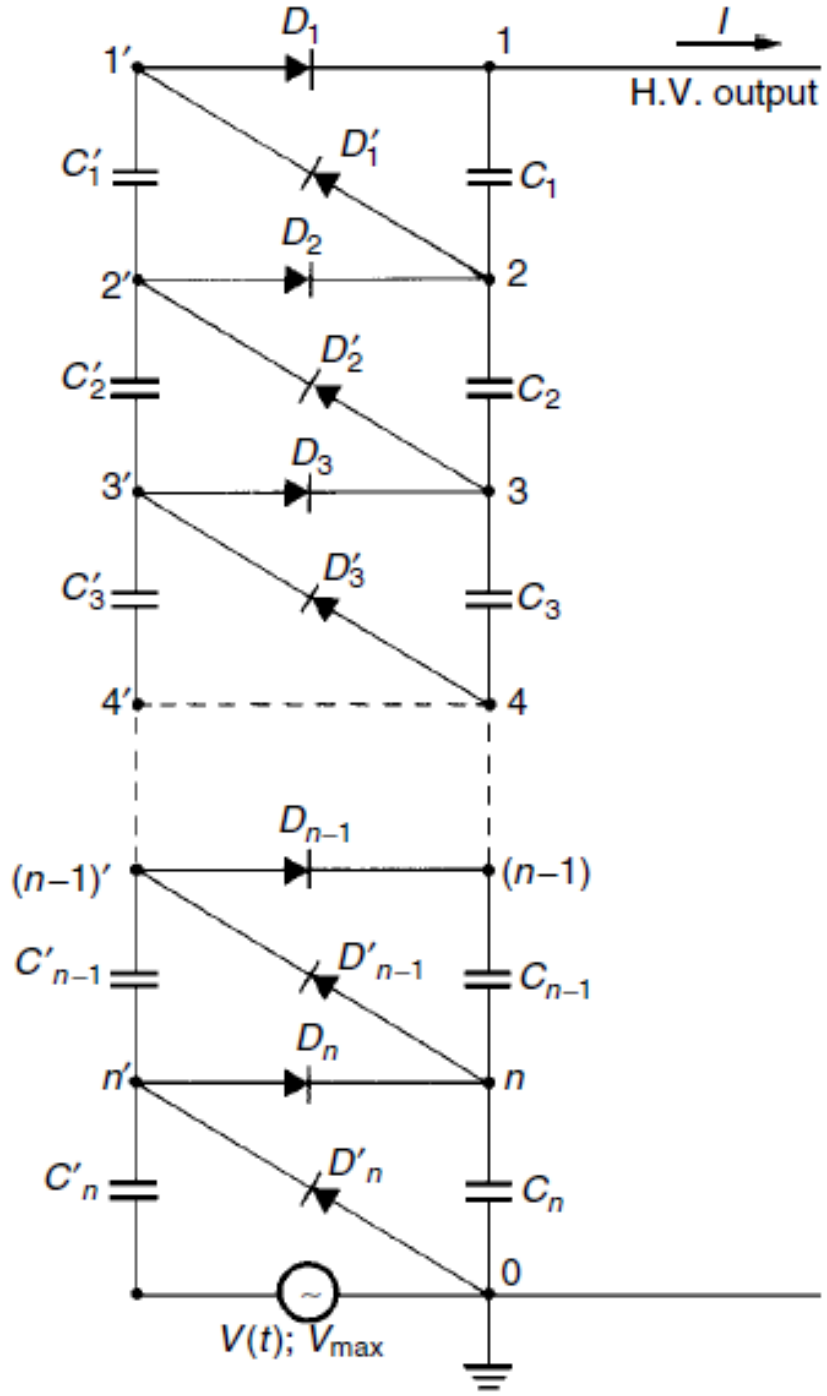
Cockroft–Walton multiplier circuit



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Generation of high voltages
'Direct Voltage, C-W multiplier circuits'

HV output open-circuited: $I = 0$.

- The portion 0-n'-$V(t)$ is a half-wave rectifier circuit in which C'_n charges up to a voltage of $+V_{max}$ if $V(t)$ has reached the lowest potential, $-V_{max}$.
- If C_n is still uncharged, the rectifier D_n conducts as soon as $V(t)$ increases (next half cycle).
- As the potential of point n' swings up to $+2V_{max}$ during the period $T = 1/f$, point n attains further on a steady potential of $+2V_{max}$ if $V(t)$ has reached the highest potential of $+V_{max}$.

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Generation of high voltages
'Direct Voltage, C-W multiplier circuits'

- The part n'-n-0 is therefore a half-wave rectifier, in which the voltage across D'_n can be assumed to be the a.c. voltage source.
- The current through D_n that charged the capacitor C_n was not provided by D'_n, but from $V(t)$ and C'_n.
- We assumed, therefore, that C'_n was not discharged, which is not correct.
- As we will take this into consideration for the loaded circuit, we can also assume that the voltage across C_n is not reduced if the potential n' oscillates between zero and $2V_{max}$.

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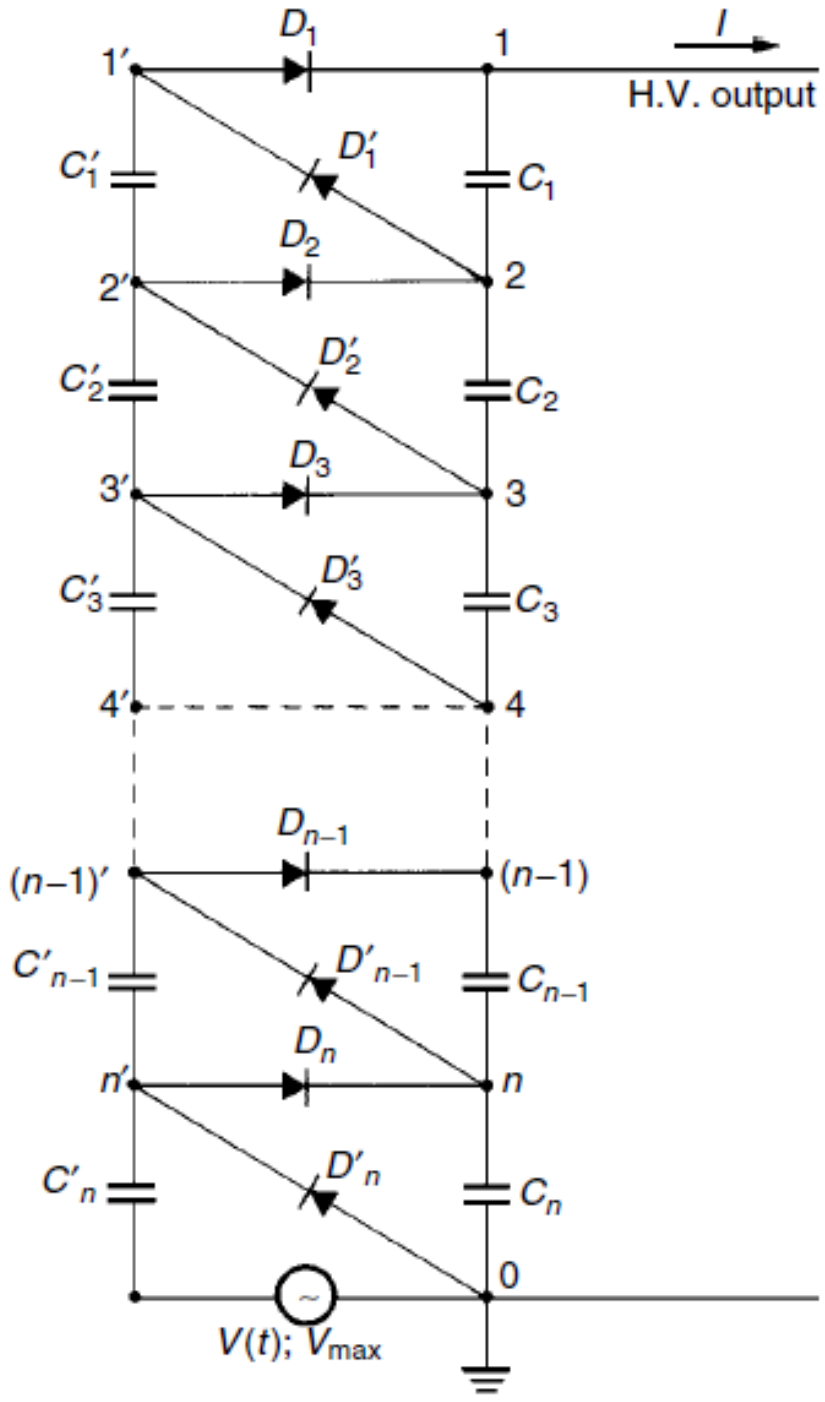
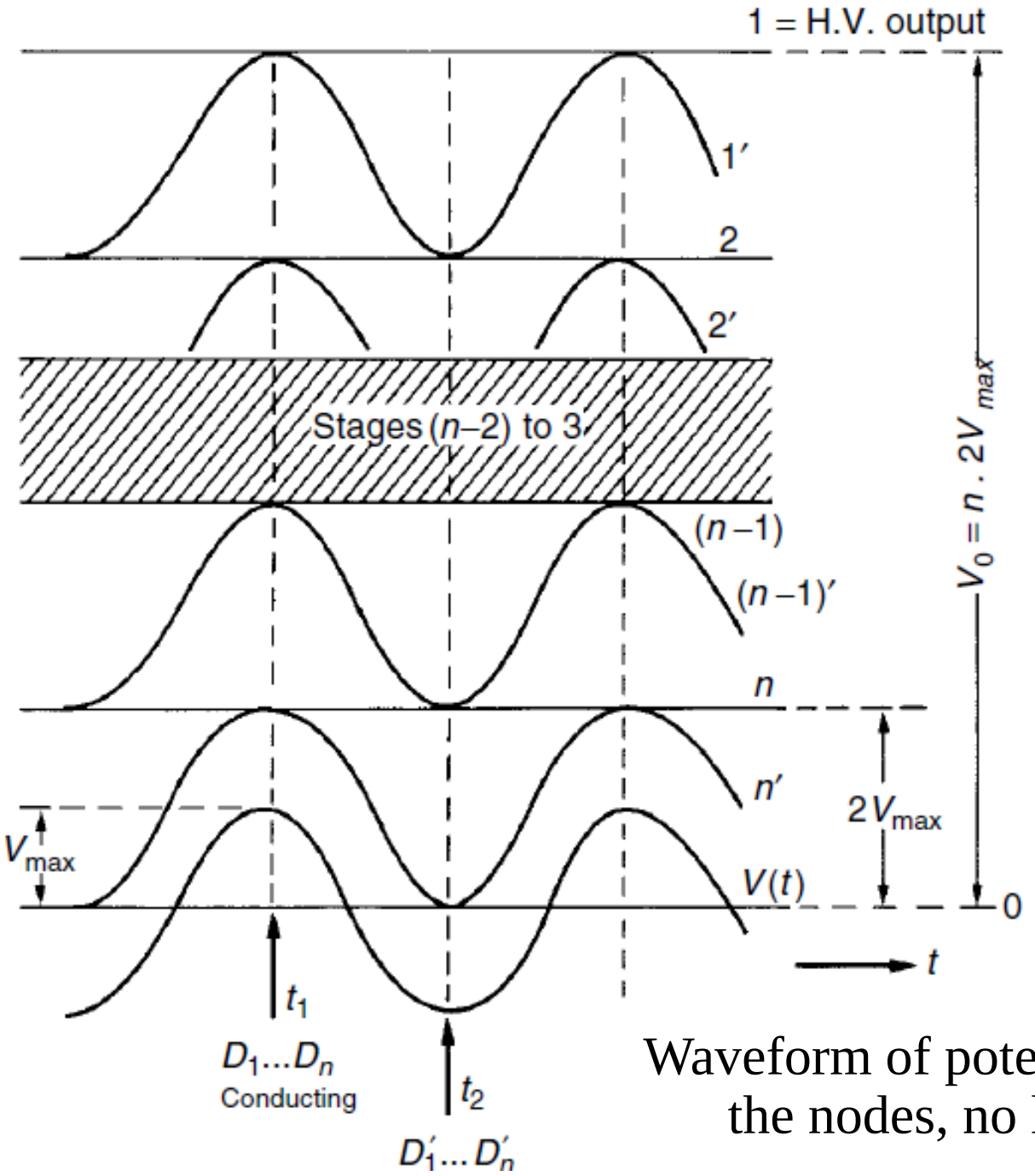
Generation of high voltages
'Direct Voltage, C-W multiplier circuits'

- If the potential of n', however, is zero, the capacitor C'_{n-1} is also charged to the potential of n, i.e. to a voltage of $+2V_{max}$.
- The next voltage oscillation of $V(t)$ from V_{max} to $-V_{max}$ will force the diode D_{n-1} to conduct, so that also C_{n-1} will be charged to a voltage of $+2V_{max}$.





Waveform of potentials at the nodes, no load

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Generation of high voltages ‘Direct Voltage, multiplier circuits’

- Notes from the output waveforms:
  - the potentials at the nodes 1′, 2′ … n' are oscillating due to the voltage oscillation of $V(t)$;
  - the potentials at the nodes 1, 2 . . . n remain constant with reference to ground potential;
  - the voltages across all capacitors are of d.c. type, the magnitude of which is $2V_{max}$ across each capacitor stage, except the capacitor C'_n which is stressed with V_{max} only;
  - every rectifier D_1, D'_1. . . D_n, D'_n is stressed with $2V_{max}$ or twice a.c. peak voltage; and
  - the h.v. output will reach a maximum voltage of $2nV_{max}$.

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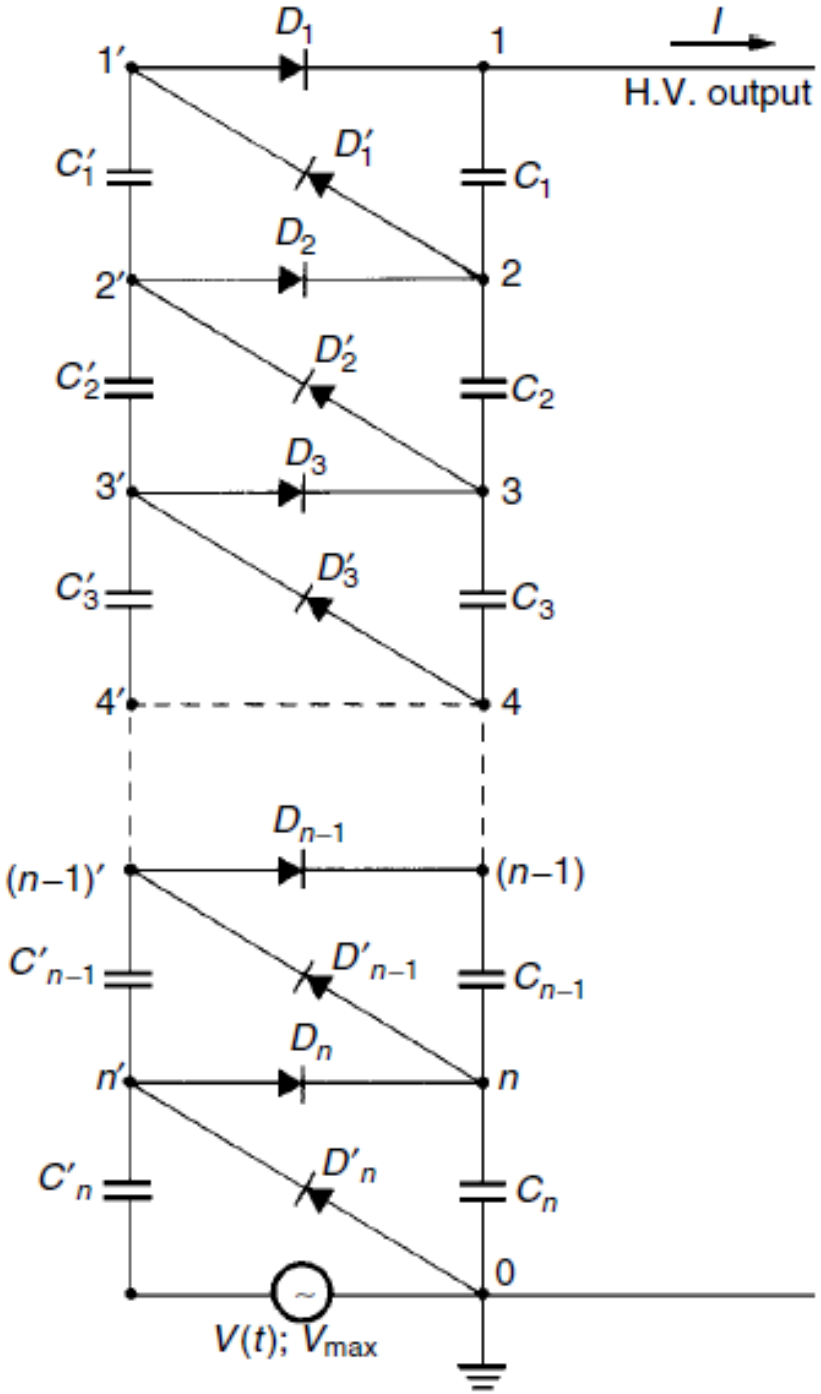
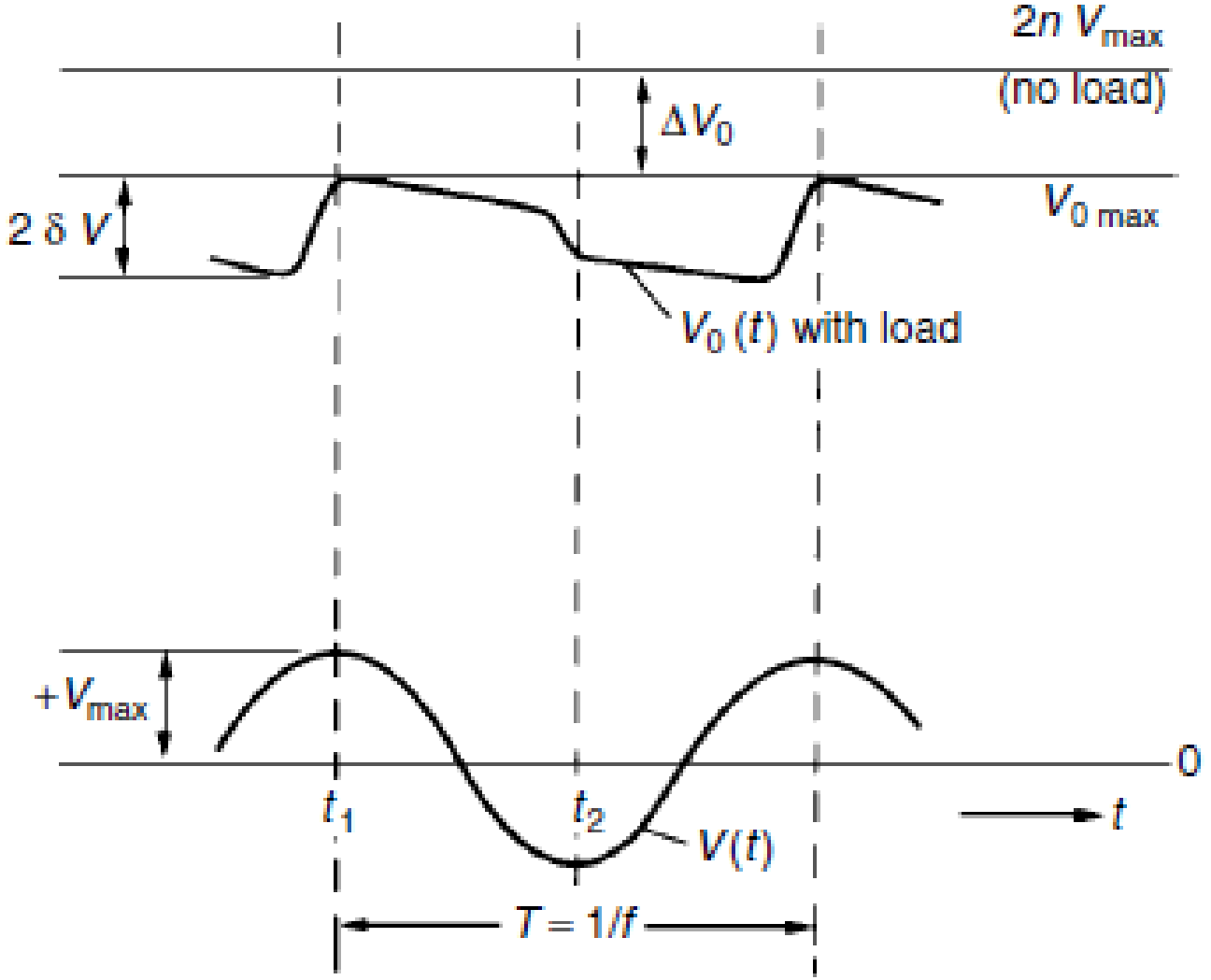
Generation of high voltages
'Direct Voltage, multiplier circuits'

H.V. output loaded: I > 0.

- If the generator supplies any load current *I*, the output voltage will never reach the value $2nV_{max}$.
- There will also be a ripple on the voltage, and therefore we have to deal with two quantities:
  - peak-to-peak ripple $2\delta V$
  - voltage drop ΔV_0





Loaded cascade circuit, definitions of voltage drop and ripple

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Generation of high voltages ‘Direct Voltage, multiplier circuits’

- The peak value of V_0 is reached at t_1, if $V(t)$ was at $+V_{max}$ and the rectifiers $D_1 \ldots D_n$ just stopped to transfer charge to the ‘smoothing column’ $C_1 \ldots C_n$.
- After that the current I continuously discharges the column, interrupted by a sudden voltage drop shortly before t_2: this sudden voltage drop is due to the conduction period of the diodes $D'_1 \ldots D'_n$, during which the ‘oscillating column’ $C'_1 \ldots C'_n$ is charged.

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Generation of high voltages
'Direct Voltage, multiplier circuits'

Peak-to-peak ripple $2\delta V$

- Now let a charge q be transferred to the load per cycle, which is obviously

$$q = IT = I/f$$

- This charge comes from the smoothing column, the series connection of $C_1 \ldots C_n$.
- If no charge would be transferred during T from this stack via $D'_1 \ldots D'_n$ to the oscillating column, the peak-to-peak ripple would merely be

$$2\delta V = IT \sum_{i=1}^{n} (i/C_i)$$

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Generation of high voltages ‘Direct Voltage, multiplier circuits’

- As, however, just before the time instant t_2 every diode $D'_1 \ldots D'_n$ transfers the same charge q, and each of these charges discharges all capacitors on the smoothing column between the relevant node and ground potential, the total ripple will be

$$2\delta V = IT \sum_{i=1}^{n} (i/C_i)$$

$$\delta V = \frac{I}{2f}\left[\frac{1}{C_1} + \frac{2}{C_2} + \frac{3}{C_3} + \ldots + \frac{n}{C_n}\right]$$

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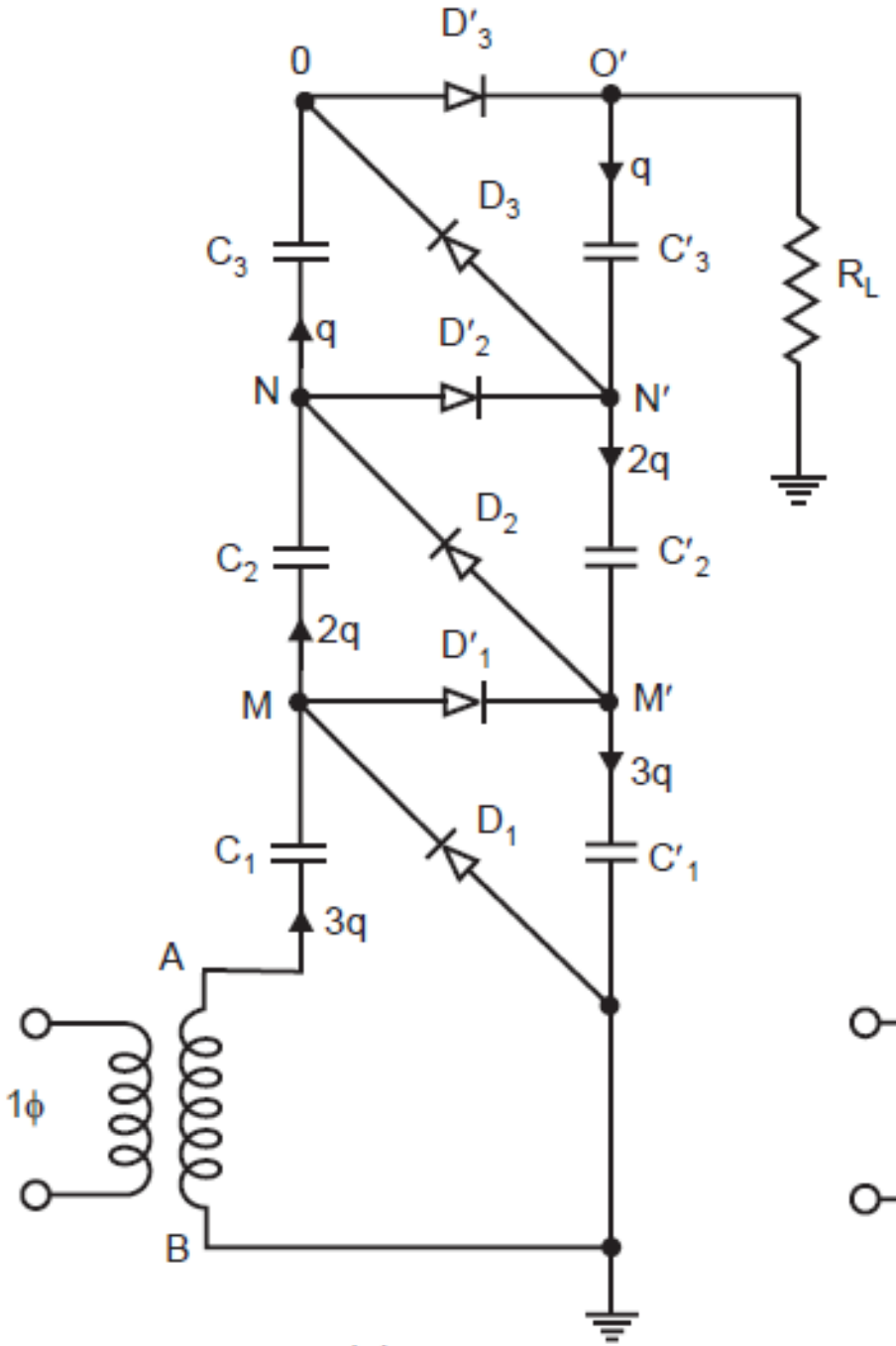
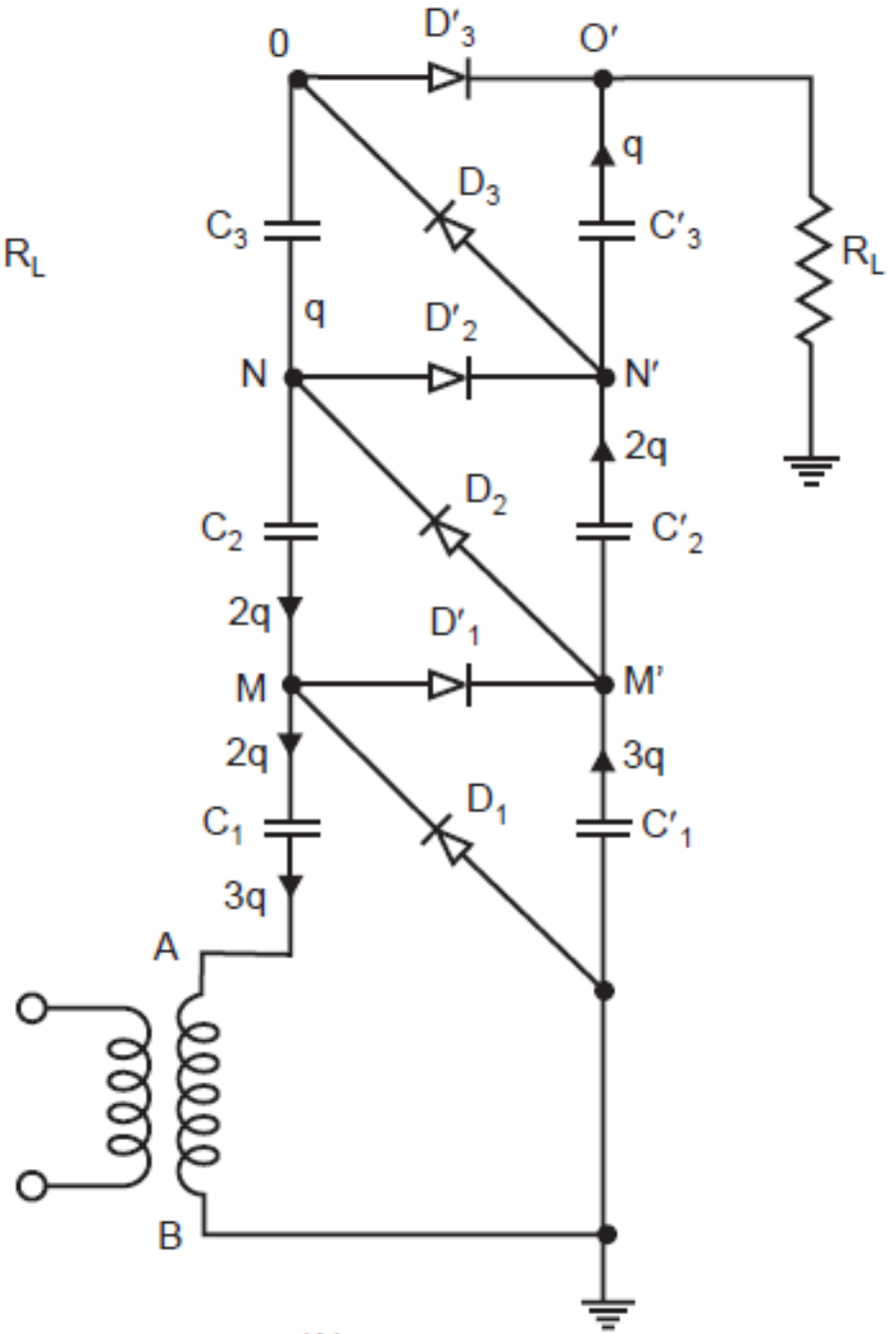
(a) Charging of smoothening column

(b) Charging of oscillating column



(a)



(b)

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Generation of high voltages
'Direct Voltage, multiplier circuits'

- Thus in a cascade multiplier the lowest capacitors are responsible for most ripple and it would be desirable to increase the capacitance in the lower stages.
- This is, however, very inconvenient for h.v. cascades, as a voltage breakdown at the load would completely overstress the smaller capacitors within the column. Therefore, equal capacitance values are usually provided, and with $C = C_1 = C_2 = \ldots = C_n$:

$$\delta V = \frac{I}{2f}\left[\frac{1}{C} + \frac{2}{C} + \frac{3}{C} + \ldots + \frac{n}{C}\right] = \frac{I}{2fC}\left[1 + 2 + 3 + \ldots + n\right] = \frac{I}{4fC}n(n+1)$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

Voltage drop ΔV_0

- It is the difference between the theoretical no load voltage $2nV_{max}$ and the on load voltage.
- Assuming that the diodes are ideal and there is no voltage drop within the AC sources, the capacitor C_1 will be charged up to the full voltage V during the negative half cycle.
- Since the capacitor C_2 has lost a total charge of nq during the previous cycle and C_1 has to replace this lost charge, C_2 will be charged to a voltage given by:

$$v_{C_2,\max} = 2V - n\frac{q}{C_1}$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

- When the source voltage reaches $-V$, the capacitor C_2 will transfer equal amounts of q to C_3, C_5 … C_{2n-1} and the load during the period T. Therefore, C_3 will be charged up to a maximum voltage given by:

$$v_{C_3,\max} = v_{C_2,\max} - n\frac{q}{C_2} = 2V - n\frac{q}{C_1} - n\frac{q}{C_2}$$

- Since the capacitor C_4 has lost a total charge of $(n-1)q$ during the previous cycle and C_3 has to replace this lost charge, C_4 will be charged to a voltage given by:

$$v_{C_4,\max} = v_{C_3,\max} - (n-1)\frac{q}{C_3} = 2V - n\frac{q}{C_1} - n\frac{q}{C_2} - (n-1)\frac{q}{C_3}$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

- When the source voltage reaches −V, the capacitor C4 will transfer equal amounts of q to C_5, C_7 … C_{2n-1} and the load during the period T. Therefore, C_5 will be charged up to a maximum voltage given by:

$$v_{C_5,\max} = v_{C_4,\max} - (n-1)\frac{q}{C_4} = 2V - n\frac{q}{C_1} - n\frac{q}{C_2} - (n-1)\frac{q}{C_3} - (n-1)\frac{q}{C_4}$$

- Since the capacitor C_6 has lost a total charge of $(n-2)q$ during the previous cycle and C_5 has to replace this lost charge, C_6 will be charged to a voltage given by:

$$v_{C_6,\max} = v_{C_5,\max} - (n-2)\frac{q}{C_5} = 2V - n\frac{q}{C_1} - n\frac{q}{C_2} - (n-1)\frac{q}{C_3} - (n-1)\frac{q}{C_4} - (n-2)\frac{q}{C_5}$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

- If all the capacitors are equal and be equal to C, the voltage drop across capacitors C_2, C_4 … C_{2n}, can be expressed as:

$$\Delta v_{C_2} = \frac{q}{C}[n]$$

$$\Delta v_{C_4} = \frac{q}{C}\left[2n + (n-1)\right]$$

$$\Delta v_{C_6} = \frac{q}{C}\left[2n + 2(n-1) + (n-2)\right]$$

$$\vdots$$

$$\Delta v_{C_{2n}} = \frac{q}{C}\left[2n + 2(n-1) + 2(n-2) + \cdots + 2\times 2 + 1\right]$$

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Generation of high voltages ‘Direct Voltage, multiplier circuits’

- After omitting *I/fC*

$$
\begin{aligned}
T_n &= n \\
T_{n-1} &= \left[2n + (n-1)\right] \\
T_{n-2} &= \left[2n + 2(n-1) + (n-2)\right] \\
T_{n-3} &= \left[2n + 2(n-1) + 2(n-2) + (n-3)\right] \\
&\vdots \\
T_1 &= \left[2n + 2(n-1) + 2(n-2) + \cdots + 2\times 3 + 2\times 2 + 1\right] \\
T &= T_n + T_{n-1} + T_{n-2} + \cdots + T_1
\end{aligned}
$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

$$T = \left[n + (n-1) + (n-2) + \cdots + 2 + 1\right]$$
$$+ \left[2n + 2(n-1) + 2(n-2) + \cdots + 2 \times 2\right]$$
$$+ \left[2n + 2(n-1) + \cdots + 2 \times 4 + 2 \times 3\right]$$
$$+ \left[2n + 2(n-1) + \cdots + 2 \times 4\right]$$
$$+ \left[2n + 2(n-1) + 2(n-2) + \cdots + 2 \times 5\right] + \cdots + 2n$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

$$
\begin{aligned}
T &= \left[n+(n-1)+(n-2)+\cdots+2+1\right] \\
&+\left[2n+2(n-1)+2(n-2)+\cdots+2\times2+2\times1\right]-2\times1 \\
&+\left[2n+2(n-1)+2(n-2)+\cdots+2\times4+2\times3+2\times2+2\times1\right]-2\times2-2\times1 \\
&+\left[2n+2(n-1)+2(n-2)+\cdots+2\times4+2\times3+2\times2+2\times1\right]-2\times3-2\times2-2\times1 \\
&\vdots \\
&+\left[2n+2(n-1)+\cdots+2\times2+2\times1\right]-\left[2(n-1)+2(n-2)+\cdots+2\times2+2\times1\right]
\end{aligned}
$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

$$T = \left[n + (n-1) + (n-2) + \cdots + 2 + 1\right] +$$
$$+ (n-1)\left[2n + 2(n-1) + 2(n-2) + \cdots + 2\times 2 + 2\times 1\right] -$$
$$- 2\left[(1) + (1+2) + (1+2+3) + \cdots + (1+2+3+\cdots+(n-1))\right]$$

$$T = \left[n + (n-1) + (n-2) + \cdots + 2 + 1\right] +$$
$$+ (n-1)\left[2n + 2(n-1) + 2(n-2) + \cdots + 2\times 2 + 2\times 1\right] -$$
$$-2\left[(1) + (1+2) + (1+2+3) + \cdots + (1+2+3+\cdots+(n-1)) + (1+2+3+\cdots+n)\right]$$
$$+2\left[1+2+3+\cdots+n\right]$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

$$T = \sum_{k=1}^{n}(k) + 2(n-1)\sum_{k=1}^{n}(k) - \left[\sum_{k=1}^{n}\left(k^2+k\right) - 2\sum_{k=1}^{n}(k)\right]$$

$$= \sum_{k=1}^{n}(k) + 2n\sum_{k=1}^{n}(k) - 2\sum_{k=1}^{n}(k) - \sum_{k=1}^{n}\left(k^2-k\right)$$

$$= \sum_{k=1}^{n}(k) + 2n\sum_{k=1}^{n}(k) - 2\sum_{k=1}^{n}(k) - \sum_{k=1}^{n}\left(k^2\right) + \sum_{k=1}^{n}(k)$$

$$= 2n\sum_{k=1}^{n}(k) - \sum_{k=1}^{n}\left(k^2\right)$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

$$T = 2n\sum_{k=1}^{n}(k) - \sum_{k=1}^{n}(k^2) = 2n\frac{n(n+1)}{2} - \frac{n(n+1)(2n+1)}{6}$$

$$= \frac{6(n^3+n^2)-(2n^3+3n^2+n)}{6} = \frac{6n^3+6n^2-2n^3-3n^2-n}{6}$$

$$= \frac{4n^3+3n^2-n}{6} = \frac{2n^3}{3}+\frac{n^2}{2}-\frac{n}{6}$$

$$\Delta V_0 = \left[\frac{2n^3}{3}+\frac{n^2}{2}-\frac{n}{6}\right]\frac{I}{fC}$$

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Generation of high voltages
'Direct Voltage, multiplier circuits'

- However, only a doubling of C'_n is convenient, since this capacitor has to withstand only half the voltage of the other capacitors; namely V_{max}. Therefore, ΔV_n decreases by an amount of 0.5 nq/C, which reduces ΔV of every stage by the same amount, thus n times. Hence,

$$\Delta V_0 = \frac{I}{fC}\left[\frac{2n^3}{3} - \frac{n}{6}\right]$$

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- For this case and $n \geq 4$, we may neglect the linear term and therefore approximate the maximum output voltage by

$$V_{0,\max} \cong 2nV_{\max} - \frac{2In^3}{3fC}$$

- For a given number of stages, this maximum voltage or also the mean value $V_0 = V_{0,\max} - \delta V$ will decrease linearly with the load current I at constant frequency, which is obvious.

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- For a given load, however, V_0 may rise initially with the number of stages n, but reaches an optimum value and even decreases if n is too large. Thus – with respect to constant values of I, V_{max}, f and C – the highest value can be reached with the 'optimum' number of stages, obtained by differentiating last equation with respect to n. Then

$$\frac{dV_{0,\max}}{dn} = 2V_{\max} - \frac{2In_{opt}^{\ 2}}{fC} = 0$$

$$n_{\text{opt}} = \sqrt{\frac{V_{\max}\, fC}{I}}$$

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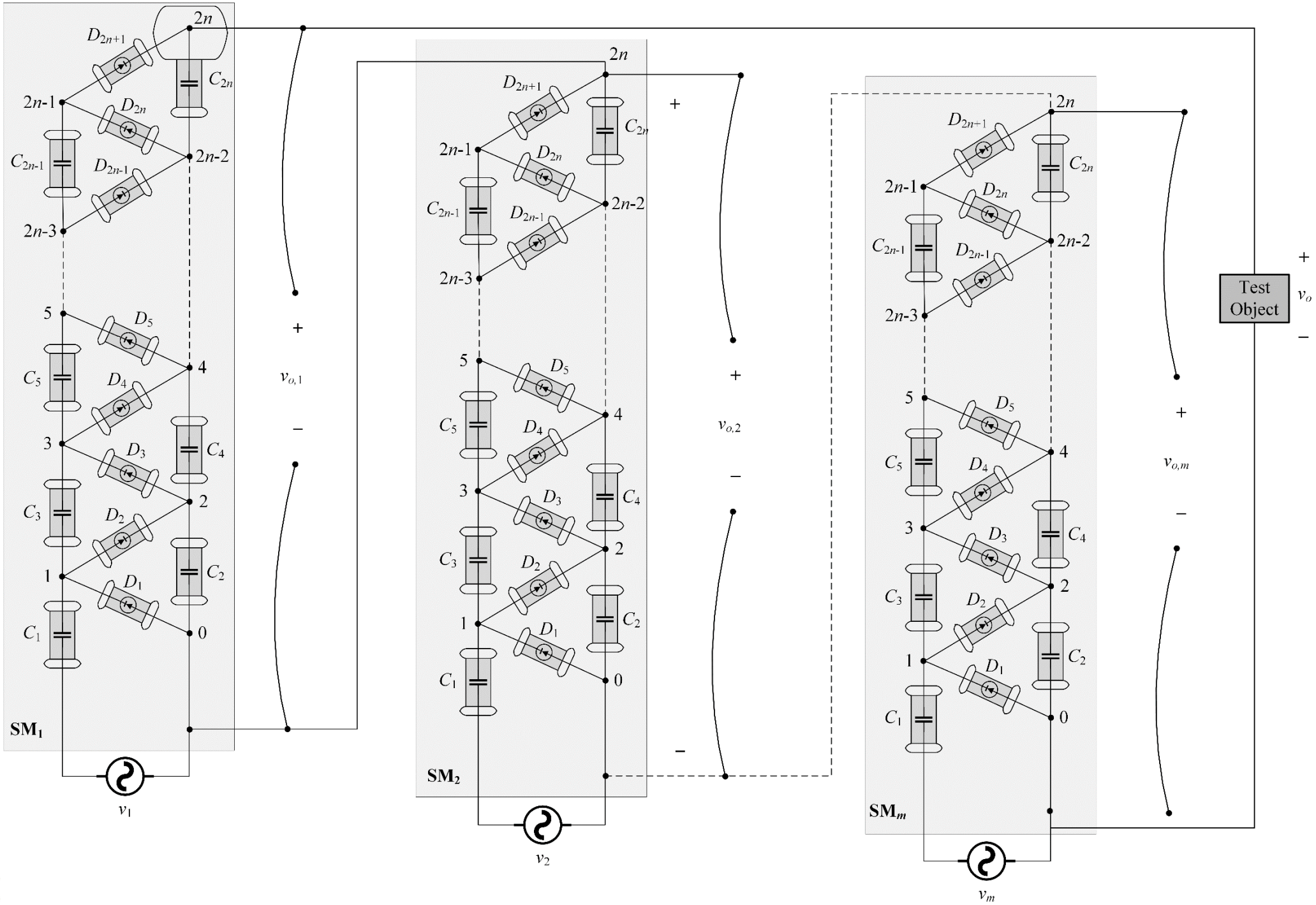
- Substituting n_{opt} in equation of $V_{0,max}$, we have

$$V_{0,\max} = \sqrt{\frac{V_{\max} fC}{I}}\left[2V_{\max} - \frac{2I}{3fC}\frac{V_{\max} fC}{I}\right]$$

$$= \sqrt{\frac{V_{\max} fC}{I}}\left[2V_{\max} - \frac{2}{3}V_{\max}\right]$$

$$= \frac{4}{3}\sqrt{\frac{V_{\max} fC}{I}}V_{\max}$$



Modular HVDC generator with embedded Cockcroft-Walton circuits.

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Generation of high voltages
'Direct Voltage, modular multiplier circuits'

- The generator consists of *m* cascaded sub-modules (SMs)), where each SM consists of a Cockcroft-Walton (CW) circuit with *n* stages with a floating AC source. The generator is fed by two ways, as shown in Fig. 2:
  - Method 1: Low power multiphase synchronous machine with star-connected stator windings. In this method, the modules are supplied by *m* isolated sources that have the same magnitude, frequency and shifted from each other by an angle of $2\pi/m$.
  - Method 2: Low power single-phase AC source. In this method, the modules are supplied via multi-winding transformer (*m* secondary windings) that have the same magnitude, frequency and phase.

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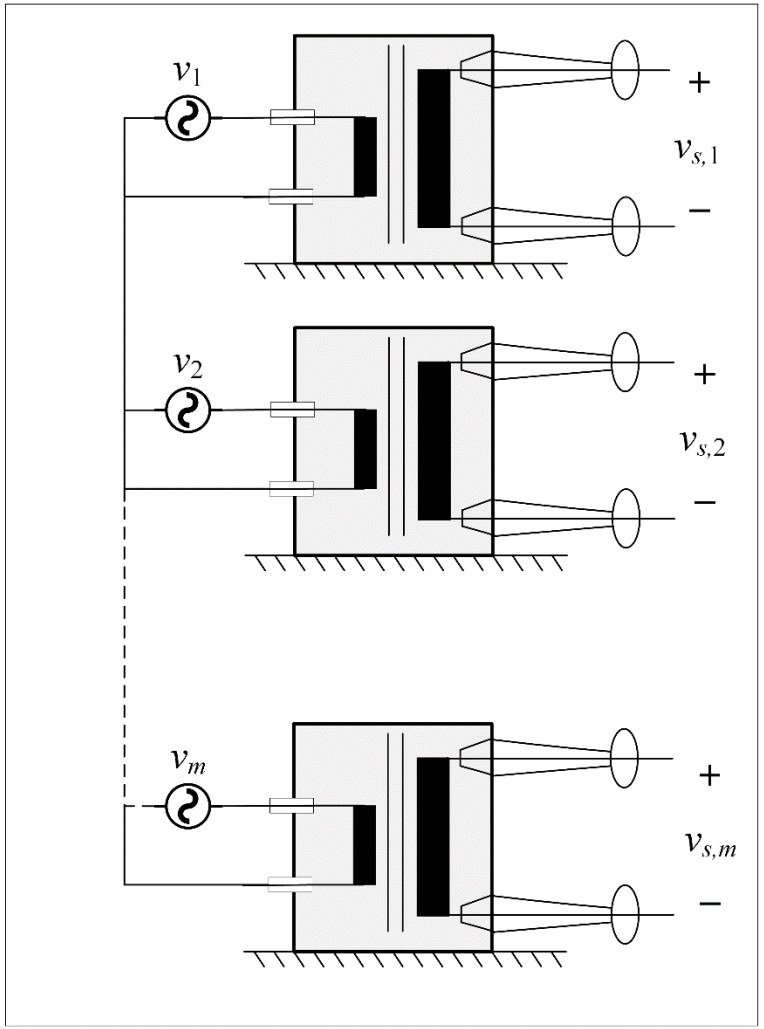
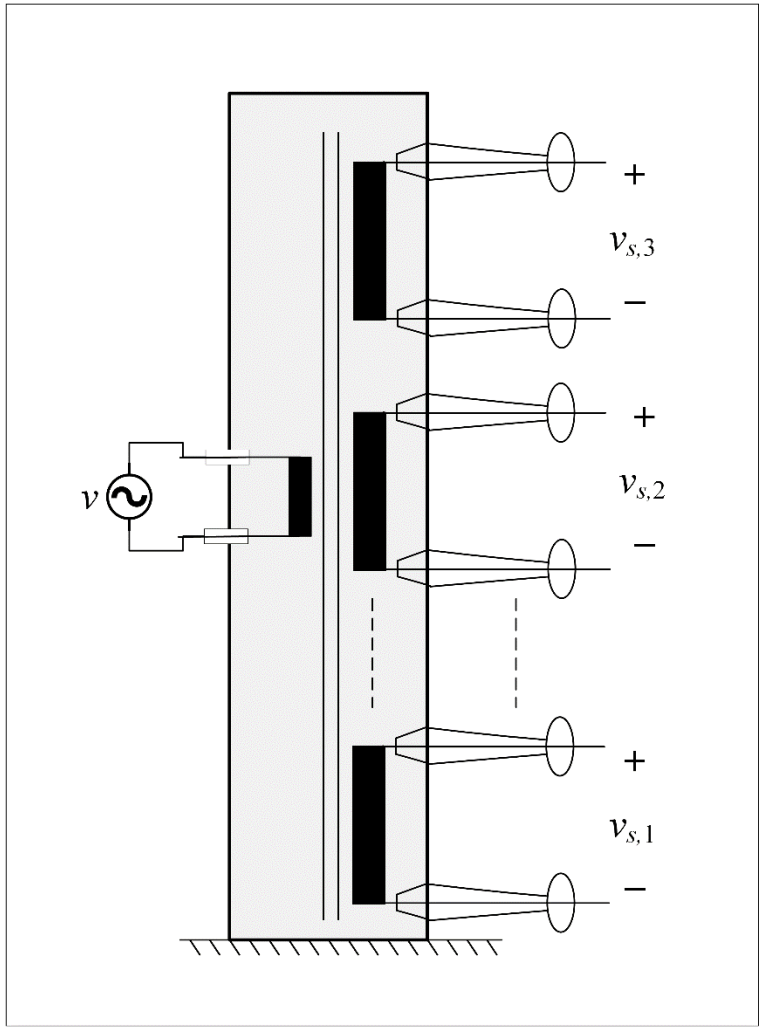


Method 1



Method 2

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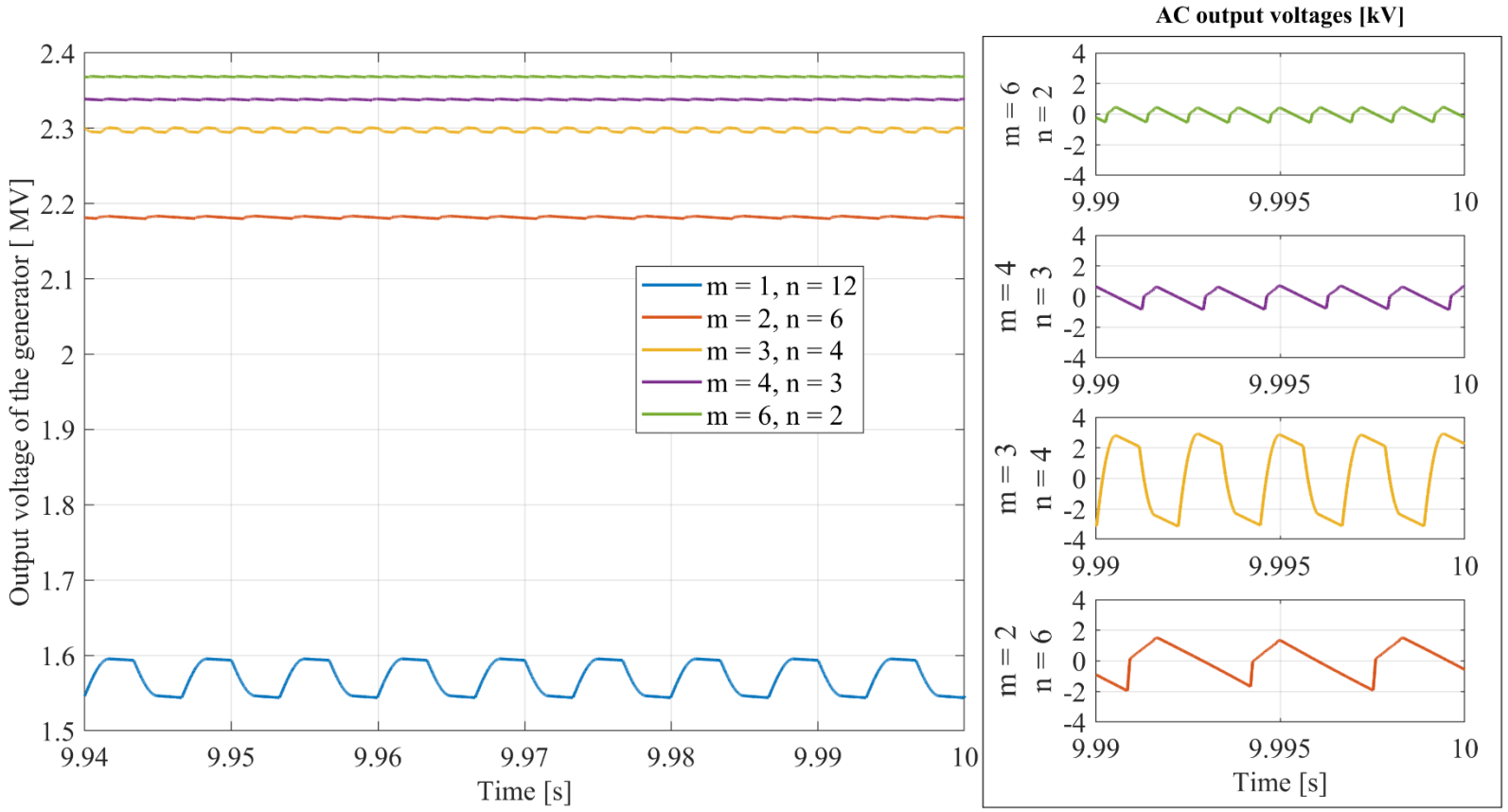

The steady state output voltages of the generator and their AC components.

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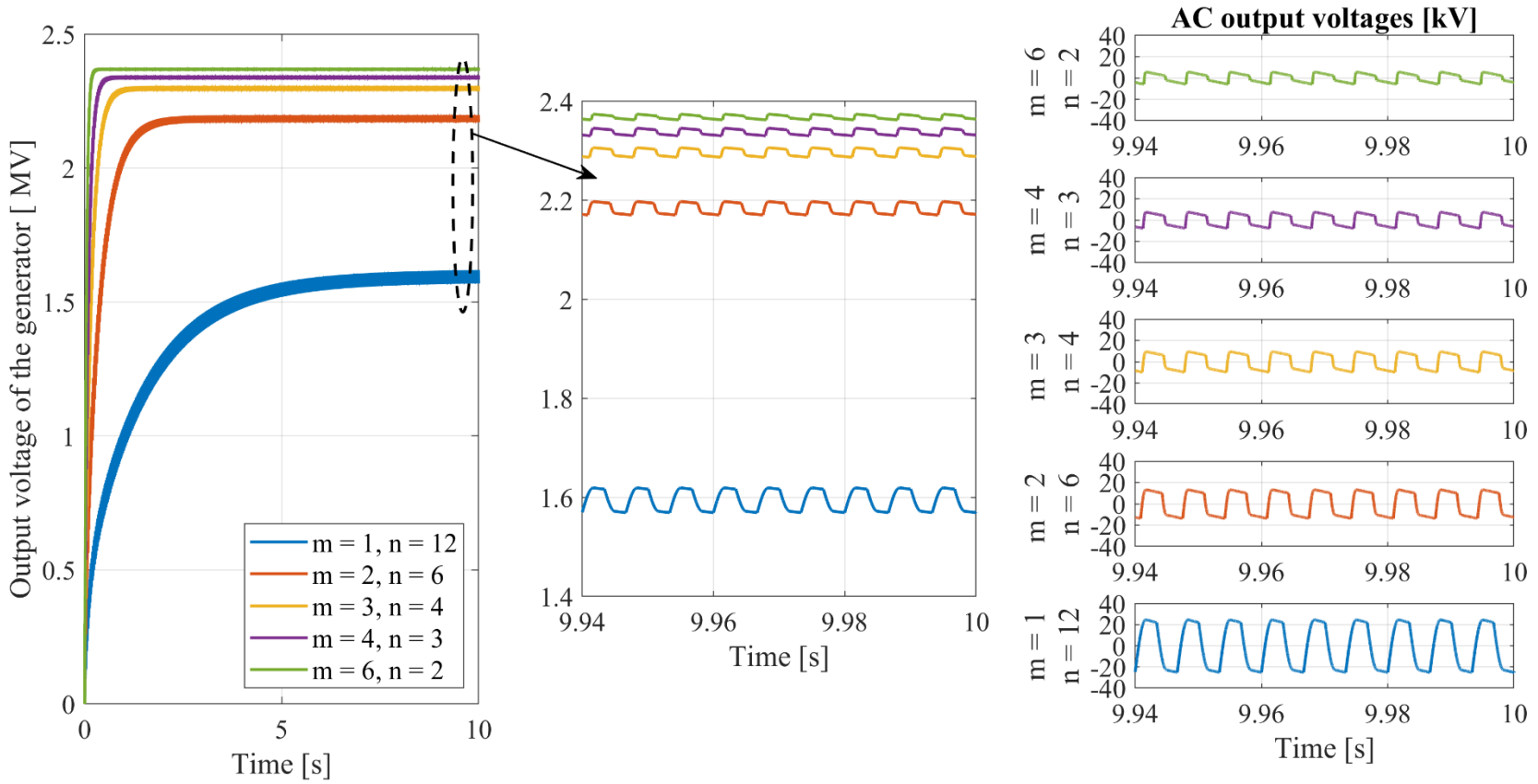
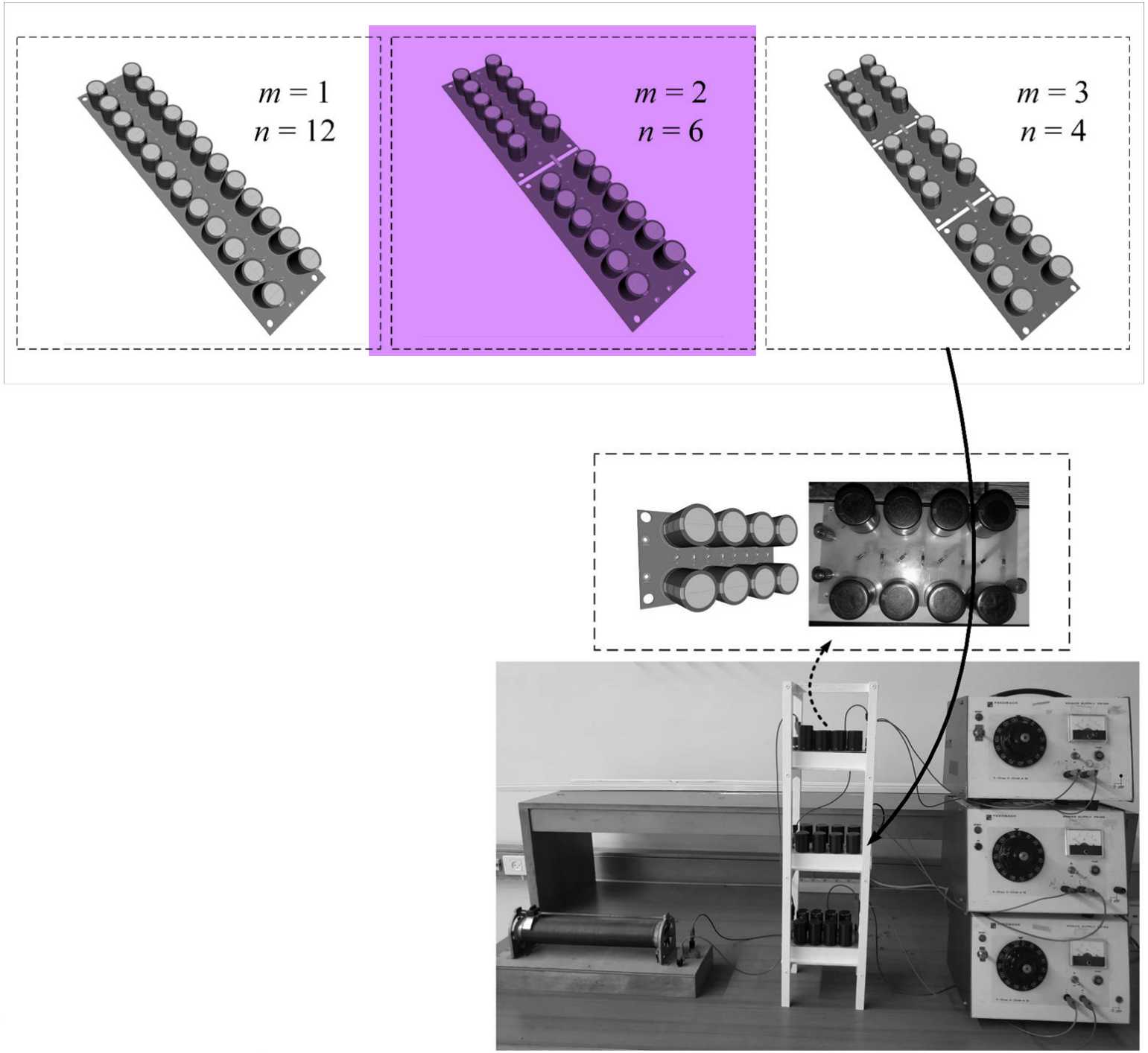
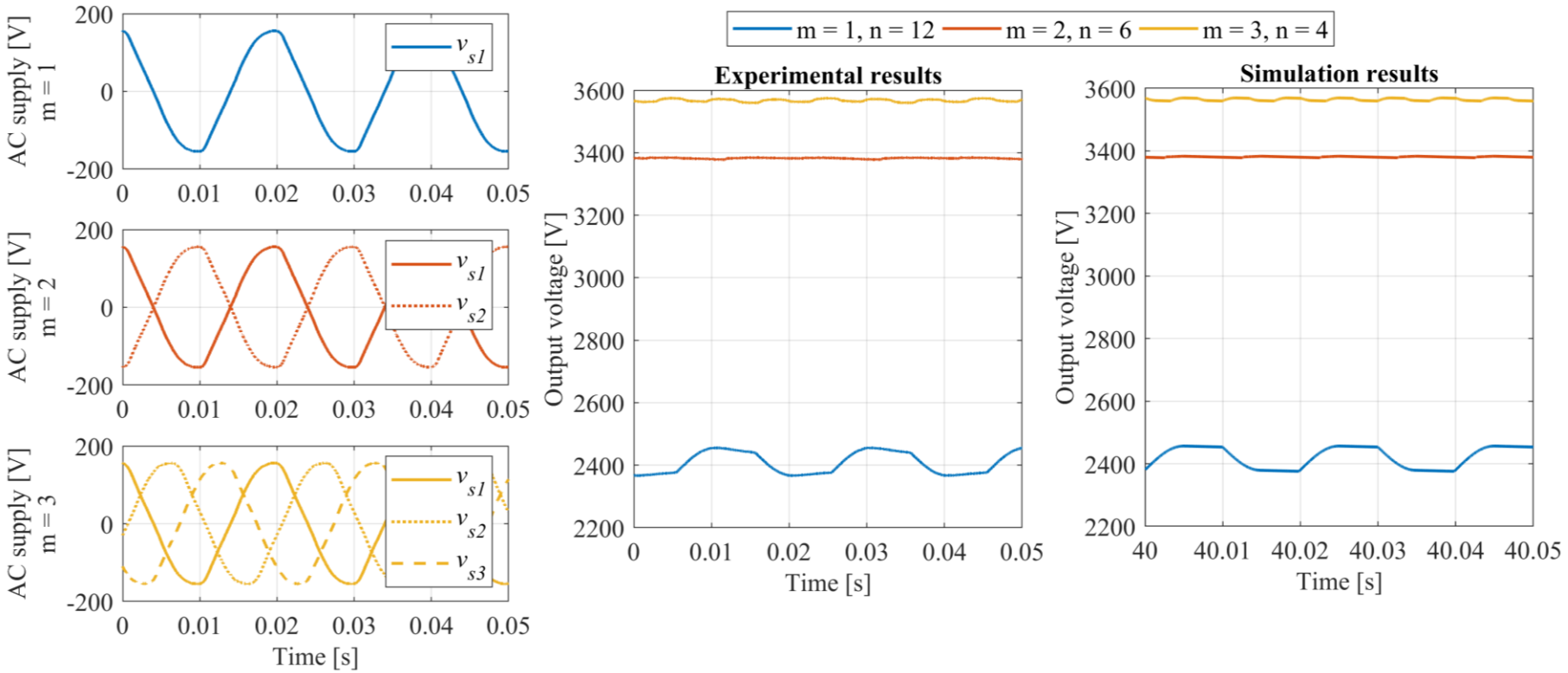


The output voltages of the generator and their AC components in the case of equal phases of input sources.



Prototype of a high voltage DC generator with three SMs



The AC source voltages and the steady state output voltages of the generator.

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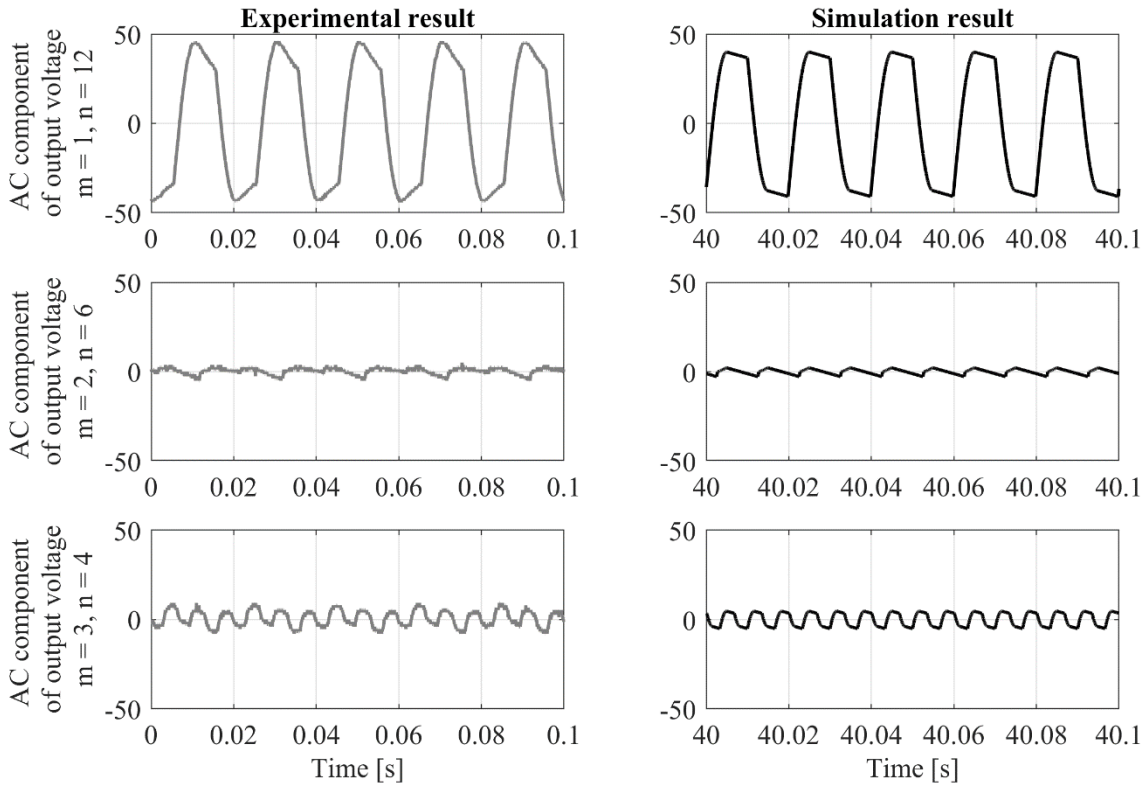

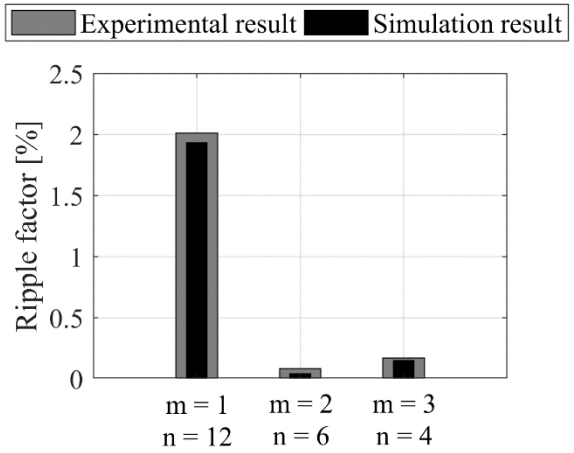

The steady state AC components of the generator output voltages and the mean values of the output voltage.

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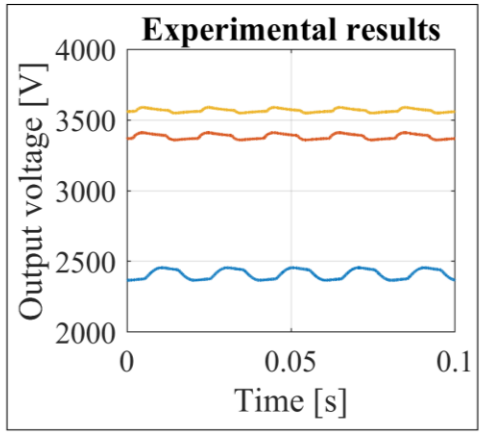

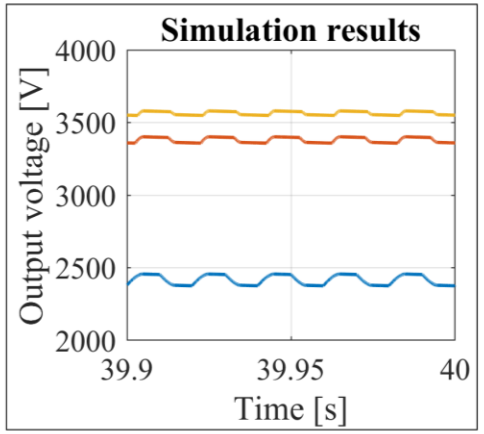

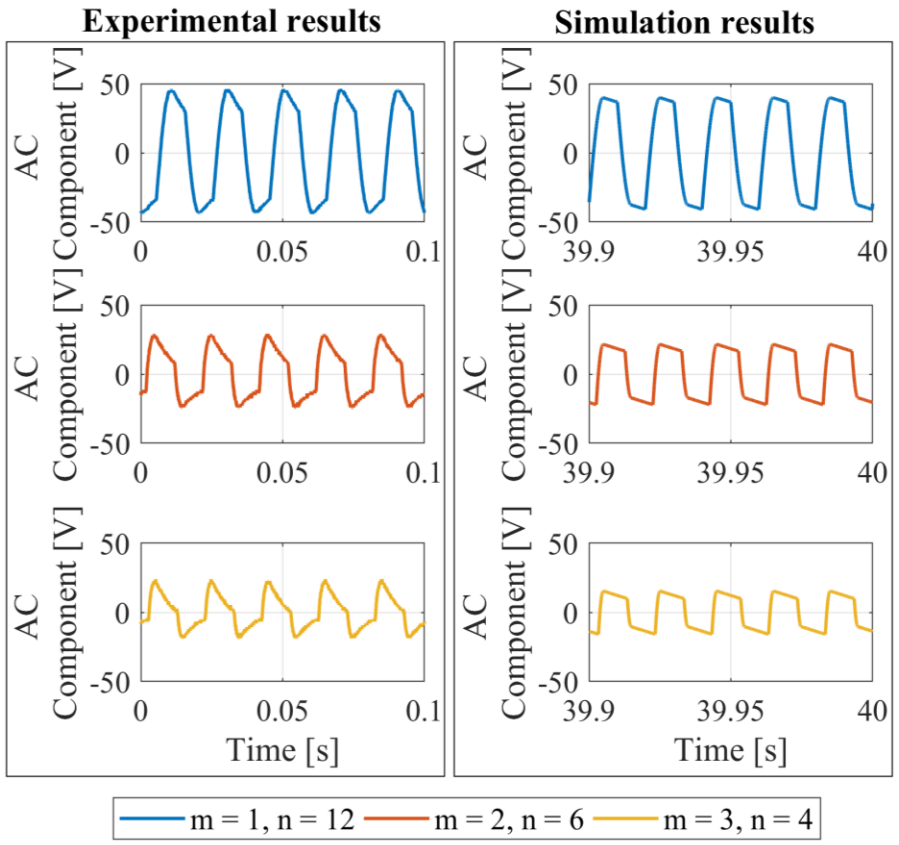

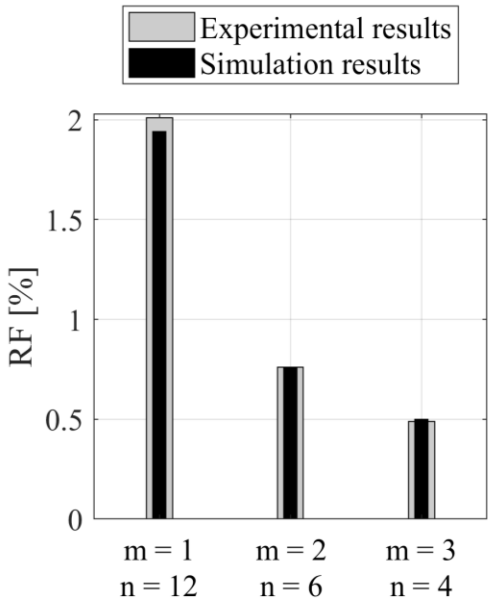

The output voltages of the generator and their AC components in the case of equal phases of input source.

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Example

A ten stage Cockraft-Walton circuit has all capacitors of 0.06 μF. The secondary voltage of the supply transformer is 100 kV at a frequency of 150 Hz. If the load current is 1 mA, determine

i. The voltage regulation
ii. The peak-to-peak ripple voltage
iii. The optimum number of stages for maximum output voltage
iv. The maximum output voltage.

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'Direct Voltage, multiplier circuits'

- Voltage drop

$$\Delta V_0 = \frac{I}{fC}\left[\frac{2n^3}{3} + \frac{n^2}{2} - \frac{n}{6}\right] = \frac{1\times10^{-3}}{150\times0.06\times10^{-6}}\left[\frac{2}{3}\times10^3\right] = 74\,\text{kV}$$

- % of voltage drop

$$\frac{74}{2\times10\times100} = 3.7\%$$

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- Peak to peak ripple voltage

$$2\delta V = \frac{I}{2fC} n(n+1) = \frac{1\times10^{-3}}{2\times150\times0.06\times10^{-6}}\left[10(11)\right] = 6.1\,\text{kV}$$

- % of ripple voltage

$$\frac{6.1}{2\times10\times100} = 0.3\%$$

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- Optimum number of stages

$$n_{\text{opt}} = \sqrt{\frac{V_{\max} fC}{I}} = \sqrt{\frac{100\times10^{3}\times150\times0.06\times10^{-6}}{10^{-3}}} = 30$$

- The maximum output voltage

$$V_{0,\max} = \frac{4}{3}\sqrt{\frac{100\times10^{3}\times150\times0.06\times10^{-6}}{10^{-3}}}100 = \frac{4}{3}\times30\times100 = 4\,\text{MV}$$